

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D $T_A = +25^\circ C$
-60V	105m Ω @ $V_{GS} = -10V$	-3.3A
	130m Ω @ $V_{GS} = -4.5V$	-3.0A

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

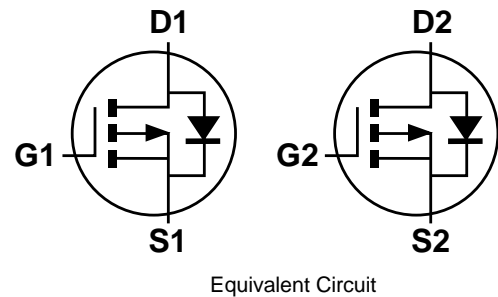
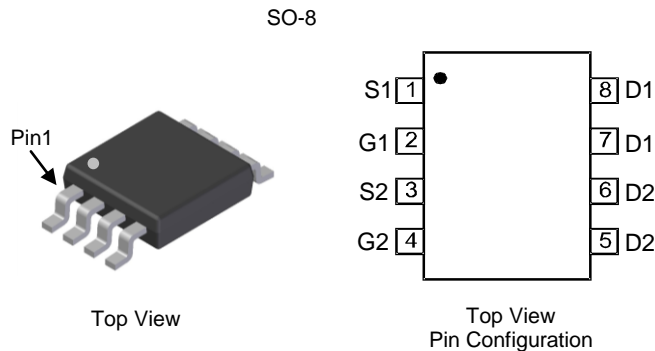
- DC-DC Converters
- Power Management Functions
- Backlighting

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (Approximate)

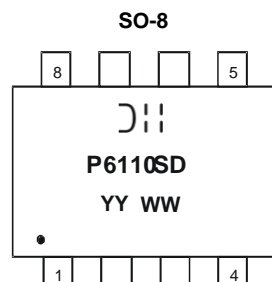


Ordering Information (Note 4)

Part Number	Case	Packaging
DMP6110SSD-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



= Manufacturer's Marking
 P6110SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Year (ex: 16 = 2016)
 WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V _{DSS}	-60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = -10V	T _C = +25°C T _C = +70°C	I _D	-7.8 -6.3	A
	T _A = +25°C T _A = +70°C	I _D	-3.3 -2.7	A
Pulsed Drain Current (380µs Pulse, 1% Duty Cycle)		I _{DM}	-24	A
Maximum Continuous Body Diode Forward Current (Note 6)		I _S	-1.8	A
Avalanche Current (Note 9) L = 0.1mH		I _{AS}	-19	A
Avalanche Energy (Note 9) L = 0.1mH		E _{AS}	18	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5 & 7)	T _A = +25°C	P _D	1.2	W
	T _A = +70°C		0.9	
Total Power Dissipation (Note 5 & 8)	T _A = +25°C		1.2	
Thermal Resistance, Junction to Ambient (Note 5 & 7)	Steady State	R _{θJA}	104	°C/W
	t < 10s		45	
Thermal Resistance, Junction to Ambient (Note 5 & 8)	Steady State		100	
Total Power Dissipation (Note 6 & 7)	T _A = +25°C	P _D	1.7	W
	T _A = +70°C		1.1	
Total Power Dissipation (Note 6 & 8)	T _A = +25°C		1.8	
Thermal Resistance, Junction to Ambient (Note 6 & 7)	Steady State	R _{θJA}	74	°C/W
	t < 10s		37	
Thermal Resistance, Junction to Ambient (Note 6 & 8)	Steady State		71	
Thermal Resistance, Junction to Case (Note 6 & 7)		R _{θJC}	15	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. For a dual device with one active die.
 8. For a device with two active die running at equal power.
 9. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 10)						
Drain-Source Breakdown Voltage	BV _{DSS}	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1	μA	V _{DS} = -48V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	100	nA	V _{GS} = ±16V, V _{DS} = 0V
ON CHARACTERISTICS (Note 10)						
Gate Threshold Voltage	V _{GS(TH)}	-1	—	-3	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	—	105	mΩ	V _{GS} = -10V, I _D = -4.5A
		—	—	130		V _{GS} = -4.5V, I _D = -3.5A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 11)						
Input Capacitance	C _{ISS}	—	969	—	pF	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	—	57	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	44	—	pF	
Gate Resistance	R _G	—	13.7	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _G	—	8.2	—	nC	V _{DS} = -30V, I _D = -12A
Total Gate Charge (V _{GS} = -10V)	Q _G	—	17.2	—	nC	V _{DS} = -30V, I _D = -12A
Gate-Source Charge	Q _{GS}	—	3.0	—	nC	
Gate-Drain Charge	Q _{GD}	—	3.1	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	4.4	—	ns	V _{GS} = -10V, V _{DS} = -30V, R _{GEN} = 3Ω, I _D = -12A
Turn-On Rise Time	t _R	—	23	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	34	—	ns	
Turn-Off Fall Time	t _F	—	42	—	ns	I _S = -12A, di/dt = 100A/μs
Body Diode Reverse Recovery Time	t _{RR}	—	13.2	—	ns	
Body Diode Reverse Recovery Charge	Q _{RR}	—	6.18	—	nC	

- Notes: 10. Short duration pulse test used to minimize self-heating effect.
11. Guaranteed by design. Not subject to product testing.

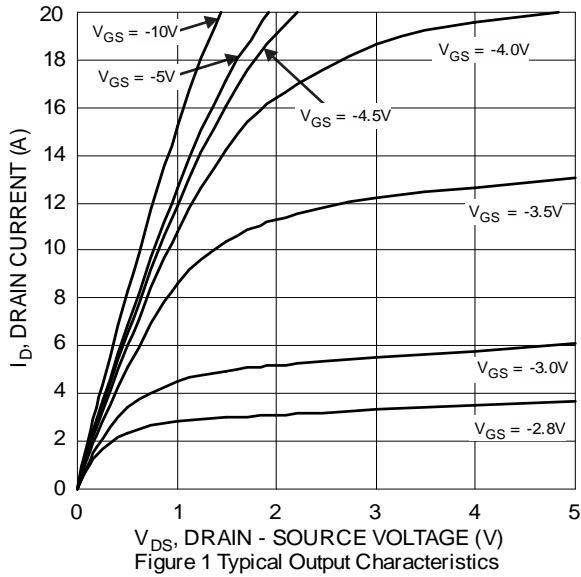


Figure 1 Typical Output Characteristics

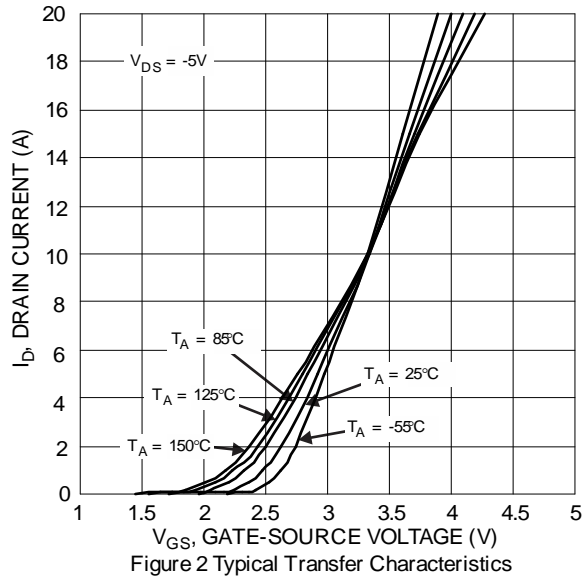


Figure 2 Typical Transfer Characteristics

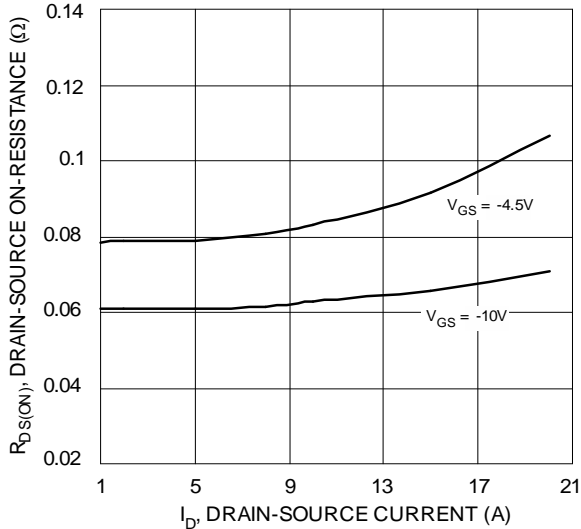


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

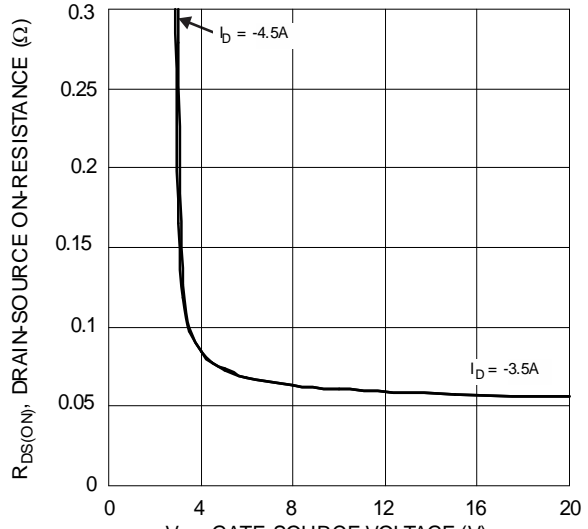


Figure 4 Typical Transfer Characteristics

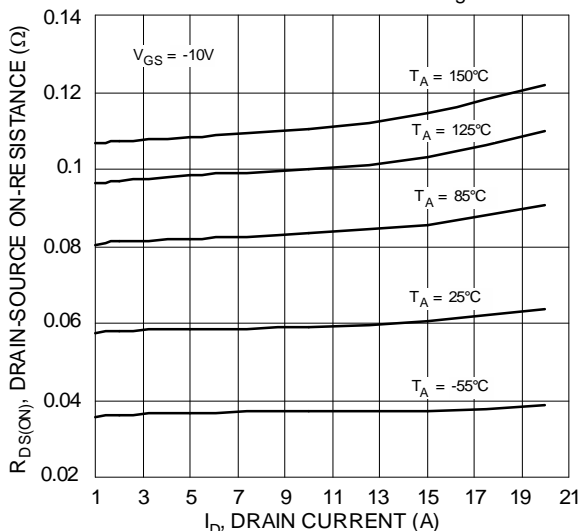


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

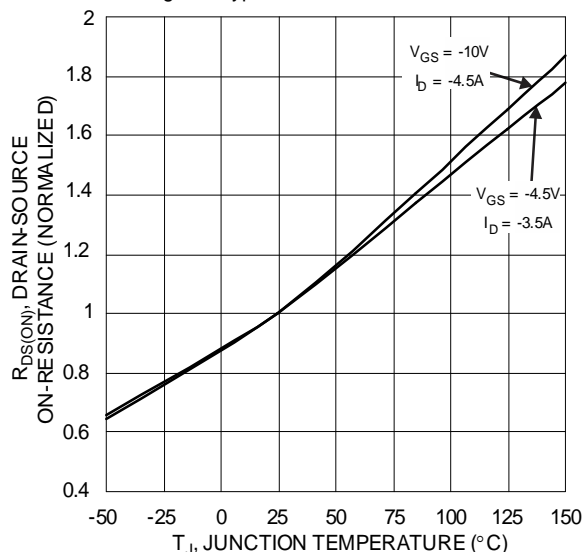


Figure 6 On-Resistance Variation with Temperature

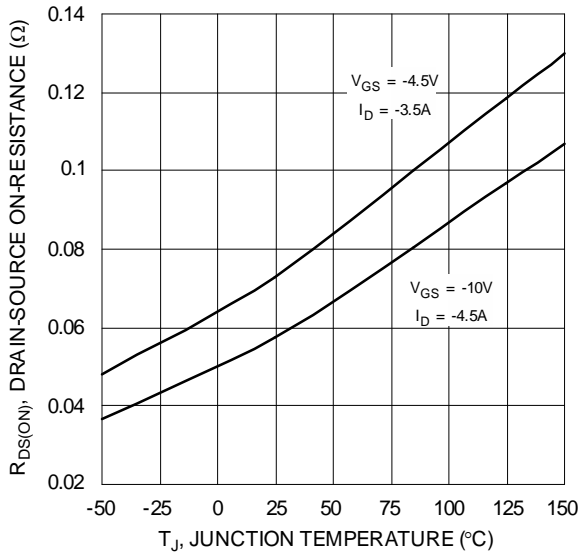


Figure 7 On-Resistance Variation with Temperature

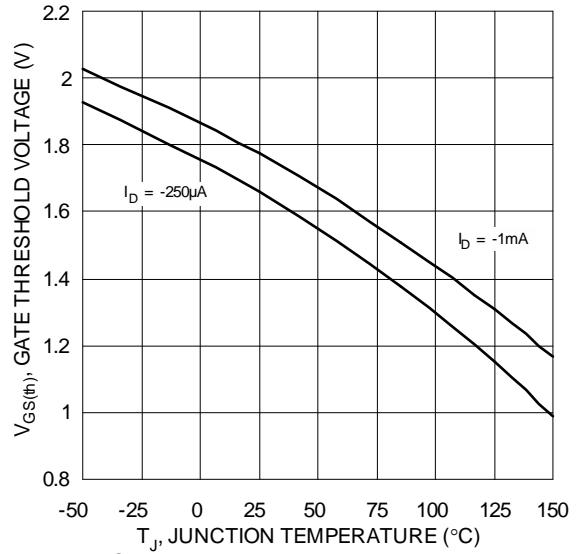


Figure 8 Gate Threshold Variation vs. Junction Temperature

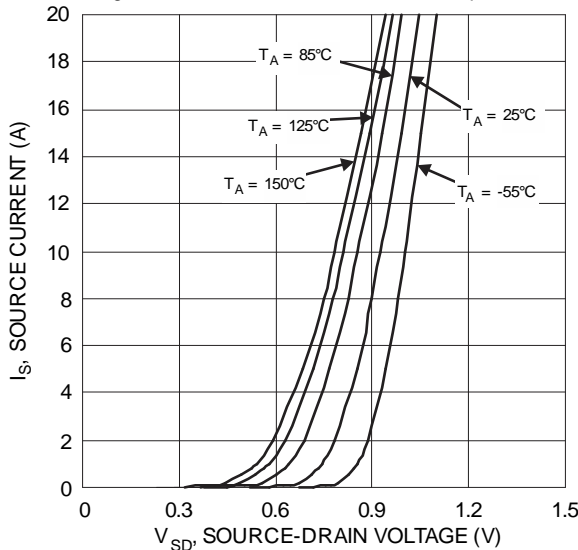


Figure 9 Diode Forward Voltage vs. Current

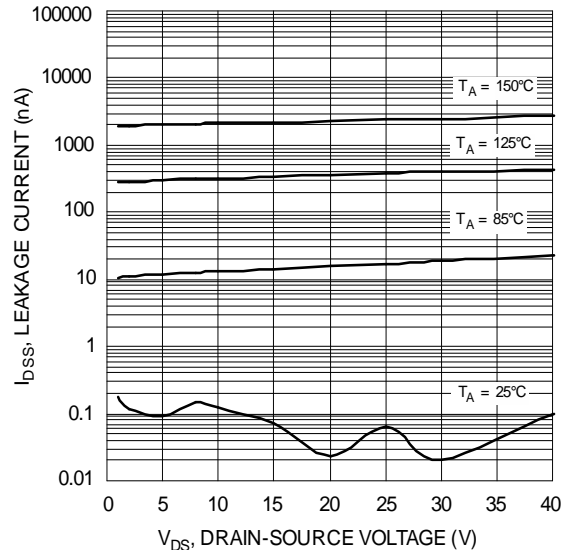


Figure 10 Typical Drain-Source Leakage Current vs. Voltage

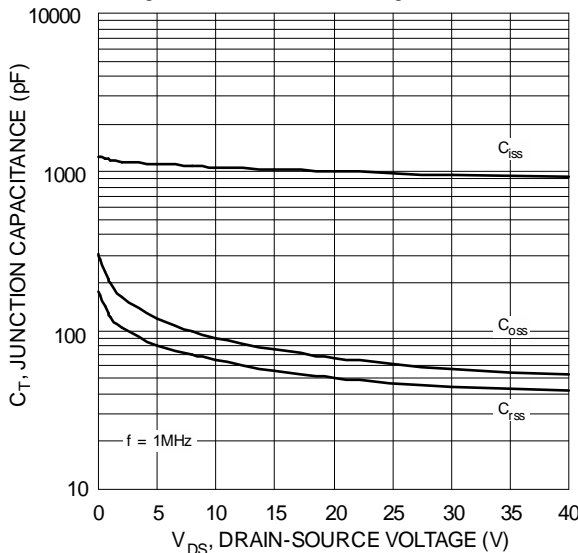


Figure 11 Typical Junction Capacitance

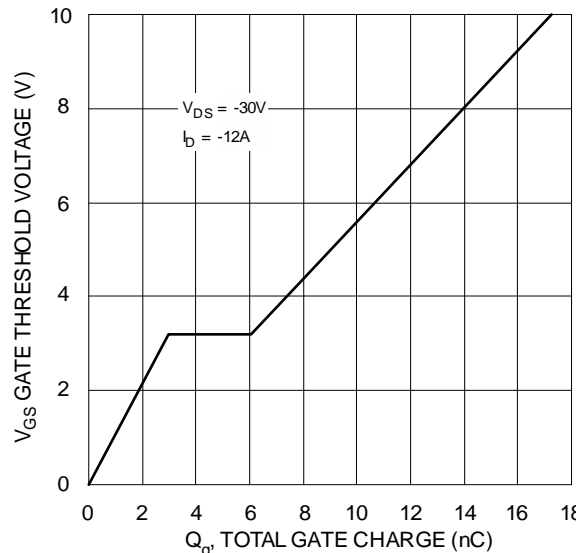
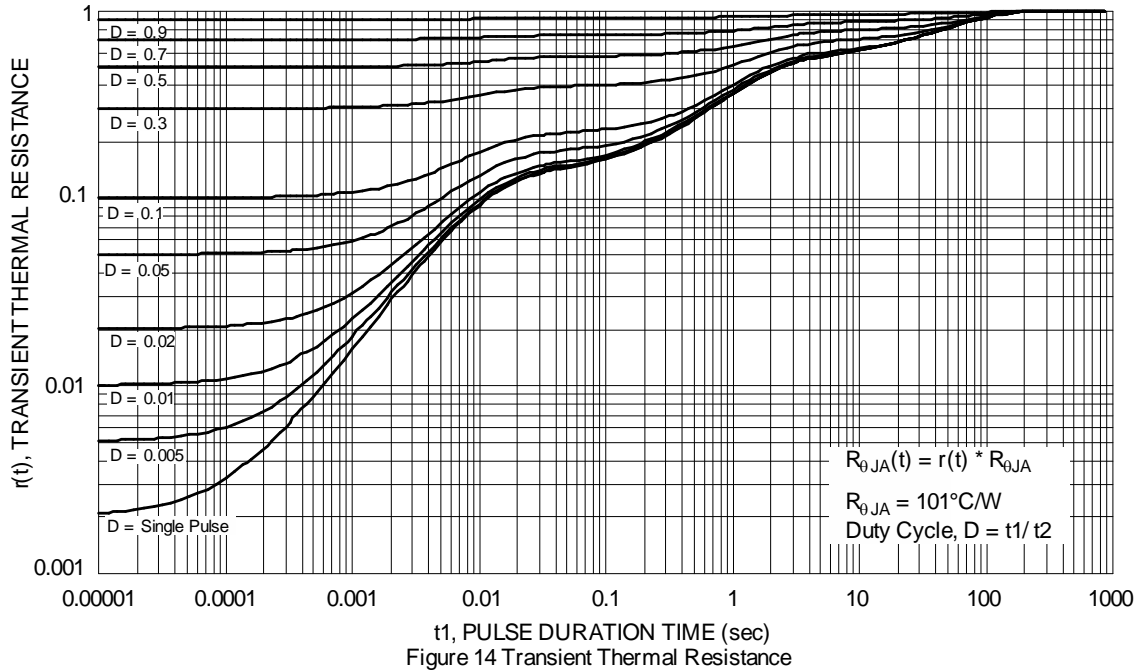
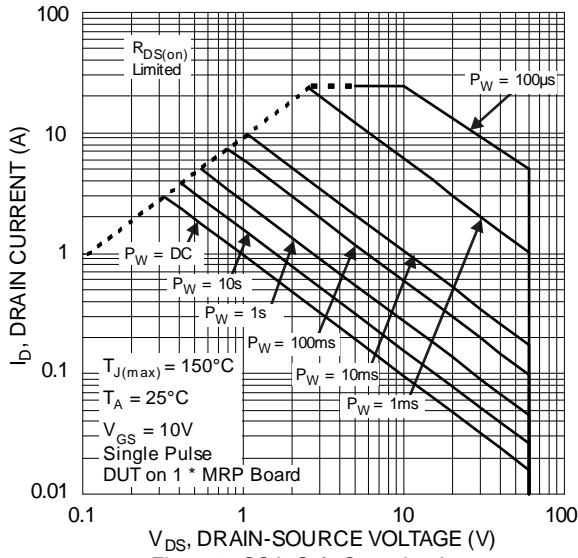


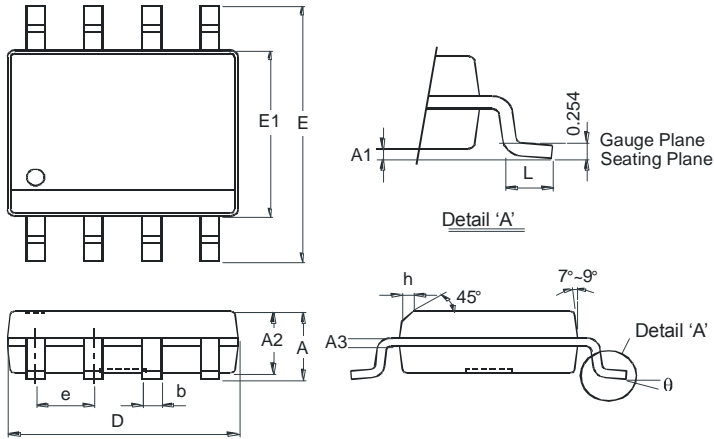
Figure 12 Gate Charge



Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8

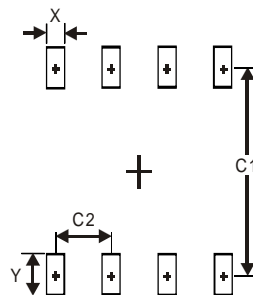


SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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