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FSA8069

Audio Jack IC Featuring Impedance and Moisture Detection

Features

- Detection:
 - Accessory Plug-In
 - Send / End Key Press
 - Impedance Detection
 - Prevents False Detection due to Moisture
- V_{DD} : 3.0 V to 4.5 V
- V_{IO} : 1.6 V to V_{DD}
- THD (MIC): 0.01% Typical
- 15 kV Air Gap ESD
- Detects 7 Steps of Headset Impedance
- Integrates LDO for MIC Bias Circuit
- MIC Switch Removes Audio Jack “Pop” and “Click” Caused by MIC Bias

Description

The FSA8069 is an audio jack detection switch for 3.5 mm and 2.5 mm headsets. The FSA8069 features impedance detection and moisture sensing, which prevents false detection of accessories in the audio jack. An integrated MIC switch allows a processor to configure attached accessories. An LDO provides DC bias to microphone and remote key circuit in accessory. The FSA8069 detects seven headset impedance steps and supports configurable gain in the amplifier according to the type of load. The architecture is designed to allow headphones to be used for listening to music from mobile handsets, personal media players, and portable peripheral devices.

Applications

- Any Device with 3.5 mm and 2.5 mm Audio Jack
- Cellular Phones, Smart Phones, and Tablets
- MP3, GPS, and PMP

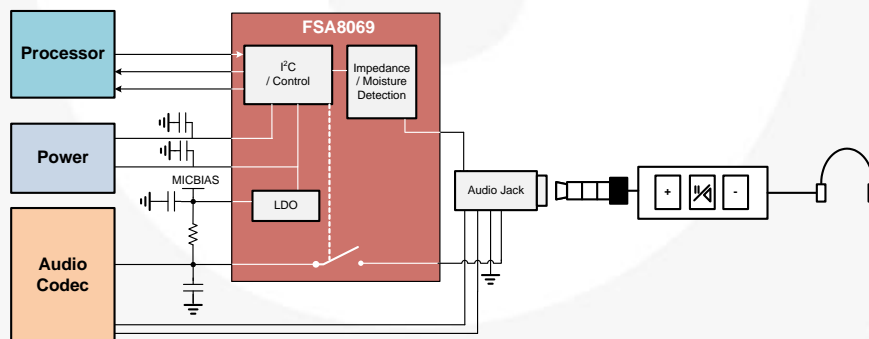


Figure 1. Block Diagram

Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package | Packing Method |
|---------------------------|-----------------------------|----------|--|----------------|
| FSA8069UCX ⁽¹⁾ | -40°C to 85°C | MX | 12-Ball WLCSP, 1.415 mm x 1.615 mm, 0.4 mm Pitch | Tape & Reel |

Notes:

1. Includes backside lamination.

Typical Application Diagram

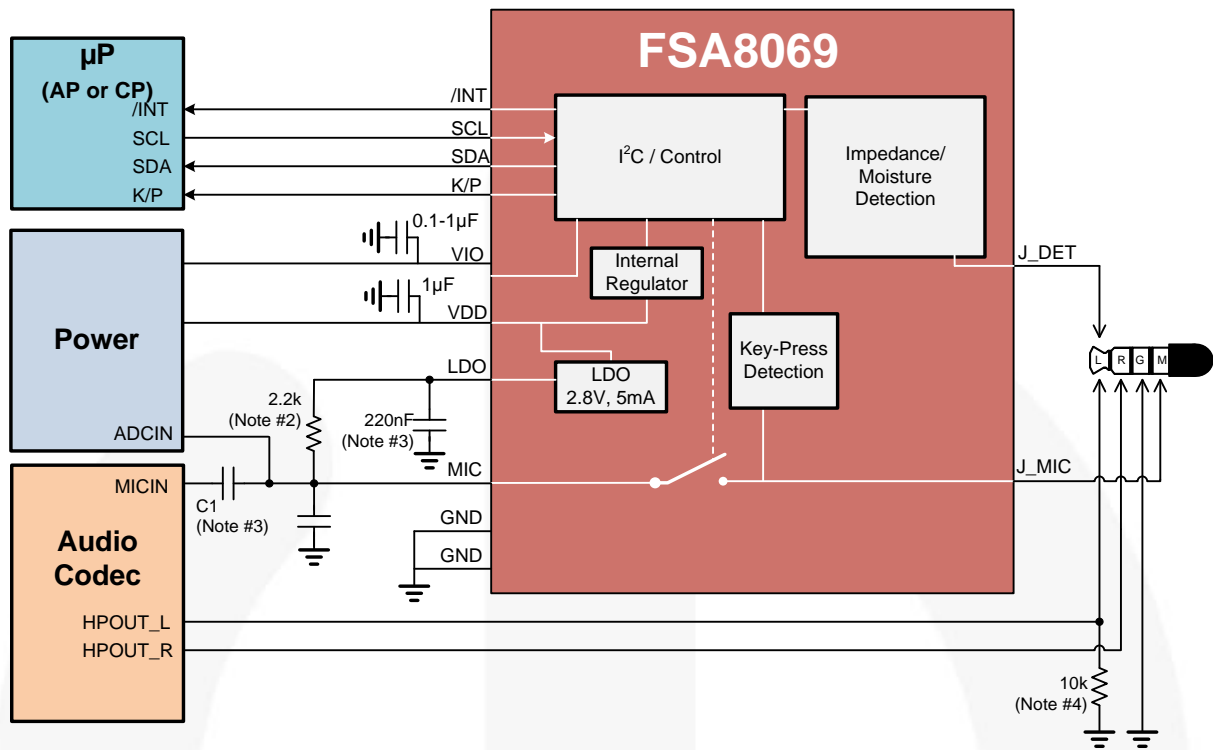


Figure 2. System Diagram

Notes:

- 2.2 kΩ can generally be used in applications to bias the accessory microphone. Two separate resistors totaling 2.2 kΩ with a large capacitor between them can improve noise rejection performance, as shown in Figure 7.
- A DC-blocking capacitor (typically 1 μF) should be used when the codec requires AC-coupled input only. This capacitor can be removed and be tied to directly without C1 if the MICIN of the codec supports DC-coupled input.
- A pull-down resistor allows the FSA8069 to detect Hi-Z (open cable) type accessories due to J_DET contact to left when an accessory is inserted.

Pin Configuration

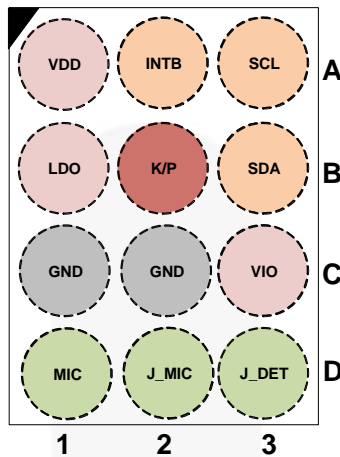


Figure 3. Pin Assignment (Through View)

Pin Definitions

| Name | Pin # | Type | Description |
|-------|--------|-----------------|---|
| VDD | A1 | Power | Device supply (3.0 V to 4.5 V) |
| VIO | C3 | Power | I/O supply (1.6 V to V _{DD}) |
| LDO | B1 | Power | LDO output (2.8 V) |
| J_DET | D3 | Detection Input | Input from the audio jack; plug insert / removal detection pin |
| MIC | D1 | Signal Path | Microphone switch path that connects to the microphone input of the codec |
| J_MIC | D2 | Signal Path | Microphone switch path that connects to the audio jack |
| SDA | B3 | DATA | I ² C data |
| SCL | A3 | DATA | I ² C clock |
| INTB | A2 | Output | Interrupt output LOW: interrupt is asserted (active) HIGH: interrupt is not asserted |
| K/P | B2 | Output | Indicates state of headset key for a 4-pole jack when a key is being pressed HIGH: Key is being pressed LOW: Key is not being pressed |
| GND | C1, C2 | Power | Device ground |

Application Information

Moisture Detection

Moisture in the audio jack can cause the phone to incorrectly route audio signals to the audio jack rather than the phone speaker or microphone. Users perceive this as a dropped call or muted phone. The FSA8069 protects against this type of false plug insertion notification and asserts a Moisture Change interrupt in Interrupt1 (0x04h) Register.

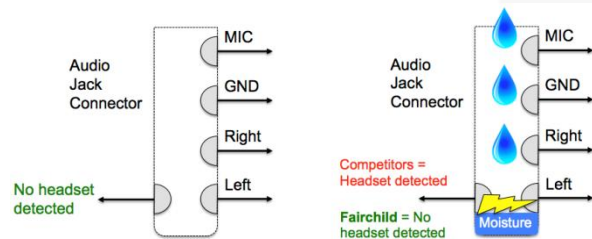


Figure 4. Moisture Impedance Detection

Music Mode

When a 4-pole headset is inserted into the audio jack and a music/listening application is used, the MIC bias is normally enabled for headset button press detection (i.e. mute, volume change, etc.). This consumes power due to a constant path from the MIC bias resistor and microphone in the headset to GND. Fairchild has developed a Music Mode to enable the MIC switch periodically to monitor for a pressed button. This results in a power savings for battery-sensitive devices, such as cell phones or MP3 players. The FSA8069 enters Music Mode when the Music Mode Enable bit in CONTROL(02h) is set and a plug is inserted. Music Mode reduces MIC bias current by approximately 90% with the default Music Mode timing (0Bh) register value.

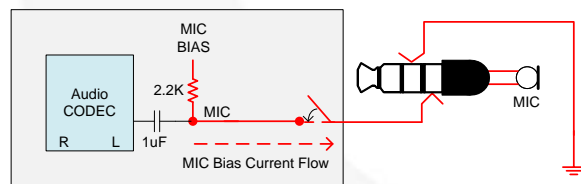


Figure 5. MIC Bias Leakage Path

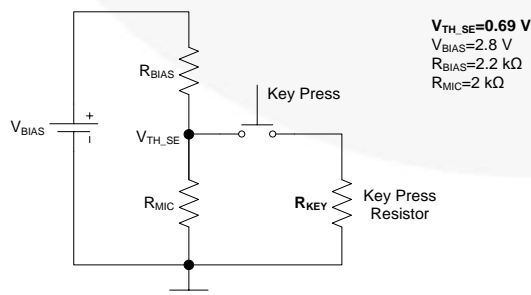


Figure 6. Example Key-Press Resistor Calculations and Values

Headset Impedance Detection Range

FSA8069 detects jack insertion and removal by monitoring impedance on the J_DET pin. The accessory types is updated in the Status (03H) register.

Table 1. Impedance Detection Range

| Accessory Type | Impedance Step | Target Range [Ω] |
|----------------------|----------------|------------------|
| Headset #1 | Step 0 | 0 to 24 |
| Headset #2 | Step 1 | 24 to 42 |
| Headset #3 | Step 2 | 42 to 100 |
| Headset #4 | Step 3 | 100 to 200 |
| Headset #5 | Step 4 | 200 to 450 |
| Headset #6 | Step 5 | 450 to 1,000 |
| Line_In/Out (CarKit) | Step 6 | 1000 to 15,000 |

LDO Operation

The integrated microphone bias LDO is set to 2.8 V. The LDO can be used to bias a microphone accessory and is enabled / disabled by the I²C register bit LDO ENABLE in the COLTROL register(02h). This LDO requires a 0.22 μF to 1 μF coupling capacitor on the output. The coupling capacitor should be placed close to the LDO pin.

Headset Key-Press Operation

The headset key-press comparator threshold is a function of the MIC bias voltage, MIC bias resistor, and the MIC impedance. All of these variables must be considered when calculating the key-press resistor value. Figure 6 is an example of how to calculate the key-press resistor value.

$$R_{KEY} \leq \frac{1}{\left(\frac{1}{V_{TH_SE}} - \frac{1}{\frac{V_{BIAS} - V_{TH_SE}}{R_{BIAS}}} \right)} - \frac{1}{R_{MIC}}$$

$$R_{KEY} \leq 1100 \Omega$$

Recommended LDO Bias Circuit and MIC Switch PCB Layout

PCB layout can degrade the audio quality and be a contributory factor in audible noise coupling issues, high-frequency noise (ESD/ EMI) issues, and signal losses. To avoid unexpected noise issues and to achieve stable regulator output, all external components should be placed as close to the FSA8069 as possible.

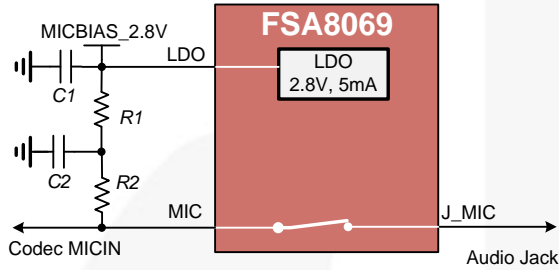


Figure 7. MIC Bias and MIC Switch Circuit

Decrease the spacing between the traces for MIC and ground signals between the audio jack to increase the inductive coupling of these signals. In effect, this creates a low-frequency band-pass filter that shunts ESD energy to ground before it reaches internal components. Where feasible, lay the MIC trace as a shielded stripline; as shown in Figure 9.

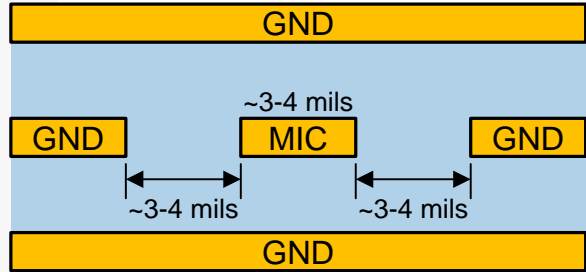


Figure 9. MIC PCB Trace as Shield Strip Line

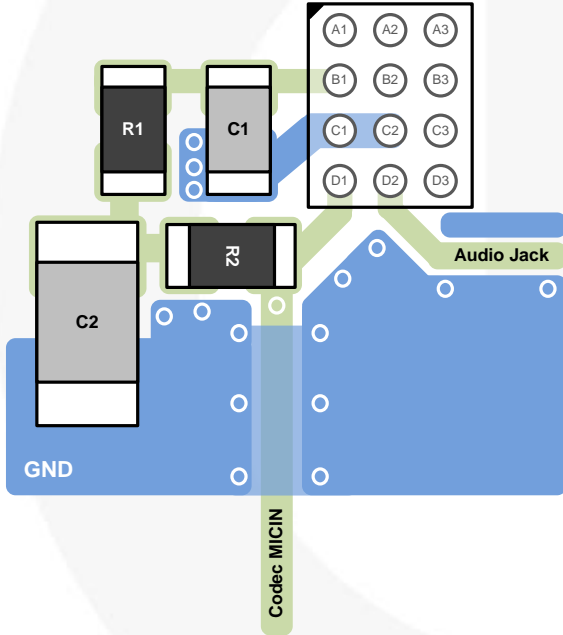


Figure 8. Recommended PCB Layout Placement

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|--------------|------|
| V_{DD}, V_{IO} | Supply Voltage from Battery | -0.5 | 6.0 | V |
| V_{SW} | Switch I/O Voltage (MIC, J_MIC) | -0.5 | $V_{DD}+0.5$ | V |
| V_{JD} | Input Voltage for J_DET Input | -1.5 | $V_{DD}+0.5$ | V |
| I_{IK} | Input Clamp Diode Current | -50 | | mA |
| I_{SW} | Switch I/O Current | | 50 | mA |
| T_{STG} | Storage Temperature Range | -65 | +150 | °C |
| T_J | Maximum Junction Temperature | | +150 | °C |
| T_L | Lead Temperature (Soldering, 10 Seconds) | | +260 | °C |
| ESD | IEC 61000-4-2 System ESD | Air Gap | 15 | kV |
| | | Contact | 8 | |
| | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | J_DET, J_MIC, V_{DD} , V_{IO} , GND | 8 | |
| | | All Other Pins | 2 | |
| Charged Device Model, JEDEC JESD22-C101 | All Pins | 1 | | |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|---|------|----------|------------|
| V_{DD} | Battery Supply Voltage | 3.0 | 4.5 | V |
| V_{IO} | Parallel I/O Supply Voltage | 1.6 | V_{DD} | V |
| V_{SW} | Switch Input Voltage (J_MIC, MIC) | 0 | 3.0 | V |
| T_A | Operating Temperature | -40 | +85 | °C |
| J_DET_{AudioV} | Audio Voltage Range on J_DET Pin | -1.4 | +1.4 | V |
| C_{OUT} | LDO Output Capacitance | 220 | | nF |
| R_{J_DET} | Resistance on Audio Accessory Left Channel to Generate Valid Attach | | 15.75 | k Ω |

DC Electrical Characteristics

All typical values are at $T_A=25^\circ\text{C}$, $C_{IN_VDD}=1.0\ \mu\text{F}$, $C_{IN_VIO}=0.1\ \mu\text{F}$, and $C_{OUT_LDO}=0.22\ \mu\text{F}$ unless otherwise specified.

| Symbol | Parameter | V_{DD} (V) | Conditions | $T_A = -40$ to $+85^\circ\text{C}$ | | | Unit |
|---|---|--------------|--|------------------------------------|------|---------------------|---------------|
| | | | | Min. | Typ. | Max. | |
| MIC Switch | | | | | | | |
| R_{ON} | MIC Switch On Resistance | 3.8 | $I_{OUT}=30\ \text{mA}$, $V_{IN}=2.2\ \text{V}$ | | 0.50 | | Ω |
| $R_{FLAT(ON)}$ | On Resistance Flatness | 3.8 | $I_{OUT}=30\ \text{mA}$, $V_{IN}=1.6\ \text{V}$ to V_{DD} | | 0.30 | 1.50 | |
| I_{OFF} | Power-Off Leakage Current Through Switch | 0 | MIC, J_MIC Ports $V_A=4.3\ \text{V}$ | | | 3 | μA |
| I_{ON} | Input Leakage Current MIC, J_MIC switch ON | 3.0 to 4.5 | Inputs V_{MIC} , $V_{MIC}=3.0\ \text{V}$, Other Side of Switch Port Floating | | | 1 | μA |
| I_{OZ} | Off Leakage Current | 4.5 | MIC and J_MIC Port $V_{IN}=3.0\ \text{V}$ | | | 1 | μA |
| Key Press | | | | | | | |
| V_{COMP} | Comparator Threshold for Key Detection | 3.0 to 4.5 | Detection Threshold (0Fh) [3:0]=1001 (790 mV) | | 0.79 | | V |
| J_DET | | | | | | | |
| $J_DET_{Tolerance}$ | Tolerance between Impedance Detection Steps (see Table 1) | 3.0 to 4.5 | Impedance Detection Mode | | 5% | | |
| Parallel I/O (KP, INTB) | | | | | | | |
| V_{OH} | Output High Voltage | | $I_{OH}=-100\ \mu\text{A}$ | $0.8 \times V_{IO}$ | | | V |
| V_{OL} | Output Low Voltage | | $I_{OL}=+100\ \mu\text{A}$ | | | $0.2 \times V_{IO}$ | |
| I²C Controller DC Characteristics Fast Mode (400 kHz) | | | | | | | |
| V_{IL} | Low-Level Input Voltage | | | | | $0.3 \times V_{IO}$ | V |
| V_{IH} | High-Level Input Voltage | | | $0.7 \times V_{IO}$ | | | V |
| V_{OL1} | Low-Level Output Voltage at 3 mA Sink Current (Open-Drain) | | $V_{IO}>2\ \text{V}$ | 0 | | 0.4 | V |
| | | | $V_{IO}<2\ \text{V}$ | | | $0.2 \times V_{IO}$ | V |
| I_{i2C} | Input Current of I2C_SDA and I2C_SCL Pins, Input Voltage 0.26 V to 2.34 V | | | -10 | | +10 | μA |
| Current | | | | | | | |
| I_{DD_SLNA} | Battery Supply Sleep Mode Current with No Accessory Attached and LDO Disabled | 3.0 to 4.5 | Static Current during Sleep Mode | | 1.5 | | μA |
| I_{DD_SLWA} | Battery Supply Sleep Mode Current with Accessory Attached | 3.0 to 4.5 | Active Current | | 30 | | μA |
| I_{DD_LDO} | LDO Quiescent Current | 3.0 to 4.5 | $I_{LOAD}=0\ \text{mA}$, $C_{OUT}=0\ \text{pF}$, LDO Enabled | | 100 | | μA |
| LDO | | | | | | | |
| V_{OUT} | Output Voltage (Output=2.8 V) | 3.0 to 4.5 | $I_{LOAD}=1\ \text{mA}$ | 2.77 | 2.80 | 2.83 | V |
| I_{OUT} | Maximum Output Current | 3.0 to 4.5 | | 5 | | | mA |

AC Electrical Characteristics

All typical values are for $V_{CC}=3.3\text{ V}$ at $T_A=25^\circ\text{C}$, $C_{IN_VDD}=1.0\ \mu\text{F}$, $C_{IN_VIO}=0.1\ \mu\text{F}$, and $C_{OUT_LDO}=0.22\ \mu\text{F}$ unless otherwise specified. Not production tested.

| Symbol | Parameter | V_{DD} (V) | Conditions | Typical | Unit |
|-------------------------------|--|--------------|---|------------------|---------------|
| MIC Switch | | | | | |
| THD | Total Harmonic Distortion | 3.0 | $R_T=600\ \Omega$, $f=20\ \text{Hz to } 20\ \text{kHz}$, $V_{IN}=2.0\ \text{V} + 0.5\ V_{pp}$ Sine | 0.01 | % |
| OIRR | Off Isolation | 3.0 | $f=20\ \text{kHz}$, $R_S=600\ \Omega$, $C_L=0\ \text{pF}$, $R_T=600\ \Omega$ | -85 | dB |
| PSRR _{sw} | Power Supply Rejection Ratio (at 217 Hz) | 4.0 | Power Supply Noise 300 mV _{PP} , 87.5% Duty Cycle, | -80 | dB |
| Timing Characteristics | | | | | |
| t_{POLL} | ON Time of MIC Switch for Sensing SEND / END Key Press Oscillator Stable Time | 3.0 to 4.5 | I ² C Register Adjustable ($t_{POLL}[3:0]$) | 15 (Default) | ms |
| t_{WAIT} | Period of MIC Switching for Sensing SEND / END Key Press | 3.0 to 4.5 | I ² C Register Adjustable ($t_{WAIT}[3:0]$) | 150 (Default) | ms |
| t_{DET_IN} | Debounce Time after J_DET Changes State from HIGH to LOW | 3.0 to 4.5 | I ² C Register Adjustable ($t_{DET_IN}[3:0]$) | 25 (Default) | ms |
| $t_{MIC_SW_OPEN}$ | Time of MIC Switch Open after J_DET Changes State from LOW to HIGH | 3.0 to 4.5 | | 30 | μs |
| t_{KBK} | Debounce Time for Sensing SEND / END Key Press / Release | 3.0 to 4.5 | I ² C Register Adjustable ($t_{KBK}[3:0]$) | 30 (Default) | ms |
| t_{DET_REM} | Debounce Time from Changing J_DET State from LOW to HIGH to Detect Jack Removal | 3.0 to 4.5 | I ² C Register Adjustable ($t_{DET_REM}[3:0]$) | 1 (Default) | ms |
| t_{EXTRA} | Additional Time to Keep Switch Closed in Music Mode after Key Release | 3.0 to 4.5 | | 600 | ms |
| t_{REG_DFT} | Time to Set Registers to Defaults from Falling and Rising V_{IO} | 3.0 to 4.5 | | 1 | ms |
| LDO | | | | | |
| PSRR _{LDO} | Power Supply Rejection Ratio (at 217 Hz) | 4.5 | Power Supply Noise 300 mV _{PP} , 87.5% Duty Cycle, $C_{OUT}=1\ \mu\text{F}$ | -80 | dB |

I²C Specifications

| Symbol | Parameter | Fast Mode | | |
|---------------------|---|----------------------|------|------|
| | | Min. | Max. | Unit |
| f _{SCL} | I2C_SCL Clock Frequency | 0 | 400 | kHz |
| t _{HD;STA} | Hold Time (Repeated) START Condition | 0.6 | | μs |
| t _{LOW} | Low Period of I2C_SCL Clock | 1.3 | | μs |
| t _{HIGH} | High Period of I2C_SCL Clock | 0.6 | | μs |
| t _{SU;STA} | Set-up Time for Repeated START Condition | 0.6 | | μs |
| t _{HD;DAT} | Data Hold Time | 0 | 0.9 | μs |
| t _{SU;DAT} | Data Set-up Time ⁽⁶⁾ | 100 | | ns |
| t _r | Rise Time of I2C_SDA and I2C_SCL Signals ⁽⁶⁾ | 20+0.1C _b | 300 | ns |
| t _f | Fall Time of I2C_SDA and I2C_SCL Signals ⁽⁶⁾ | 20+0.1C _b | 300 | ns |
| t _{SU;STO} | Set-up Time for STOP Condition | 0.6 | | μs |
| t _{BUF} | Bus-Free Time between STOP and START Conditions | 1.3 | | μs |
| t _{SP} | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0 | 50 | ns |

Notes:

- A Fast-Mode I²C-Bus® device can be used in a Standard-Mode I²C-Bus system, but the requirement t_{SU;DAT} ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line t_{r,max} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard Mode I²C-Bus specification) before the I2C_SCL line is released.
- C_b equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

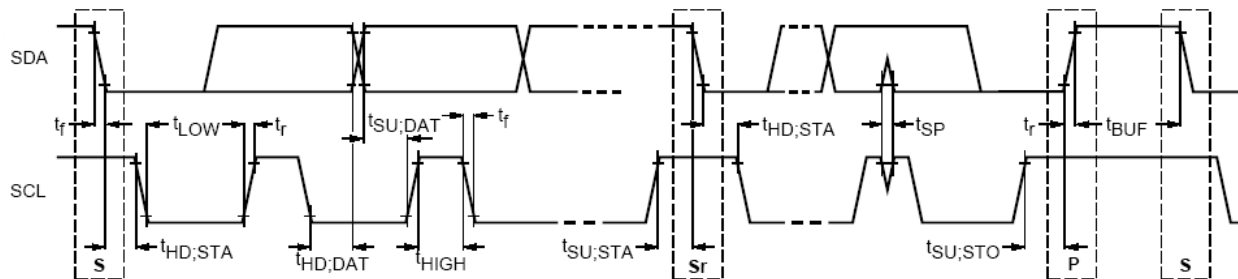


Figure 10. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Table 2. I²C Slave Address

| Name | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------|-------|-------|-------|-------|-------|-------|-------|------------|
| Slave Address | 8 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Read/Write |

Register Map

| Addr. | Register | Type | Reset Values | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|----------------------|------|--------------|---------------------------------------|----------|-----------|-----------|---|--|----------------------------------|---------------------|
| 01H | Device ID | R | 0000XXXX | Version ID | | | | Reserved* | | | |
| 02H | Control | R/W | XXXX0010 | Reserved | Reserved | Reserved | Reserved | LDO Enable | Key Detection Enable | Reserved for Future Applications | Music Mode Enable |
| 03H | Status | R | XXXX0000 | Reserved | Reserved | Reserved | Reserved | Impedance Attached Status | Impedance status [2:0] 000: Impedance Type 0 (16 Ω) 001: Impedance Type 1 (32 Ω) 010: Impedance Type 2 (64 Ω) 011: Impedance Type 3 (150 Ω) 100: Impedance Type 4 (300 Ω) 101: Impedance Type 5 (600 Ω) 110: Impedance Type 6 (2 kΩ) 111: Moisture Detection | | |
| 04H | Interrupt 1 | R/C | XXXXX000 | Reserved | Reserved | Reserved | Reserved | Reserved | Moisture Change | Plug removal | Plug insertion |
| 05H | Interrupt 2 | R/C | XX000000 | Reserved | Reserved | Reserved | Reserved | Key Release | Reserved | Reserved | Key Press |
| 07H | Interrupt Mask 1 | R/W | XXXXX000 | Reserved | Reserved | Reserved* | Reserved* | Reserved* | Moisture Change Mask | Plug Removal Mask | Plug Insertion Mask |
| 08H | Interrupt Mask 2 | R/W | XX000000 | Reserved | Reserved | Reserved | Reserved | Key Release Mask | Reserved | Reserved | Key Press Mask |
| 0AH | J_DET Timing | R/W | 00001001 | Insert (t_{DET-IN}) | | | | Removal ($t_{DET-REM}$) | | | |
| 0BH | Music Mode Timing | R/W | 00101000 | Key-Press Polling Time (t_{POLL}) | | | | Key-Press Waiting Time (t_{WAIT}) | | | |
| 0CH | Key Debounce Timing | R/W | XXXX0101 | Reserved | Reserved | Reserved | Reserved | Key-Press Debounce Timing (t_{KBR}) | | | |
| 0EH | Reserved | R/W | XXXX1000 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 0FH | Detection Thresholds | R/W | 10011000 | Key Threshold [3:0] | | | | Reserved | Reserved | Reserved | Reserved |
| 10H | Reset | R/W | XXXXXXXX0 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reset |

Notes:

8. Do not use registers that are blank and reserved.
9. Write "0" to undefined register bits.
10. Values read from undefined register bits are not defined and are invalid.



Register Definition

Table 3. Address: 01H

Type: Read

| DEVICE ID | | | Default | xxxx0000 |
|-----------|------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 3:0 | Reserved | 4 | Do Not Use | |
| 7:4 | Version ID | 4 | 0000 = Version 0.0 0001 = Version 0.1 | |

Table 4. Address: 02H

Type: Read/Write

| CONTROL | | | Default | xxxx0010 |
|---------|----------------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 0 | Music Mode Enable | 1 | 0: Music Mode disabled (MIC switch keep closed or opened) 1: Music Mode enabled (MIC switch repeats open and close if plug inserted completely) | |
| 1 | Reserved | 1 | Do Not Use Reserved for future applications, default = 1 | |
| 2 | Key Detection Enable | 1 | 0: Key detection disabled (Default) 1: Key detection enabled | |
| 3 | LDO Enable | 1 | 0: LDO disabled (Default) 1: LDO enabled | |
| 7:4 | Reserved | 4 | Do Not Use | |

Table 5. Address: 03H

Type: Read

| STATUS | | | Default | xxxx0000 |
|--------|------------------------------|------|--|----------|
| Bit # | Name | Size | Function | |
| 2:0 | Impedance Status | 3 | Only valid at Impedance Accessory Attached bit set 000 : Impedance Type 0 (16 Ω) (Default) 001: Impedance Type 1 (32 Ω) 010: Impedance Type 2 (64 Ω) 011: Impedance Type 3 (150 Ω) 100: Impedance Type 4 (300 Ω) 101: Impedance Type 5 (600 Ω) 110: Impedance Type 6 (2k Ω) 111: Moisture detected | |
| 3 | Impedance Accessory Attached | 1 | 0: Accessory not attached (Default) 1: Accessory attached and Impedance Status[2:0] valid | |
| 7:4 | Reserved | 4 | Do Not Use | |

Table 6. Address: 04H Type: Read/Clear

| INTERRUPT 1 | | | Default | xx000000 |
|-------------|-----------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 0 | Plug Insertion | 1 | 0: Plug Insertion not detected (Default) 1: Plug Insertion detected | |
| 1 | Plug Removal | 1 | 0: Plug removal not detected (Default) 1: Plug removal detected | |
| 2 | Moisture Change | 1 | 0: Moisture status not changed (Default) 1: Moisture status changed | |
| 7:4 | Reserved | 4 | Do Not Use | |

Table 7. Address: 05H Type: Read/Clear

| INTERRUPT 2 | | | Default | xxxx0xx0 |
|-------------|-------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 0 | Key Press | 1 | 0: Key not pressed (Default) 1: Key pressed | |
| 2:1 | Reserved | 2 | Do Not Use | |
| 3 | Key Release | 1 | 0: Key not released (Default) 1: Key released | |
| 7:4 | Reserved | 4 | Do Not Use | |

Table 8. Address: 07H Type: Read/Write

| ITERRUPT MASK1 | | | Default | xxxxx000 |
|----------------|----------------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 0 | Plug Insertion Mask | 1 | 0: Plug insert detection not masked (Default) 1: Plug insert detection masked | |
| 1 | Plug Removal Mask | 1 | 0: Plug removal detection not masked (Default) 1: Plug removal detect masked | |
| 2 | Moisture Change Mask | 1 | 0: Moisture change not masked (Default) 1: Moisture change masked | |
| 7:3 | Reserved | 5 | Do Not Use | |

Table 9. Address: 08H Type: Read/Write

| INTERRUPT MASK 2 | | | Default | xxxx0xx0 |
|------------------|------------------|------|---|----------|
| Bit # | Name | Size | Function | |
| 0 | Key Press Mask | 1 | 0: Key press not masked (Default) 1: Key press masked | |
| 2:1 | Reserved | 2 | Do Not Use | |
| 3 | Key Release Mask | 1 | 0: Key release not masked (Default) 1: Key release masked | |
| 7:4 | Reserved | 4 | Do Not Use | |

Table 10. Address: 0AH Type: Read/Write

| J_DET TIMING | | | Default | 00001001 |
|--------------|---|------|--|----------|
| Bit # | Name | Size | Function | |
| 3:0 | t_{DET_REM}[3:0] Plug Removal Debounce Timing | 4 | 0000: 100 μs 0001: 200 μs 0010: 300 μs 0011: 400 μs 0100: 500 μs 0101: 600 μs 0110: 700 μs 0111: 800 μs 1000: 900 μs 1001: 1000 μs 1010: 1200 μs 1011: 1400 μs 1100: 1600 μs 1101: 1800 μs 1110: 2000 μs 1111: 5000 μs | |
| 7:4 | t_{DET_IN}[3:0] Plug Insertion Debounce Time | 4 | 0000: 25 ms 0001: 50 ms 0010: 75 ms 0011: 100 ms 0100: 125 ms 0101: 150 ms 0110: 175 ms 0111: 200 ms 1000: 225ms 1001: 250 ms 1010: 275 ms 1011: 300 ms 1100: 325 ms 1101: 350 ms 1110: 375 ms 1111: 400 ms | |

Table 11. Address: 0BH Type: Read/Write

| MUSIC MODE TIMING | | | Default | 00101000 |
|-------------------|---|------|---|----------|
| Bit # | Name | Size | Function | |
| 3:0 | t_{WAIT}[3:0] Key Press Waiting Time in Music Mode | 4 | 0000: 5 ms 0001: 10 ms 0010: 15 ms 0011: 20 ms 0100: 25 ms 0101: 30 ms 0110: 50 ms 0111: 100 ms 1000: 150 ms (Default) 1001: 200 ms 1010: 250 ms | |

| MUSIC MODE TIMING | | | Default | 00101000 |
|-------------------|--|------|--|----------|
| Bit # | Name | Size | Function | |
| | | | 1011: 300 ms 1100: 350 ms 1101: 400 ms 1110: 450 ms 1111: 500 ms | |
| 7:4 | t_{POLL}[3:0] Key Press Polling Time in Music Mode | 4 | 0000: 5 ms 0001: 10 ms 0010: 15 ms (Default) 0011: 20 ms 0100: 25 ms 0101: 30 ms 0110: 35 ms 0111: 40 ms 1000: 45 ms 1001: 50 ms 1010: 60 ms 1011: 70 ms 1100: 80 ms 1101: 90 ms 1110: 100 ms 1111: 150 ms | |

Table 12. Address: 0CH

Type: Read/Write

| MIC DEBOUNCE TIME | | | Default | xxxx0101 |
|-------------------|---|------|--|----------|
| Bit # | Name | Size | Function | |
| 3:0 | t_{KBK}[3:0] Key Press/ Release Debounce Timing | 4 | 0000: 5 ms 0001: 10 ms 0010: 15 ms 0011: 20 ms 0100: 25 ms 0101: 30 ms (Default) 0110: 35 ms 0111: 40 ms 1000: 45 ms 1001: 50 ms 1010: 55 ms 1011: 60 ms 1100: 65 ms 1101: 70 ms 1110: 75 ms 1111: 80 ms | |
| 7:4 | Reserved | 5 | Do Not Use | |

Table 13. Address: 0FH Type: Read/Write

| DETECTION THRESHOLD | | | Default | 1001xxxx |
|---------------------|--|------|---|----------|
| Bit # | Name | Size | Function | |
| 3:0 | Reserved | 4 | Do Not Use | |
| 7:4 | <p style="text-align: center;">Key [3:0]</p> <p style="text-align: center;">Key Threshold</p> | 4 | 0000: 660 mV 0001: 680 mV 0010: 700 mV 0011: 710 mV 0100: 730 mV 0101: 750 mV 0110: 760 mV 0111: 770 mV 1000: 780 mV 1001: 790 mV (Default) 1010: 800 mV 1011: 810 mV 1100: 830 mV 1101: 850 mV 1110: 870 mV 1111: 890 mV | |

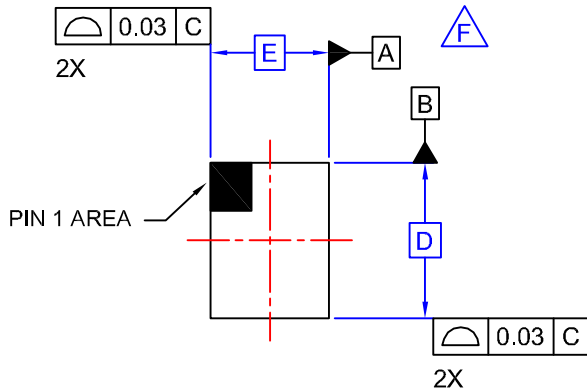
Table 14. Address: 10H Type: Read/Write

| RESET | | | Default | xxxxxxx0 |
|-------|--|------|--|----------|
| Bit # | Name | Size | Function | |
| 0 | <p style="text-align: center;">Reset</p> <p>After reset, this bit is automatically cleared to '0'</p> | 4 | 0: No Change 1: Reset Device – Reset all I ² C register to default values. | |
| 7:1 | Reserved | 7 | Do Not Use | |

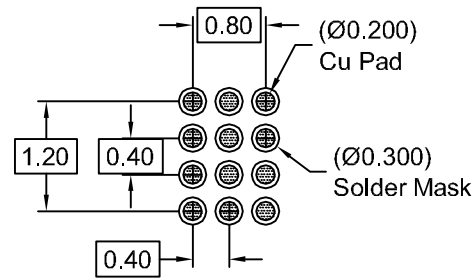
Package Specific Dimensions

| D | E | X | Y |
|----------|----------|-----------|-----------|
| 1.615 mm | 1.415 mm | 0.3075 mm | 0.2075 mm |

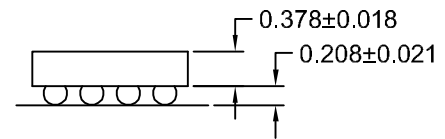
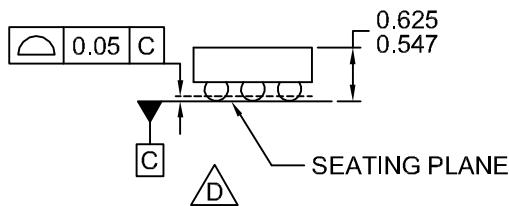
| REVISIONS | | | |
|-----------|--------------------------|---------|-------------------|
| REV | DESCRIPTION | DATE | APP'D / SITE |
| 1 | Initial drawing release. | 8-19-09 | L. England / FSME |



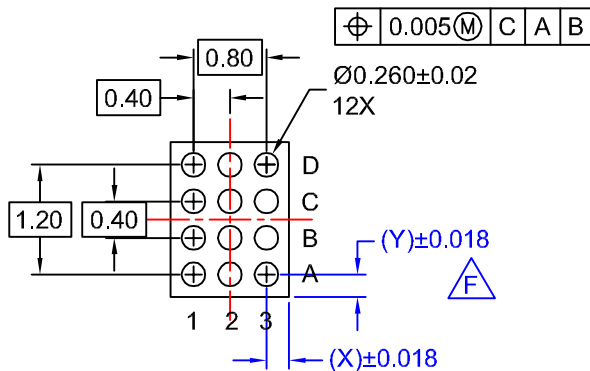
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC012ACrev1.

| APPROVALS | | DATE | FAIRCHILD SEMICONDUCTOR™ | | | |
|------------|------------|---------|--|------|----------------|-----|
| DRAWN | L. England | 8-19-09 | 12BALL WLCSP, 3X4 ARRAY 0.4MM PITCH, 250UM BALL | | | |
| DFTG. CHK. | S. Martin | 8-19-09 | | | | |
| ENGR. CHK. | | | | | | |
| | | | | | | |
| | | | SCALE | SIZE | DRAWING NUMBER | REV |
| | | | N/A | N/A | MKT-UC012AC | 1 |
| | | | DO NOT SCALE DRAWING | | SHEET 1 of 1 | |

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