FDB1D7N10CL7

N-Channel Shielded Gate POWERTRENCH® MOSFET

100 V, 268 A, 1.7 mΩ

Description

This N−Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Max $R_{DS(on)}$ = 1.75 mΩ at V_{GS} = 10 V, I_D = 100 A
- Max $R_{DS(on)}$ = 1.7 mΩ at V_{GS} = 12 V, I_D = 100 A
- Max $R_{DS(on)}$ = 1.65 mΩ at V_{GS} = 15 V, I_D = 100 A
- Max $R_{DS(on)}$ = 4.4 mΩ at V_{GS} = 6 V, I_D = 63 A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated Tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C) (Note 5)	268	A
	Continuous (T_C = 100°C) (Note 5)	190	
	Pulsed (Note 4)	1390	
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	595	mJ
P_D	Power Dissipation T_C = 25°C	250	W
	T_A = 25°C (Note 1a)	3.8	
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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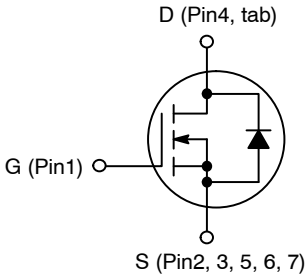
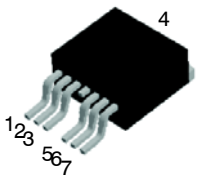
V_{DS}	I_D MAX	$r_{DS(on)}$ MAX
100 V	268 A	1.7 mΩ



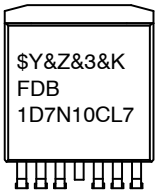
N−Channel MOSFET



1. Gate
2. Source
3. Source
4. Drain
5. Source
6. Source
7. Source

D2PAK7 (TO−263 7 LD)
CASE 418AY

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDB1D7N10CL7	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	57	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 700 μA	2.0	3.1	4.0	V
$V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 700 μA, referenced to 25°C	–	–9	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 100 A	–	1.5	1.75	mΩ
		V_{GS} = 12 V, I_D = 100 A	–	1.4	1.7	
		V_{GS} = 15 V, I_D = 100 A	–	1.33	1.65	
		V_{GS} = 6 V, I_D = 63 A	–	2.2	4.4	
		V_{GS} = 10 V, I_D = 100 A, T_J= 150°C	–	2.65	3.1	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 100 A	–	237	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	8285	11600	pF
C_{oss}	Output Capacitance		–	5025	7035	pF
C_{rss}	Reverse Transfer Capacitance		–	50	80	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 100 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	39	63	ns
t_r	Rise Time		–	33	53	ns
$t_{d(off)}$	Turn−Off Delay Time		–	85	136	ns
t_f	Fall Time		–	36	58	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 100 A	–	116	163	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V; V_{DD} = 50 V, I_D = 100 A	–	74	104	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 100 A	–	37	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 100 A	–	24	–	nC
Q_{oss}	Output Charge	V_{DD} = 50 V, V_{GS} = 0 V	–	333	–	nC
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Continuous Drain to Source Diode Forward Current		–	–	268	A
I_{SM}	Pulsed Drain to Source Diode Forward Current		–	–	1390	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 100 A (Note 2)	–	0.9	1.2	V

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SOURCE-DRAIN DIODE CHARACTERISTICS						
t_{rr}	Reverse Recovery Time	I_F = 50 A, di/dt = 300 A/μs	–	63	101	ns
Q_{rr}	Reverse Recovery Charge		–	186	298	nC
t_{rr}	Reverse Recovery Time	I_F = 50 A, di/dt = 1000 A/μs	–	82	132	ns
Q_{rr}	Reverse Recovery Charge		–	869	1390	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
   a) 40°C/W when mounted on a 1 in2 pad of 2 oz copper.
   b) 62.5°C/W when mounted on a minimum pad of 2 oz copper.
2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 595 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 63 A, V_{DD} = 90 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 91 A.
4. Pulsed Id please refer to Figure "Forward Bias Safe Operating Area" for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB1D7N10CL7	FDB1D7N10CL7	D2−PAK−7L	330 mm	24 mm	800 Units

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

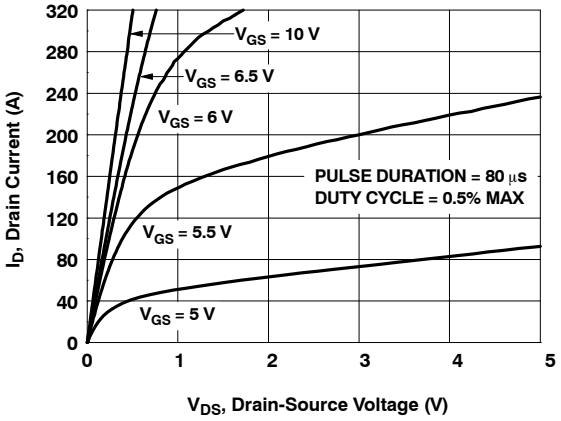


Figure 1. On-Region Characteristics

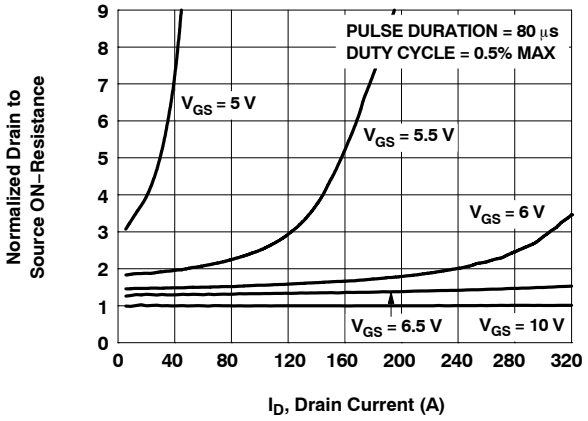


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

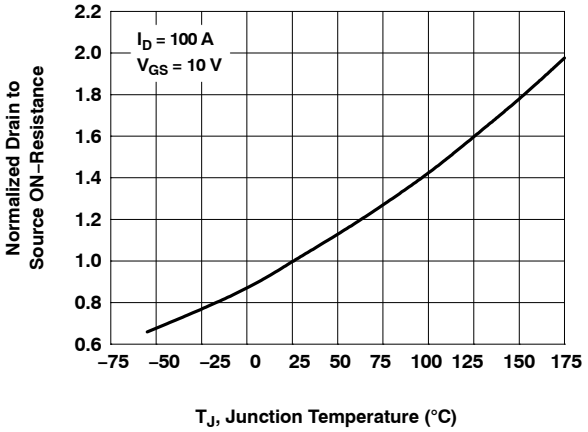


Figure 3. Normalized On−Resistance vs. Junction Temperature

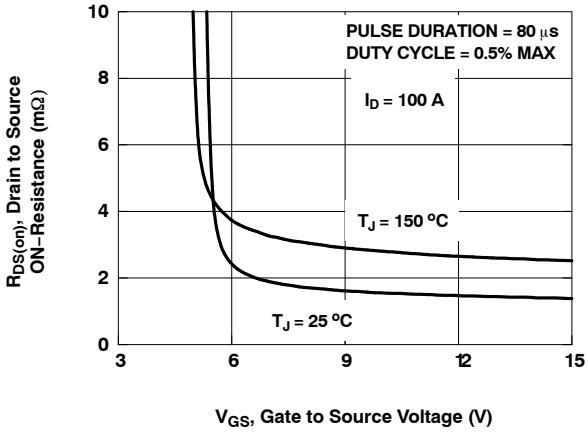


Figure 4. On−Resistance vs. Gate to Source Voltage

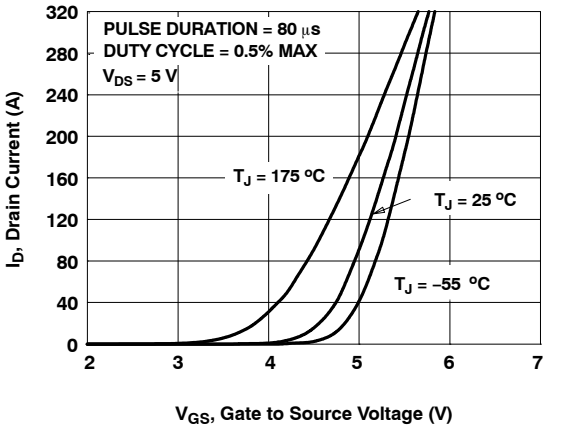


Figure 5. Transfer Characteristics

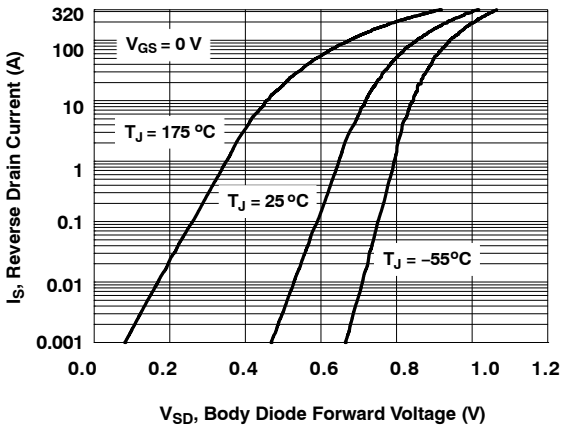


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Continued)

(T_J = 25°C unless otherwise noted)

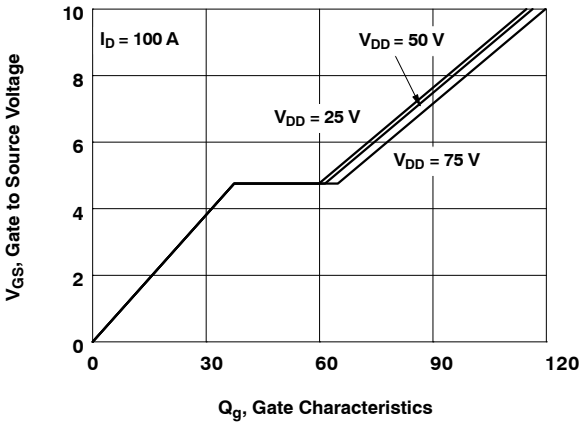


Figure 7. Gate Charge Characteristics

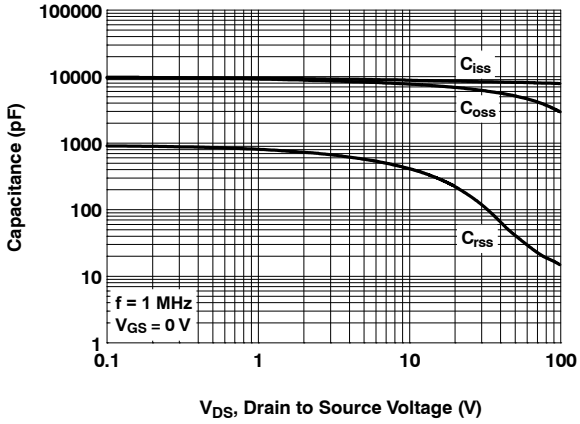


Figure 8. Capacitance vs. Drain to Source Voltage

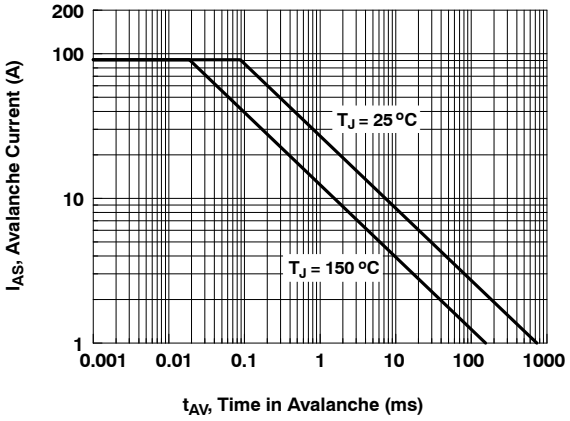


Figure 9. Unclamped Inductive Switching Capability

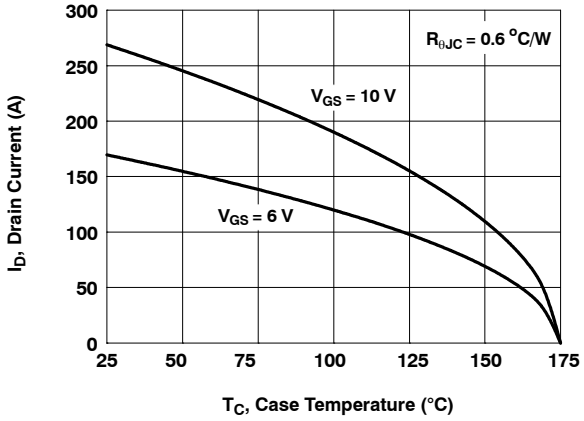


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

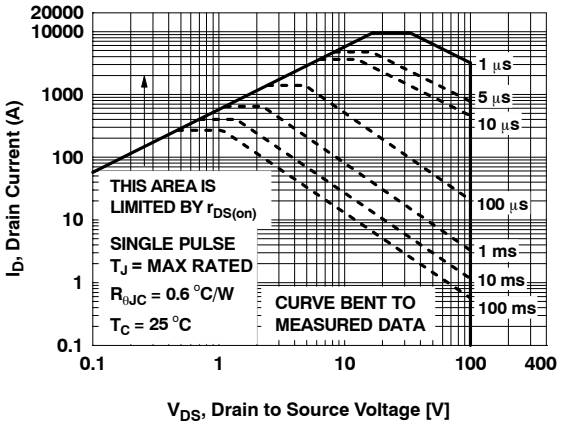


Figure 11. Forward Bias Safe Operating Area

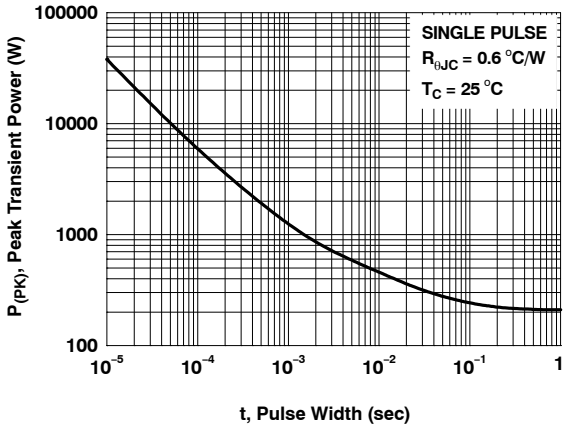


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Continued)

(T_J = 25°C unless otherwise noted)

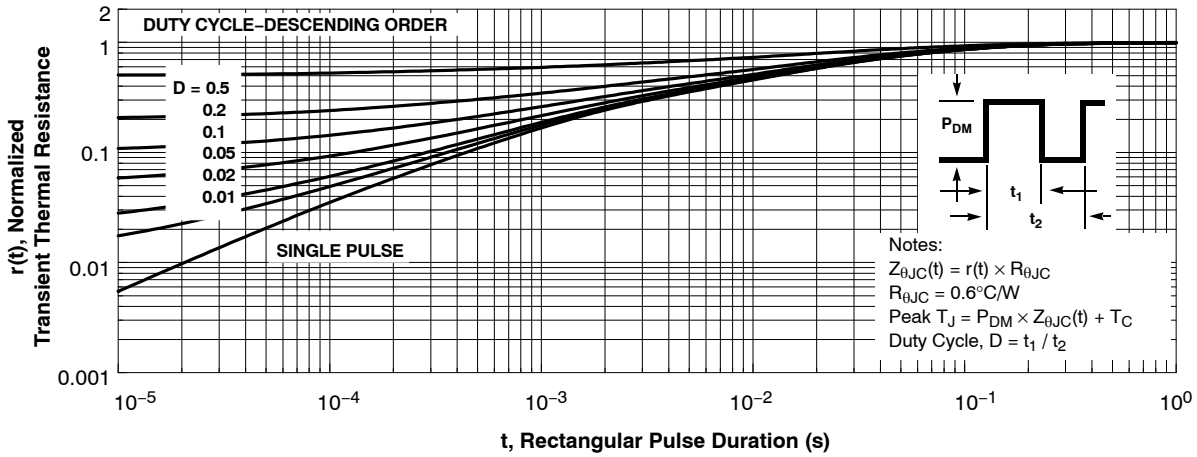


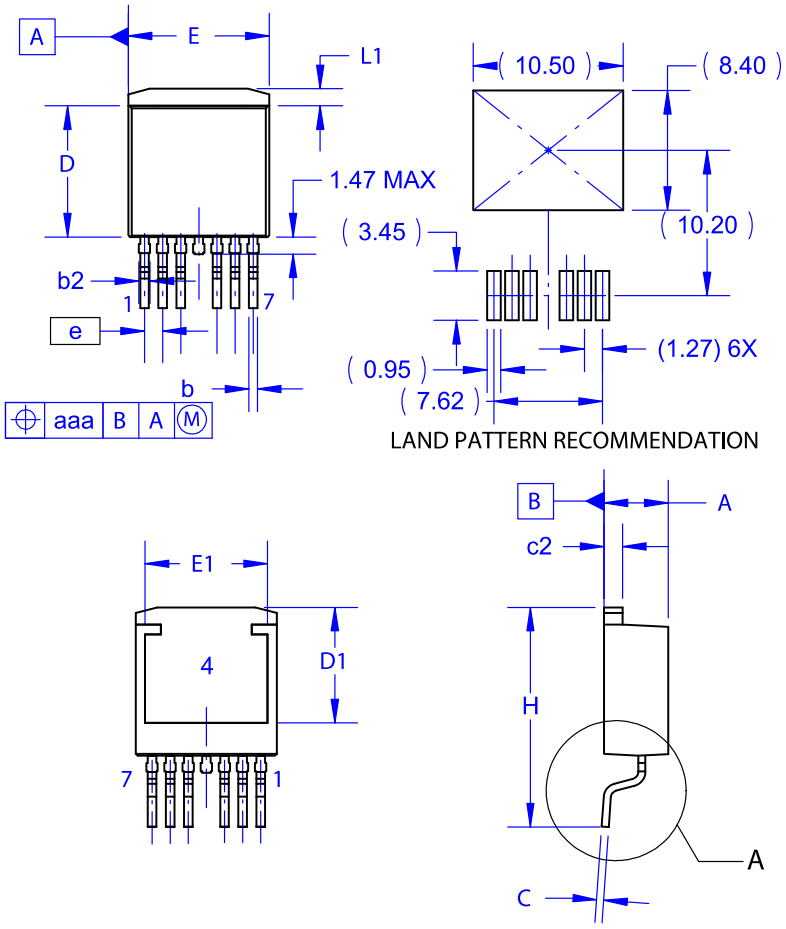
Figure 13. Normalized Max Junction to Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

D2PAK7 (TO−263 7 LD)
CASE 418AY
ISSUE C

DATE 15 JUL 2019



NOTES:

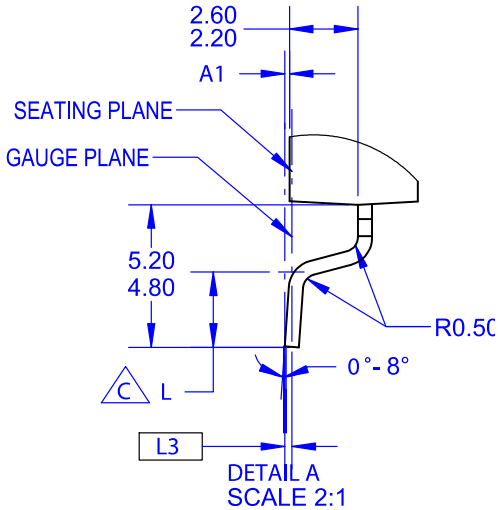
A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
F. LAND PATTERN RECOMMENDATION PER IPC. TO127P1524X465-8N.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.70	0.80	0.90
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.70	~	~
E	9.70	9.90	10.20
E1	8.38	8.58	8.78
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**D2PAK7 (TO−263 7 LD)**	**PAGE 1 OF 1**

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