Application Note 90
Using the Multiplex Bus RTC Extended Features

www.dalsemi.com

DESCRIPTION

This application note discusses the extended features for the following Real Time Clocks (RTCs): DS1685/87, DS1688/91, DS1689/93, DS17285/87, DS17485/87 and DS17885/87. Also included is an initialization flow chart. All of these devices incorporate these extended features unless otherwise noted.

EXTENDED FEATURES

AUXILIARY BATTERY INPUT (V_{BAUX})

The auxiliary battery input, V_{BAUX}, provides the power required to use the and the 32 kHz square wave in the absence of system power. The timekeeping and RAM data can also be maintained by this power source. The ABE bit, Bit 7 in control register 48h must be set to a logic 1, to enable V_{BAUX} to power the 32 kHz square wave and kickstart input in the absence of $V_{CC.}$ If this input is not going to be used then ABE must be set to a logic 0 and the V_{BAUX} input tied to ground.

KICKSTART INPUT ($\overline{KS}$)

The kickstart pin is intended to be used in the battery-backed mode in conjunction with the $\overline{PWR}$ signal providing systems with power management control. A signal providing a ground closure will force the $\overline{PWR}$ signal to transition low. The $\overline{KS}$ pin can also be used as an interrupt input while V_{CC} is applied.

POWER–ON OUTPUT ($\overline{PWR}$)

This output is open drain and requires an external pull–up resistor for proper operation. This signal is intended to be used in conjunction with $\overline{KS}$ and the wakeup alarm for power management features.

32 KHz SQUARE WAVE OUTPUT (SQW)

The SQW output pin can provide a 32 kHz square waves for power management purposes. The DS1685/87, DS1688/91, DS17285/87, DS17485/87, and DS17885/87 will provide the 32 kHz each time the system power, V_{CC}, is applied. The DS1689/93 must be programmed to output the 32 kHz after the system power is applied.

SILICON SERIAL NUMBER

A unique 64–bit silicon serial number is located in bank 1 registers 40h – 47h. The serial number is divided into three separate parts. The first byte, location 40h, contains a model number to identify the device type and revision. The following is a list of the model numbers currently assigned for the devices mentioned above:

Model #	Part #
71h	DS1685/87
72h	DS17285/87
73h	DS1688/91
73h	DS1689/93
74h	DS17485/87
78h	DS17885/87

The second part of the serial number is a unique 48–bit binary number located in registers 41h – 46h. The third part of the serial number is located in register 47h and contains a CRC number used to validate the data in registers 40h – 46h. This 8-byte serial number is read only.

CENTURY BYTE

The century byte, located in bank 1 register 48h, will update every 100 years keeping track of the century.

DATE ALARM BYTE

The date alarm byte, located in bank 1 register 49h, can be used in conjunction with the time of day alarm providing a system with a wakeup alarm programmable to any day within a month.

CONTROL REGISTERS 4 Ah and 4 Bh

See the Register Description section.

EXTENDED RAM SOFTWARE PORT

The extended user RAM can be accessed through software via three internal registers located in bank 1 locations 50h, 51h, and 53h. Locations 50h and 51h are used for the RAM address and location 53h is used for the data transfer. This unique feature eliminates the need for external hardware and at the same time provides the ability to switch RAM densities without any hardware modification required. This feature is not available on the DS1688/91 or DS1689/93.

V_{CC} ELAPSED TIME COUNTER

A 32–bit V_{CC} powered elapsed time counter, located in bank 1 registers 54h (LSB) through 57h (MSB), will keep track of how long system power has been applied. This counter will update once per second as long as V_{CC} is within nominal limits and the oscillator and countdown chain are enabled. When V_{CC} falls outside of the nominal limits the counter is halted and the elapsed time is retained. This counter can be read or written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

V_{BAT} ELAPSED TIME COUNTER

A 32–bit V_{BAT} powered elapsed time counter, located in bank 1 registers 58h (LSB) through 5 Bh (MSB) will keep track of how long the system has been in service. This counter will run continuously and update once per second as long as V_{BAT} or V_{BAUX} is within nominal limits and the oscillator and countdown chain are enabled. This counter can be read or written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

POWER CYCLE COUNTER

A 16–bit power cycle counter, located in bank 1 registers 5 Ch (LSB) and 5 Dh (MSB), will keep track of the number of times a system is powered on and off. Each time system power, V_{CC}, is applied within nominal limits, the counter will be incremented by one. This counter can be read and written at the user's discretion. This feature is available only on the DS1688/91 and DS1689/93.

ADDITIONAL SERIAL NUMBER

An additional 64–bit customer specific serial number or ROM is located in bank 1 registers 60h through 67h. This feature is available only on the DS1688/91 and DS1689/93.

BURST MODE

The DS17285/87, DS17485/87, and DS17885/87 are the only devices which provide the burst mode option. The model byte uniquely identifies these devices as having burst mode.

REGISTER DESCRIPTION

LOCATION	DESCRIPTION
0 Ah	Control Register A Bit 7 Update In Progress (UIP) – (read only) 0=time/date can be read 1=update in progress Bits 6 – 4 Oscillator Control (DV2-DV0) DV2=countdown chain 0=countdown chain enabled 1=resets countdown chain only if DV1=1 DV1=oscillator enable 0=oscillator off 1=oscillator on DV0=bank select 0=original bank 1=extended registers Bits 3 – 0 Rate Selection (RS3-RS0) These bits define the square wave output frequency and the periodic interrupt rate.

LOCATION	DESCRIPTION
0 Bh	Control Register B Bit 7 Halt Clock Updates (SET) 0=updates time/date once per second 1=time/date updates are inhibited Bit 6 Periodic Interrupt Enable (PIE) 0=disabled 1=enabled Bit 5 Alarm Interrupt Enable (AIE) 0=disabled 1=enabled Bit 4 Update-Ended Interrupt Enable (UIE) 0=disabled 1=enabled Bit 3 Square Wave Enable (SQWE) 0=disabled 1=enabled Bit 2 Time and Date Data Mode (DM) 0=binary coded decimal (BDC) format 1=binary format Bit 1 Hour Format (24/12) 0=12 hour mode 1= 24 hour mode Bit 0 Daylight Savings Time Enable (DSE) 0=disabled 1=enabled
0 Ch	Status Register C (read only) Bit 7 Interrupt Request Flag (IRQF) – (read only) Bit 6 Periodic Interrupt (PF) – (read only) Bit 5 Alarm Interrupt Flag (AG) – (read only) Bit 4 Update-Ended Interrupt Flag (UF) – (read only) Bit 3 – 0 Reserved (read only logic 0)

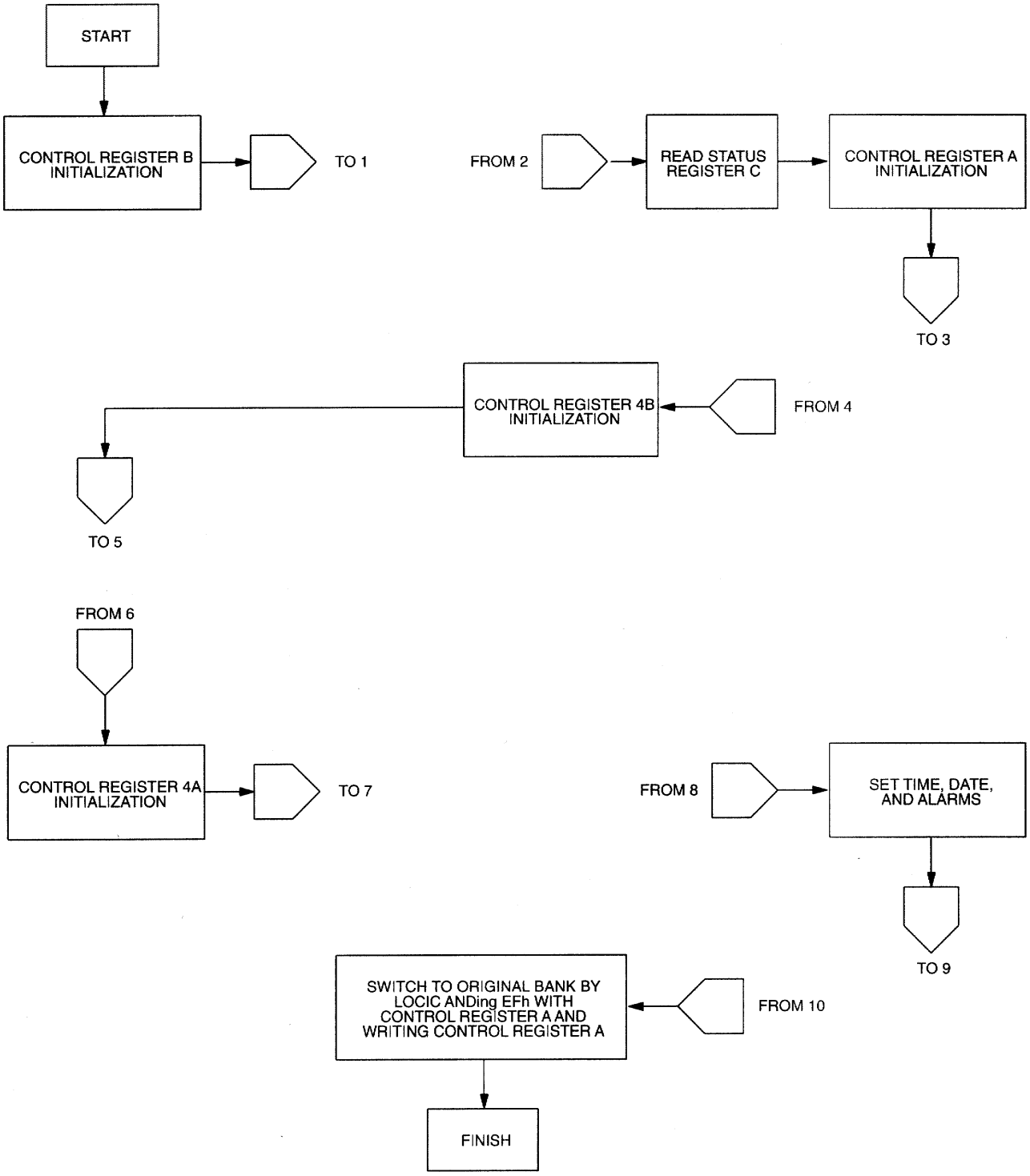
LOCATION	DESCRIPTION
0 Dh	Status Register D (read only) Bit 7 Valid RAM and Time (VRT) – (read only) 0=battery low; CMOS RAM invalid 1=battery good; CMOS RAM valid Bit 6 – 0 Reserved (read only logic 0)
04 Ah	Extended Control Register 4A Bit 7 Valid RAM and Time 2 (VRT2) – (read only) 0=auxiliary battery is low 1=auxiliary battery is good Bit 6 Increment in Progress (INCR) – (read only) 0=time/date has been updated 1=time/date is incrementing and checking alarms Bit 5 Burst Mode Enable (BME) – See Note 1 0=single-byte extended RAM reads and writes 1=auto-increments address for extended RAM reads and writes Bit 4 Reserved Bit 3 Power Active Bar (PAB) 0= $\overline{\text{PWR}}$ pin is in the active low state 1= $\overline{\text{PWR}}$ pin is in the inactive high state Bit 2 RAM Clear Flag (RF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{RCLR}}$ if RCE=1 Bit 1 Wakeup Alarm Flag (WF) 0=cleared state (must be written) 1=wakeup alarm condition has occurred Bit 0 Kickstart Flag (KF) 0=cleared state (must be written) 1=high to low transition detected on $\overline{\text{KS}}$ input

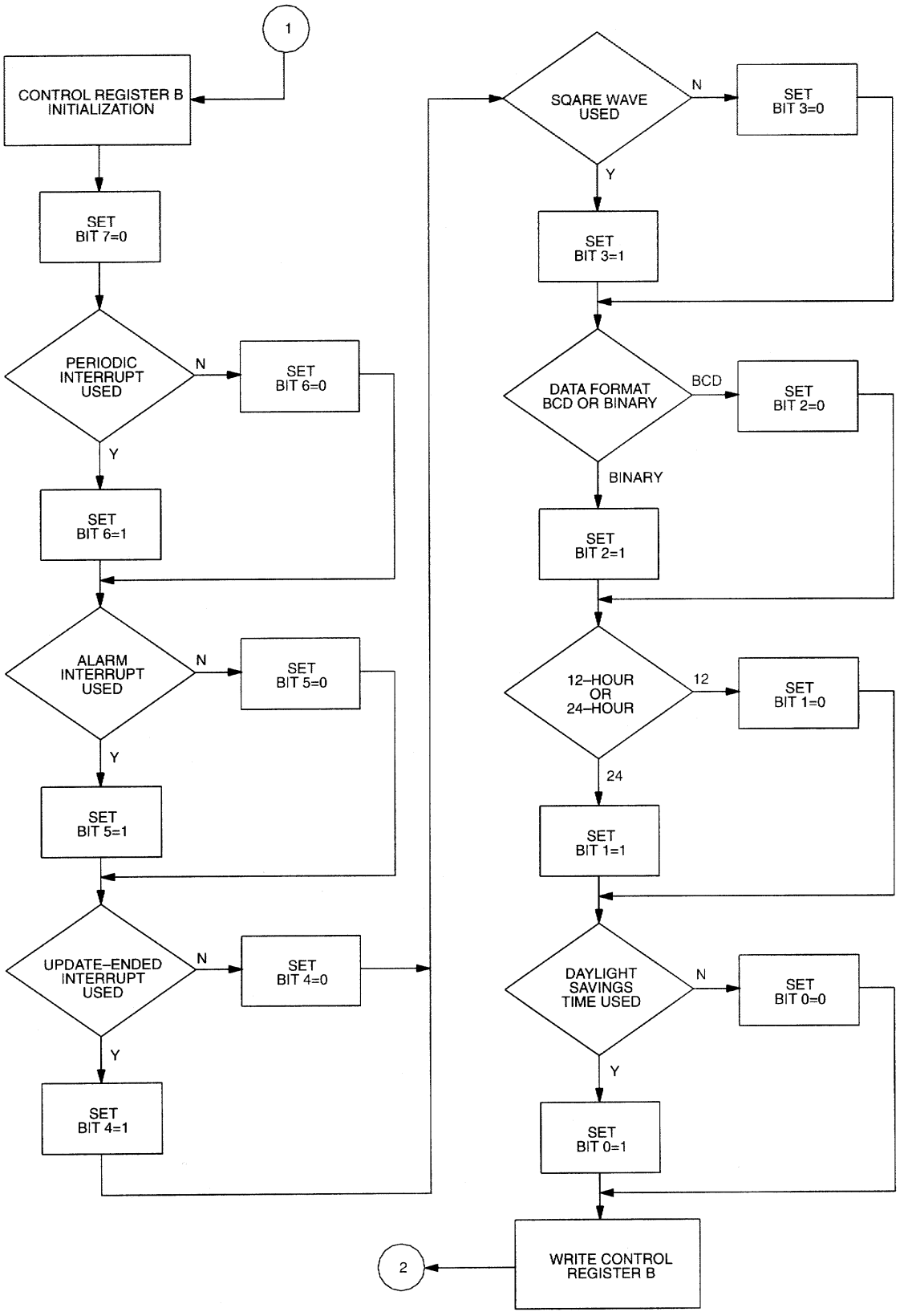
LOCATION	DESCRIPTION
04Bh	Extended Control Register 4B Bit 7 Auxiliary Battery Enable (ABE) 0=auxiliary battery input not being used 1=auxiliary battery input used for extended features Bit 6 Enable 32 kHz (E32K) 0=32 kHz disabled 1=32 kHz enabled to be output on the SQW pin Bit 5 Crystal Selection (CS) 0=oscillator configured for a crystal with a load capacitance of 6 pF 1=oscillator configured for a crystal with a load capacitance of 12.5 pF Bit 4 RAM Clear Enable (RCE) 0=RAM clear function is disabled 1=allows $\overline{\text{RCLR}}$ pin to clear user RAM Bit 3 Power Active Bar Reset Select (PRS) 0= $\overline{\text{PWR}}$ pin will go High-Z when entering power fail 1= $\overline{\text{PWR}}$ pin remains active when entering power fail Bit 2 RAM Clear Interrupt Enable (RIE) 0=disabled 1=enables RAM clear function to generate interrupts Bit 1 Wakeup Alarm Interrupt Enable (WIE) 0=disabled 1=enables wakeup alarm to generate interrupts Bit 0 Kickstart Interrupt Enable (KSE) 0=disabled 1=enables $\overline{\text{KS}}$ to generate interrupts

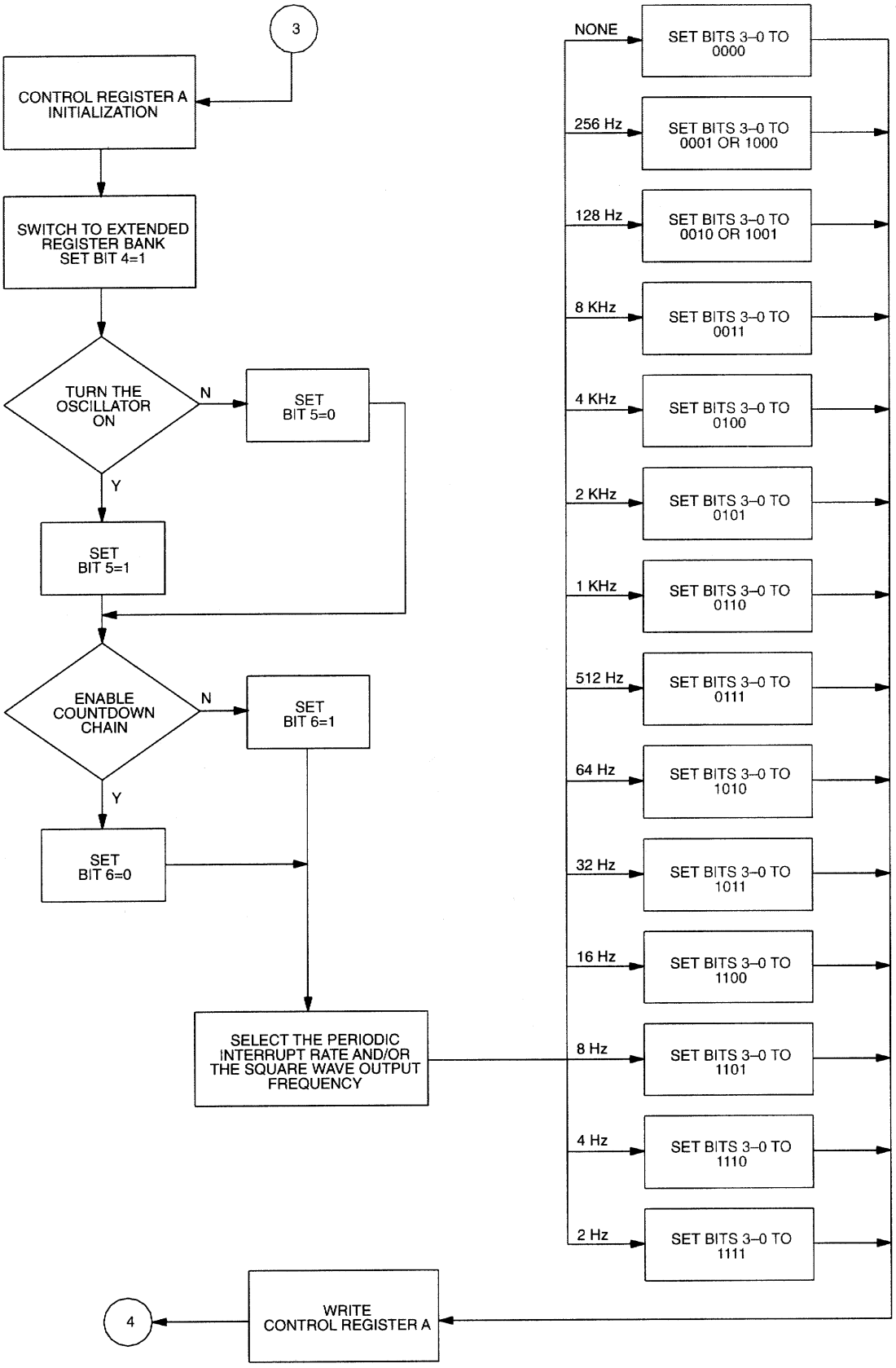
NOTES:

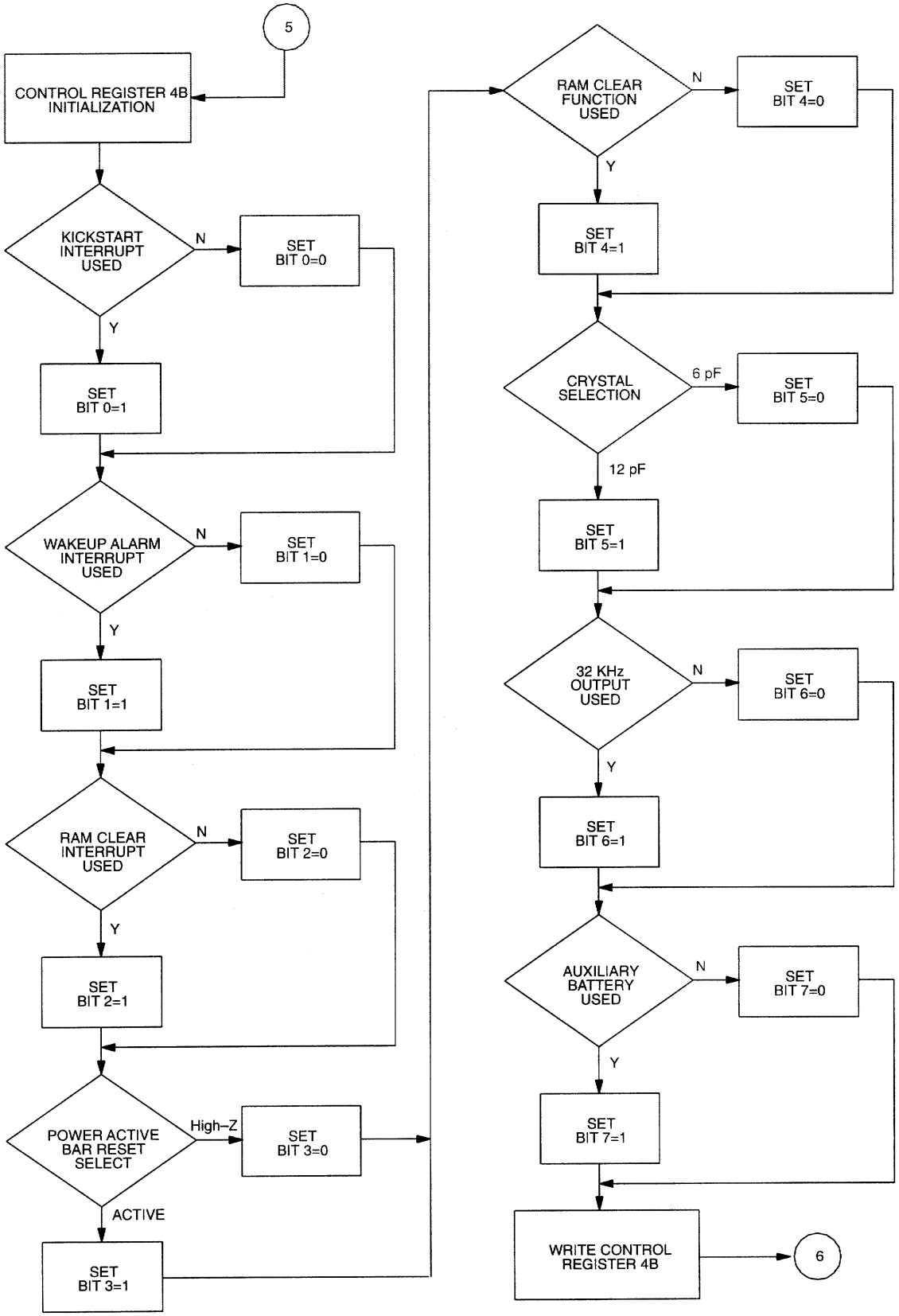
1. Burst Mode Enable (BME) is available only on the DS17285/87, DS17485/87, and DS17885/87 devices.

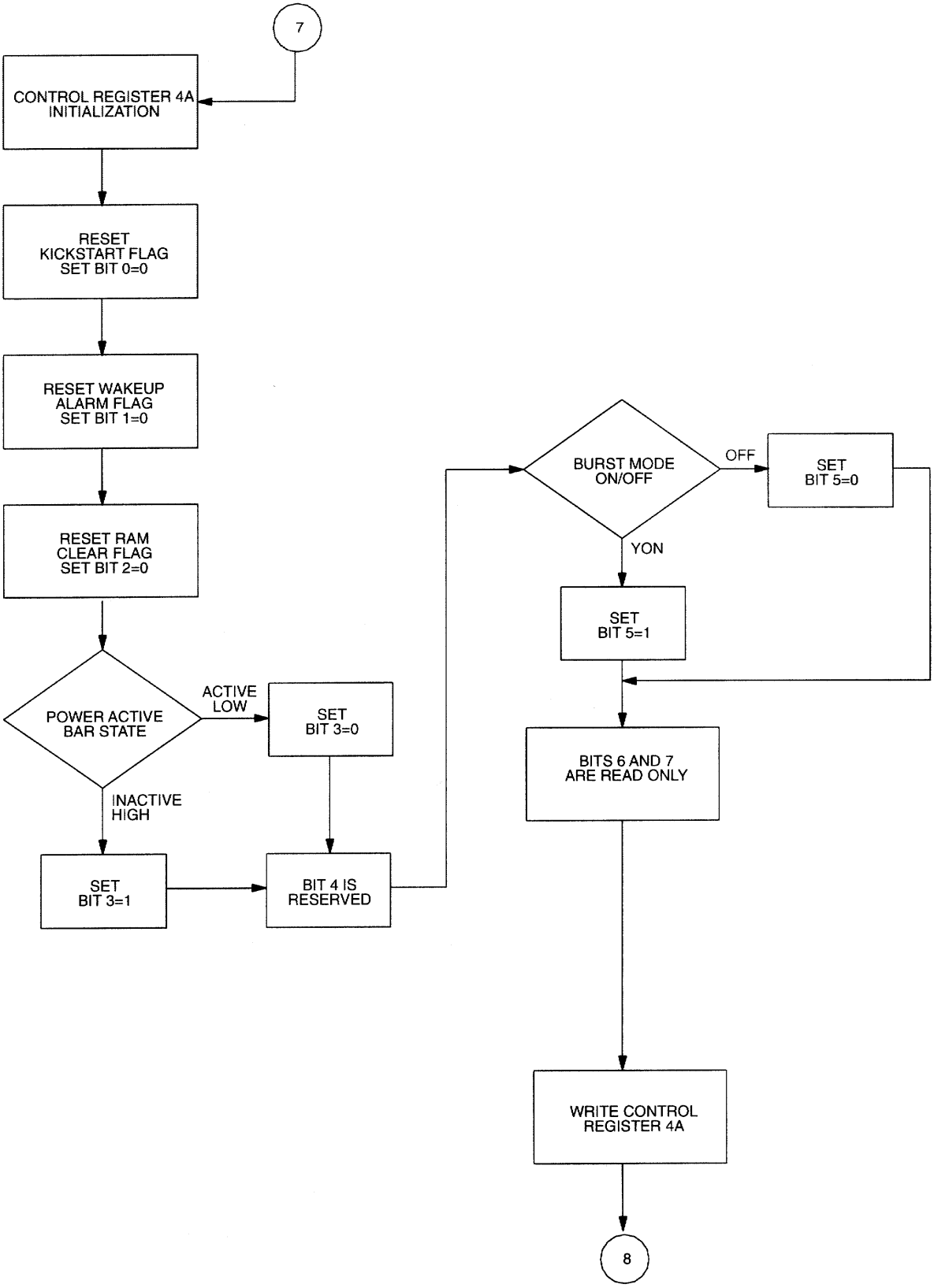
INITIALIZATION PROCEDURE

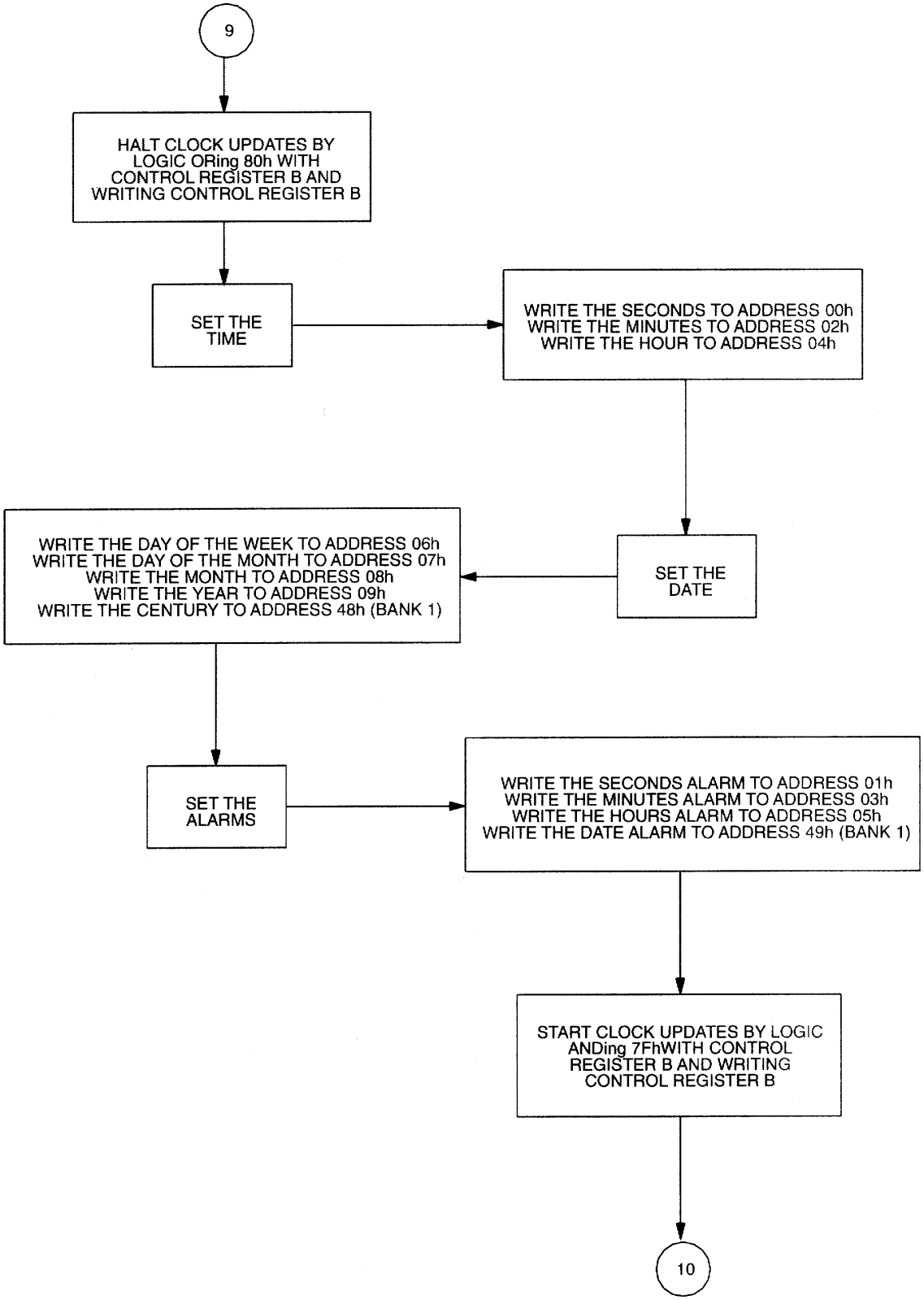



1
CONTROL REGISTER B INITIALIZATION
SET BIT 7=0
PERIODIC INTERRUPT USED
N
SET BIT 6=0
Y
SET BIT 6=1
ALARM INTERRUPT USED
N
SET BIT 5=0
Y
SET BIT 5=1
UPDATE-ENDED INTERRUPT USED
N
SET BIT 4=0
Y
SET BIT 4=1
SQARE WAVE USED
N
SET BIT 3=0
Y
SET BIT 3=1
DATA FORMAT BCD OR BINARY
BCD
SET BIT 2=0
BINARY
SET BIT 2=1
12-HOUR OR 24-HOUR
12
SET BIT 1=0
24
SET BIT 1=1
DAYLIGHT SAVINGS TIME USED
N
SET BIT 0=0
Y
SET BIT 0=1
WRITE CONTROL REGISTER B
2


3
CONTROL REGISTER A INITIALIZATION
SWITCH TO EXTENDED REGISTER BANK SET BIT 4=1
TURN THE OSCILLATOR ON
N
SET BIT 5=0
Y
SET BIT 5=1
ENABLE COUNTDOWN CHAIN
N
SET BIT 6=1
Y
SET BIT 6=0
SELECT THE PERIODIC INTERRUPT RATE AND/OR THE SQUARE WAVE OUTPUT FREQUENCY
NONE
SET BITS 3–0 TO 0000
256 Hz
SET BITS 3–0 TO 0001 OR 1000
128 Hz
SET BITS 3–0 TO 0010 OR 1001
8 KHz
SET BITS 3–0 TO 0011
4 KHz
SET BITS 3–0 TO 0100
2 KHz
SET BITS 3–0 TO 0101
1 KHz
SET BITS 3–0 TO 0110
512 Hz
SET BITS 3–0 TO 0111
64 Hz
SET BITS 3–0 TO 1010
32 Hz
SET BITS 3–0 TO 1011
16 Hz
SET BITS 3–0 TO 1100
8 Hz
SET BITS 3–0 TO 1101
4 Hz
SET BITS 3–0 TO 1110
2 Hz
SET BITS 3–0 TO 1111
WRITE CONTROL REGISTER A
4


5
CONTROL REGISTER 4B INITIALIZATION
KICKSTART INTERRUPT USED
N
SET BIT 0=0
Y
SET BIT 0=1
WAKEUP ALARM INTERRUPT USED
N
SET BIT 1=0
Y
SET BIT 1=1
RAM CLEAR INTERRUPT USED
N
SET BIT 2=0
Y
SET BIT 2=1
POWER ACTIVE BAR RESET SELECT
High–Z
SET BIT 3=0
ACTIVE
SET BIT 3=1
RAM CLEAR FUNCTION USED
N
SET BIT 4=0
Y
SET BIT 4=1
CRYSTAL SELECTION
6 pF
SET BIT 5=0
12 pF
SET BIT 5=1
32 KHz OUTPUT USED
N
SET BIT 6=0
Y
SET BIT 6=1
AUXILIARY BATTERY USED
N
SET BIT 7=0
Y
SET BIT 7=1
WRITE CONTROL REGISTER 4B
6


7
CONTROL REGISTER 4A INITIALIZATION
RESET KICKSTART FLAG SET BIT 0=0
RESET WAKEUP ALARM FLAG SET BIT 1=0
RESET RAM CLEAR FLAG SET BIT 2=0
POWER ACTIVE BAR STATE
ACTIVE LOW
SET BIT 3=0
INACTIVE HIGH
SET BIT 3=1
BIT 4 IS RESERVED
BURST MODE ON/OFF
OFF
SET BIT 5=0
YON
SET BIT 5=1
BITS 6 AND 7 ARE READ ONLY
WRITE CONTROL REGISTER 4A
8


9
HALT CLOCK UPDATES BY LOGIC ORing 80h WITH CONTROL REGISTER B AND WRITING CONTROL REGISTER B
SET THE TIME
WRITE THE SECONDS TO ADDRESS 00h
WRITE THE MINUTES TO ADDRESS 02h
WRITE THE HOUR TO ADDRESS 04h
SET THE DATE
WRITE THE DAY OF THE WEEK TO ADDRESS 06h
WRITE THE DAY OF THE MONTH TO ADDRESS 07h
WRITE THE MONTH TO ADDRESS 08h
WRITE THE YEAR TO ADDRESS 09h
WRITE THE CENTURY TO ADDRESS 48h (BANK 1)
SET THE ALARMS
WRITE THE SECONDS ALARM TO ADDRESS 01h
WRITE THE MINUTES ALARM TO ADDRESS 03h
WRITE THE HOURS ALARM TO ADDRESS 05h
WRITE THE DATE ALARM TO ADDRESS 49h (BANK 1)
START CLOCK UPDATES BY LOGIC ANDing 7FhWITH CONTROL REGISTER B AND WRITING CONTROL REGISTER B
10