



STW45NM60

N-channel 650V @ Tjmax - 0.09Ω - 45A - TO-247
MDmesh™ Power MOSFET

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STW45NM60	650V	< 0.11Ω	45A

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Description

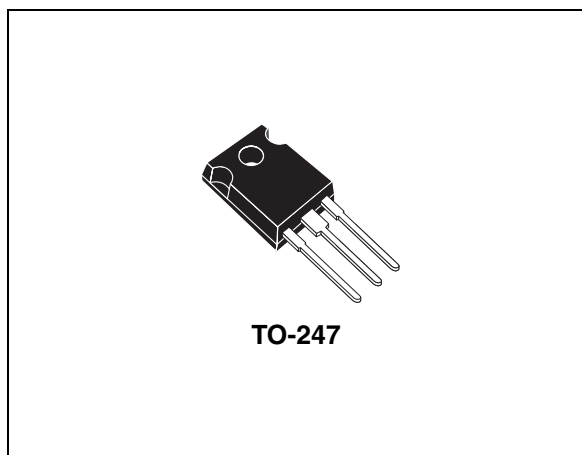
The MDmesh™ is a new revolutionary Power MOSFET technology that associates the multiple drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competitor's products.

Application

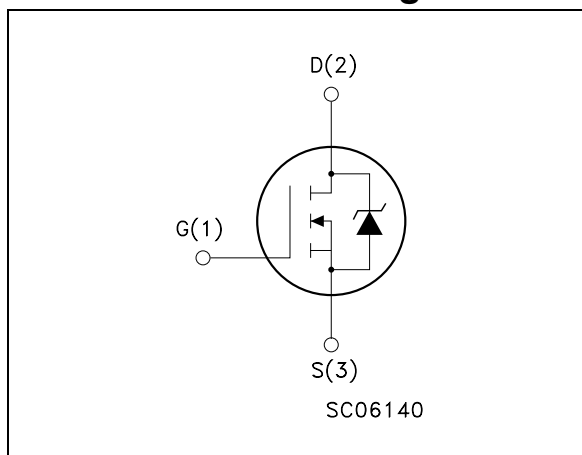
- Switching application

Order code

Part number	Marking	Package	Packaging
STW45NM60	W45NM60	TO-247	Tube



Internal schematic diagram



Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	45	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	28	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	417	W
	Derating factor	3.33	W/°C
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 45\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.3	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	30	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 35\text{V}$)	850	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	600			V
I _{DSS}	Zero gate voltage Drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C = 125 °C			10 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 22.5A		0.09	0.11	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 22.5A		30		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		3800 1250 80		pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0V, V _{DS} = 0V to 480V		340		pF
R _G	Gate input resistance	f=1 MHz Gate DC Bias = 0 test signal level = 20mV open drain		1.4		Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 400V, I _D = 45A, V _{GS} = 10V <i>Figure 14</i>		96 31 43	134	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%.

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 250V$, $I_D = 22.5A$ $R_G = 4.7\Omega$, $V_{GS} = 10V$ <i>Figure 13</i>		30 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{DD} = 400V$, $I_D = 45A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ <i>Figure 13</i>		16 23 40		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				45	A
I_{SDM}	Source-drain current (pulsed)				180	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 45A$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 45A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$, $T_j = 25^\circ C$ <i>Figure 15</i>		508 10 40		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 45A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$, $T_j = 150^\circ C$ <i>Figure 15</i>		650 14 43		ns μC A

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

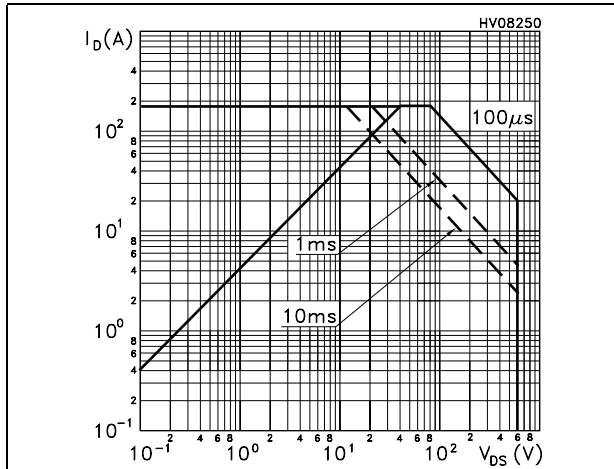


Figure 2. Thermal impedance

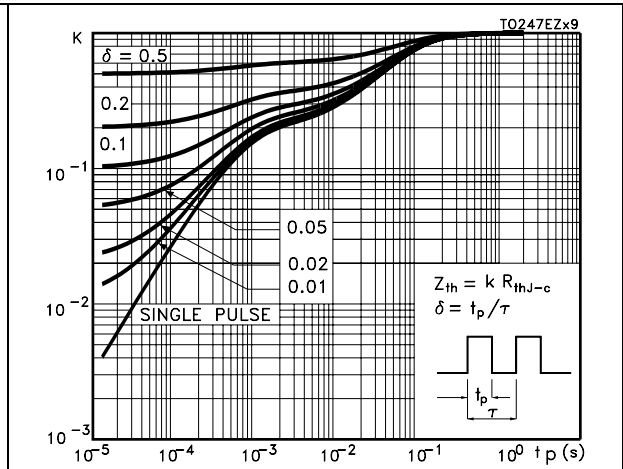


Figure 3. Output characteristics

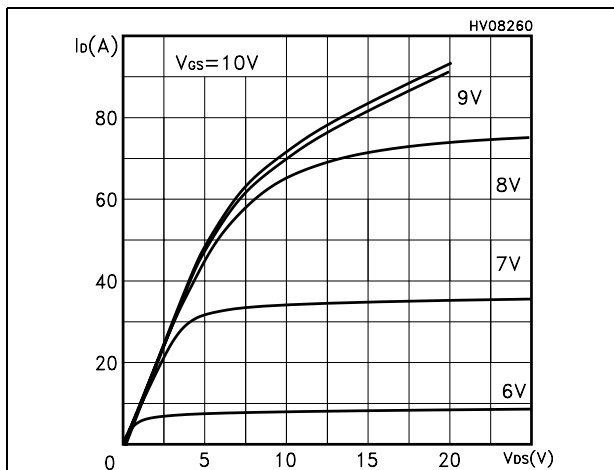


Figure 4. Transfer characteristics

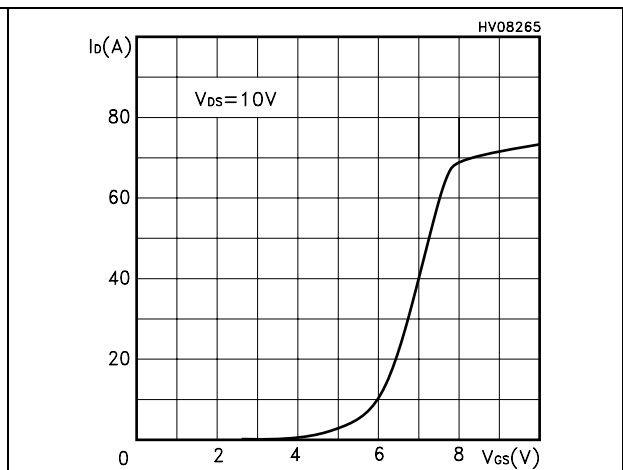


Figure 5. Transconductance

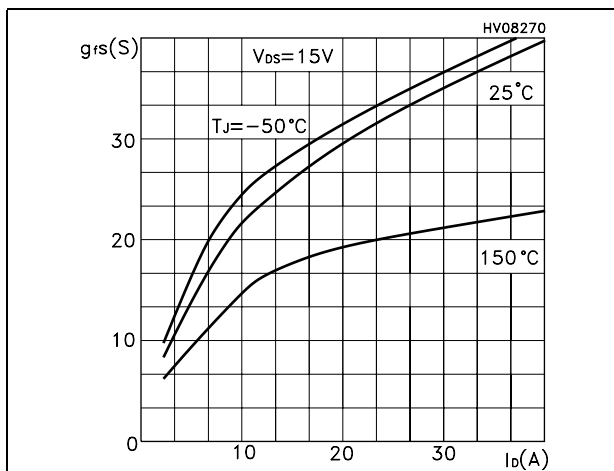


Figure 6. Static-drain source on resistance

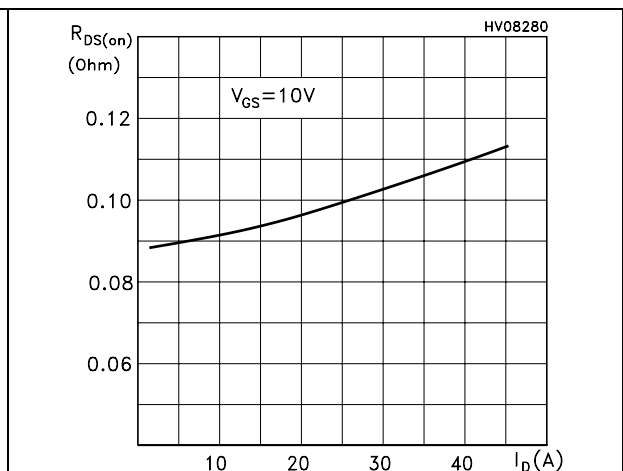


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

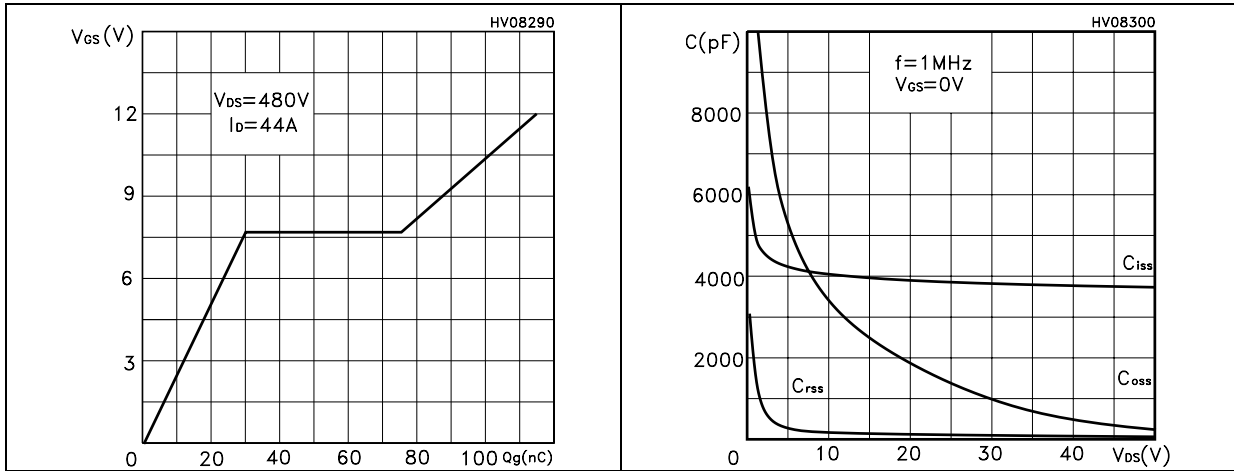


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

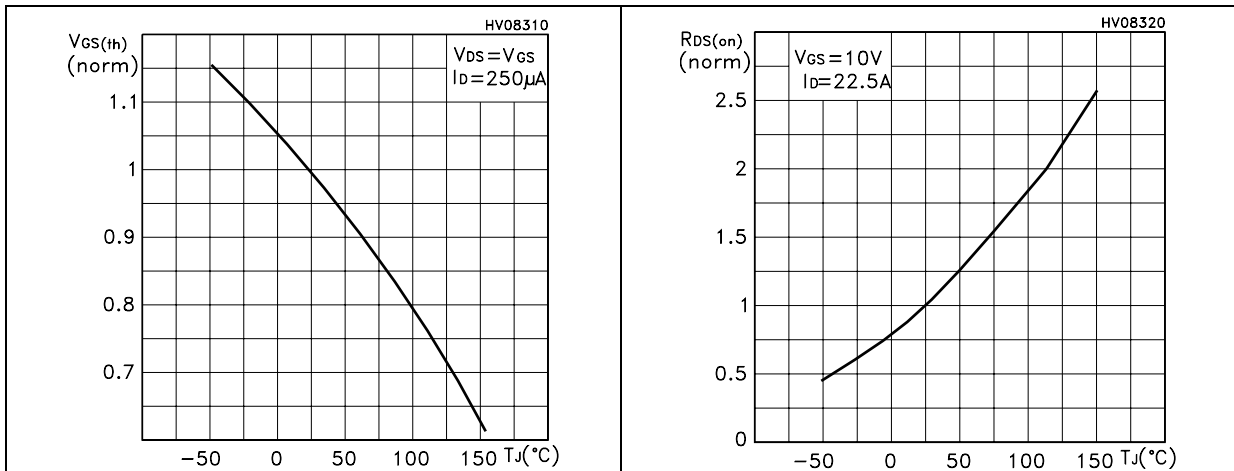
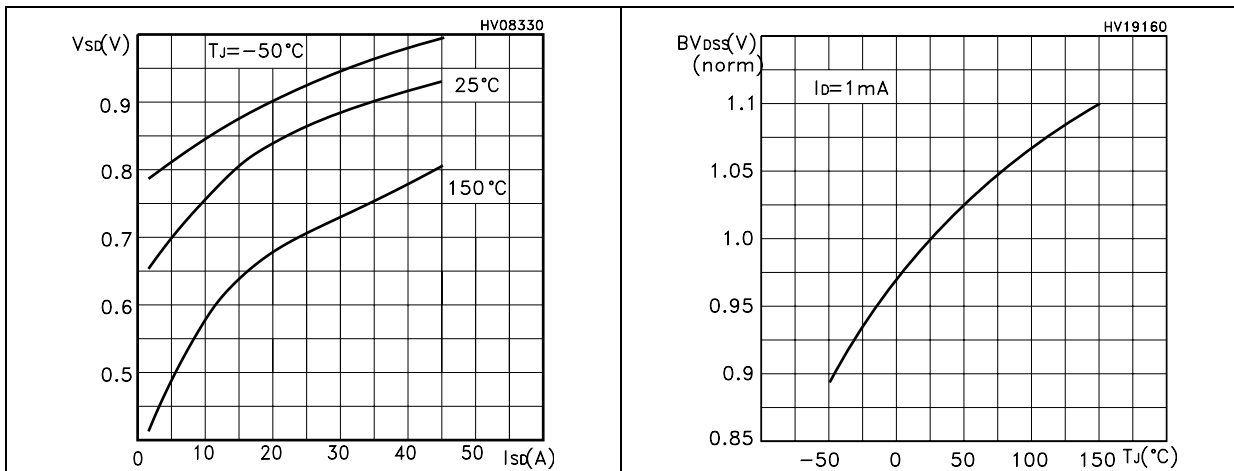


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

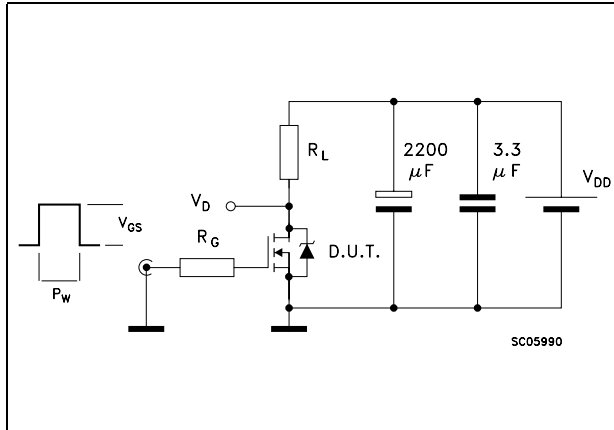


Figure 14. Gate charge test circuit

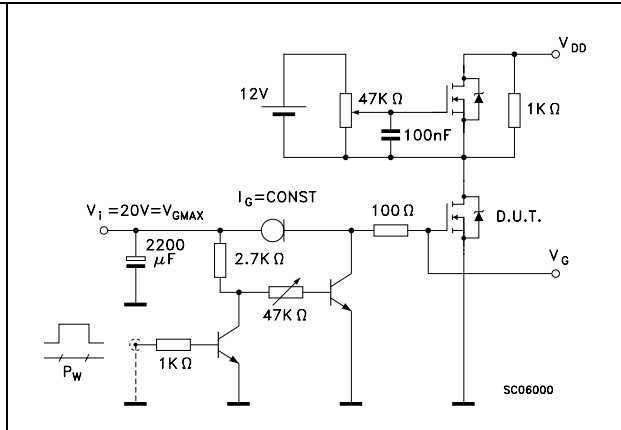


Figure 15. Test circuit for inductive load switching and diode recovery times

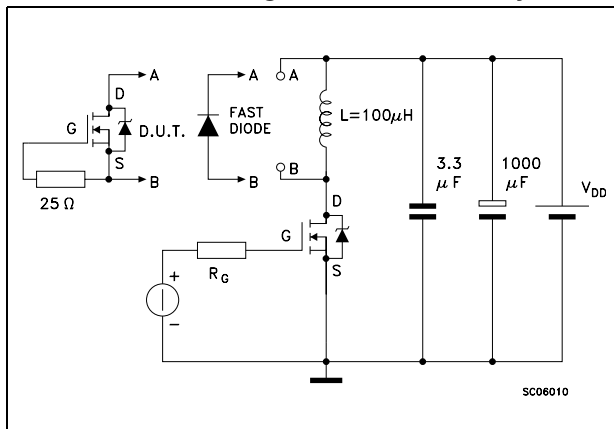


Figure 16. Unclamped inductive load test circuit

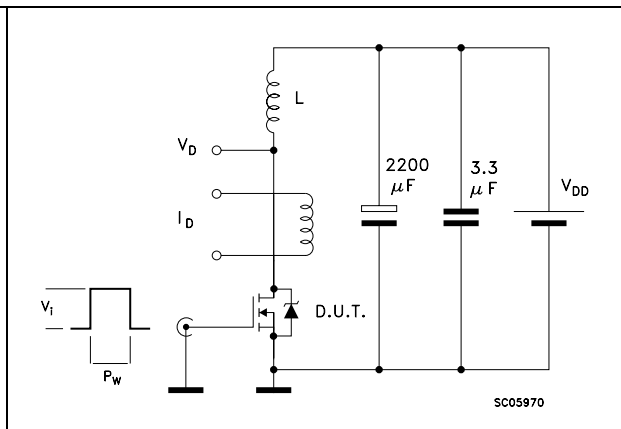


Figure 17. Unclamped inductive waveform

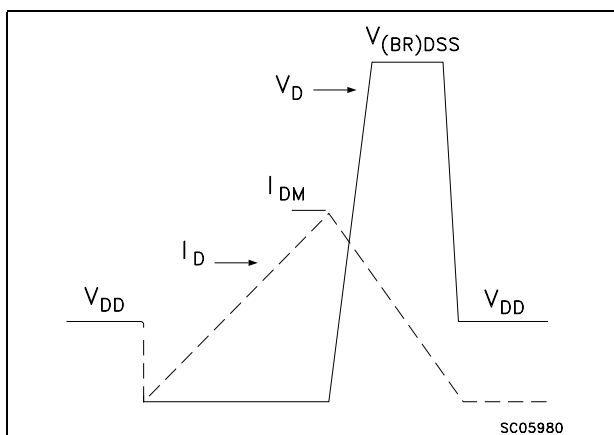
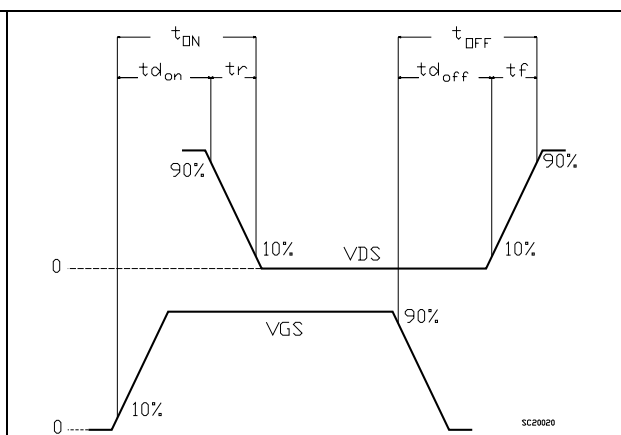


Figure 18. Switching time waveform

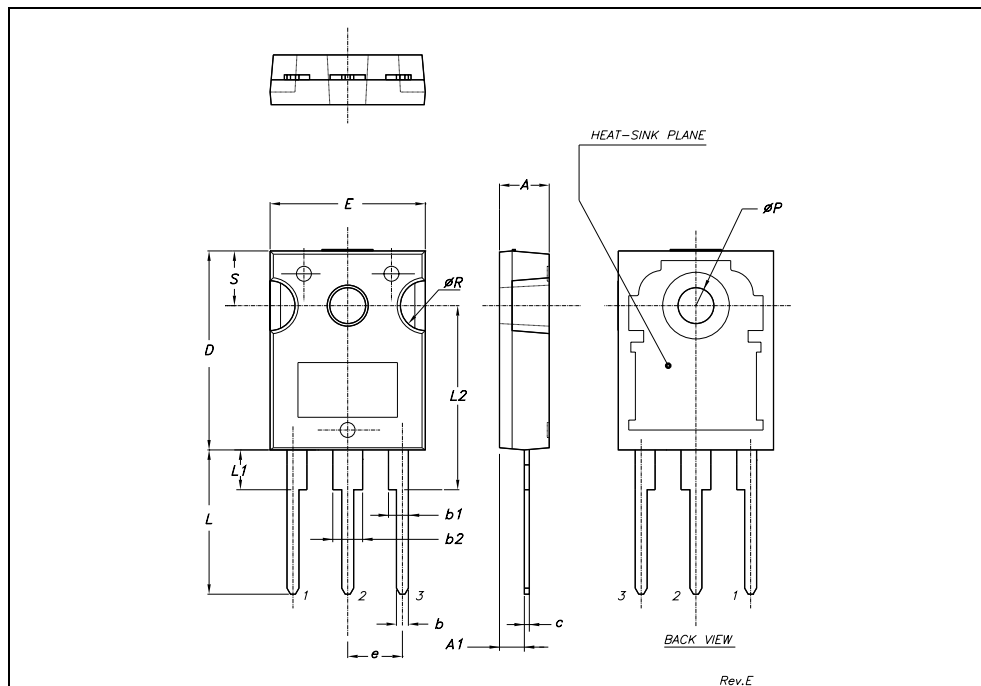


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 8. Revision history

Date	Revision	Changes
05-Mar-2005	5	Complete document with curves
16-May-2006	6	The document has been reformatted
18-Dec-2006	7	Updates curves: <i>Figure 1.</i> , <i>Figure 4.</i> and <i>Figure 6.</i>
02-Apr-2007	8	<i>Figure 1.</i> has been updated.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com