Description

The AP2162A and AP2172A are dual channel current-limit integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB standards and available with both polarities of Enable input.

The devices have fast short-circuit response time for improved overall system robustness, and have integrated output discharge function to ensure completely controlled discharging of the output voltage capacitor. They provide a complete protection solution for application subject to heavy capacitive loads and the prospect of short circuit, and offer reverse current blocking, overcurrent, overtemperature and short-circuit protections, as well as controlled rise time and undervoltage lockout functionality. A 7ms deglitch capability on the open-drain flag output prevents false overcurrent reporting and does not require any external components.

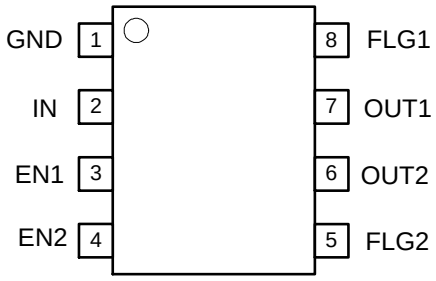
Both devices are available in SO-8, MSOP-8EP and U-DFN3030-8 (Type E) packages.

Features

- Dual Channel Current-Limit Power Switch with Output Discharge
- Fast Short-Circuit Response Time: 2µs
- 1.4A Accurate Current Limiting
- Reverse Current Blocking
- 85mΩ On-Resistance
- Input Voltage Range: 2.7V to 5.5V
- Built-in Soft-Start with 0.6ms Typical Rise Time
- Short-Circuit and Thermal Protection
- Fault Report (FLG) with Blanking Time (7ms typ)
- ESD Protection: 2kV HBM, 300V MM
- Active High (AP2172A) or Active Low (AP2162A) Enable
- Ambient Temperature Range: -40°C to +85°C
- SO-8, MSOP-8EP and U-DFN3030-8 (Type E) (Exposed Pad): Available in “Green” Molding Compound (No Br, Sb)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified
- Thermally-Efficient Low Profile Packages
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

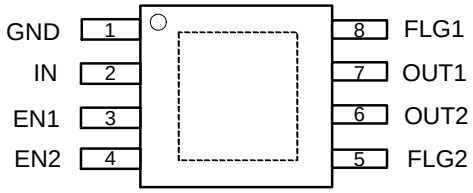
Pin Assignments

(Top View)



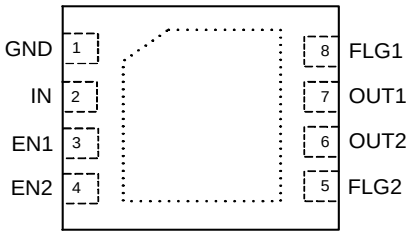
SO-8

(Top View)



MSOP-8EP

(Top View)



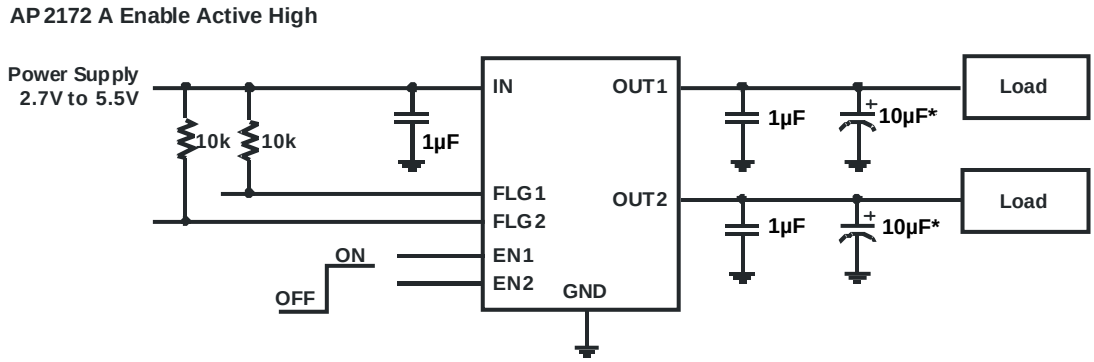
U-DFN3030-8 (Type E)

Applications

- LCD TVs & monitors
- Set-top boxes, residential gateways
- Laptops, desktops, servers
- Printers, docking stations, hubs

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



Note: * USB 2.0 requires 120µF per hub

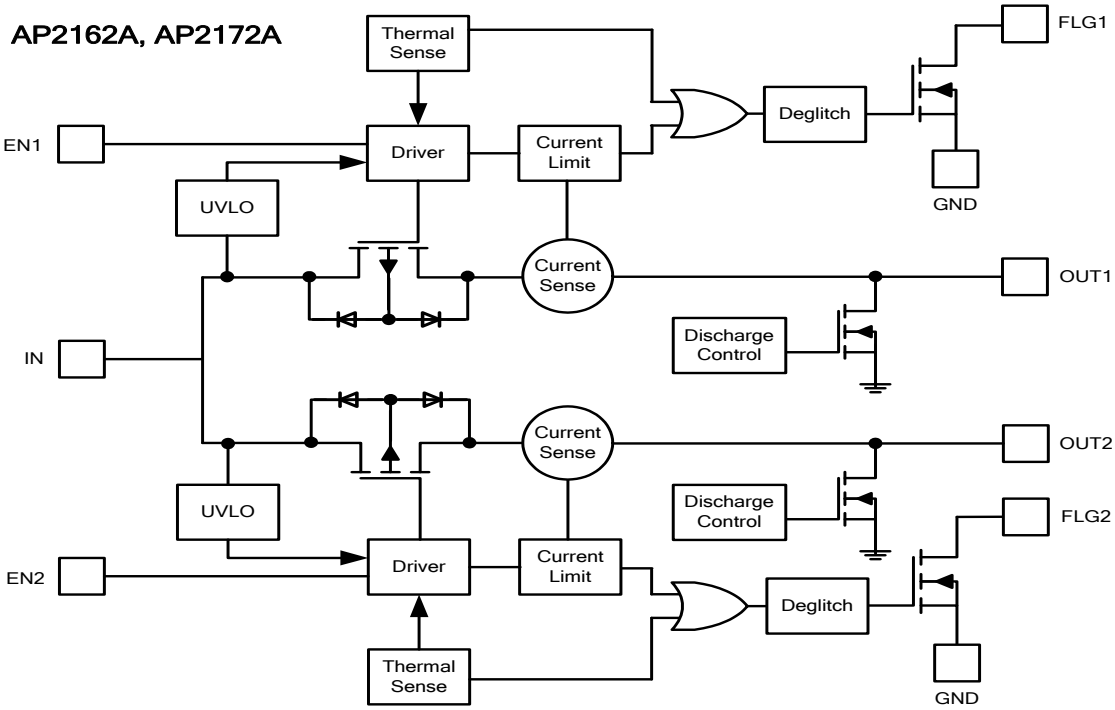
Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (Typ)	Recommended Maximum Continuous Load Current
AP2162A	2	Active Low	1.4A	1.0A
AP2172A	2	Active High	1.4A	1.0A

Pin Descriptions

Pin Name	Pin Number		Function
	SO-8	MSOP-8EP U-DFN3030-8 (Type E)	
GND	1	1	Ground
IN	2	2	Voltage input pin
EN1	3	3	Switch 1 enable input, active low (AP2162A) or active high (AP2172A)
EN2	4	4	Switch 2 enable input, active low (AP2162A) or active high (AP2172A)
FLG2	5	5	Switch 2 overcurrent and overtemperature fault report; open-drain flag is active low when triggered
OUT2	6	6	Switch 2 voltage output pin
OUT1	7	7	Switch 1 voltage output pin
FLG1	8	8	Switch 1 overcurrent and overtemperature fault report; open-drain flag is active low when triggered
Exposed Pad	—	Exposed Pad	Exposed Pad: It should be connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD MM	Machine Model ESD Protection	300	V
V_{IN}	Input Voltage	6.5	V
V_{OUT}	Output Voltage	V_{IN} +0.3	V
V_{EN}, V_{FLG}	Enable Voltage	6.5	V
I_{LOAD}	Maximum Continuous Load Current	Internal Limited	A
$T_{J(MAX)}$	Maximum Junction Temperature	+150	°C
T_{ST}	Storage Temperature Range (Note 5)	-65 to +150	°C

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. UL recognized rating from -30°C to +70°C (Diodes Incorporated qualified T_{ST} from -65°C to +150°C).

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.7	5.5	V
I_{OUT}	Output Current	0	1.0	A
V_{IH}	High-Level Input Voltage on EN or $\overline{EN}$	2	V_{IN}	V
V_{IL}	Low-Level Input Voltage on EN or $\overline{EN}$	0	0.8	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, V_{IN} = +5.0V, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 6)		Min	Typ	Max	Unit
V_{UVLO}	Input UVLO	—		1.6	2.0	2.4	V
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0		—	0.1	1	µA
I_Q	Input Quiescent Current, Dual	Enabled, I_{OUT} = 0		—	115	180	µA
I_{LEAK}	Input Leakage Current	Disabled, OUT grounded		—	—	1	µA
I_{REV}	Reverse Leakage Current	Disabled, V_{IN} = 0V, V_{OUT} = 5V, I_{REV} at V_{IN}		—	0.01	0.1	µA
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5V, I_{OUT} = 1A, T_A = +25°C	SO-8	—	90	110	mΩ
			MSOP-8EP U-DFN3030-8 (Type E)	—	85	105	
		V_{IN} = 5V, I_{OUT} = 1A, -40°C ≤ T_A ≤ +85°C		—	—	135	
		V_{IN} = 3.3V, I_{OUT} = 1A, T_A = +25°C	SO-8	—	110	130	
			MSOP-8EP U-DFN3030-8 (Type E)	—	105	125	
		V_{IN} = 3.3V, I_{OUT} = 1A, -40°C ≤ T_A ≤ +85°C		—	—	170	
I_{LIMIT}	Overload Current Limit	V_{IN} = 5V, V_{OUT} = 4V, C_L = 10µF	-40°C ≤ T_A ≤ +85°C	1.1	1.4	1.7	A
I_{LIMIT_G}	Ganged Overload Current Limit	V_{IN} = 5V, V_{OUT} = 4.8V, OUT1 & OUT2 tied together, C_L = 10µF	-40°C ≤ T_A ≤ +85°C	2.2	2.8	3.4	A
I_{Trig}	Current Limiting Trigger Threshold	Output Current Slew Rate (< 100A/s), C_L = 10µF		—	1.8	—	A
I_{Trig_G}	Ganged Current Limiting Trigger Threshold	OUT1 & OUT2 tied together, Output Current Slew Rate (< 100A/s), C_L = 10µF		—	3.6	—	A
I_{OS}	Short-Circuit Current per Channel	OUTx connected to ground, device enabled into short circuit, C_L = 10µF		—	1.4	—	A
I_{OS_G}	Ganged Short-Circuit Current	OUT1 & OUT2 connected to ground, device enabled into short circuit, C_L = 10µF		2.2	2.8	3.4	A
t_{SHORT}	Short-Circuit Response Time	V_{OUT} = 0V to I_{OUT} = I_{LIMIT} (output shorted to ground)		—	2	—	µs
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 2.7V to 5.5V		—	—	0.8	V
V_{IH}	EN Input Logic High Voltage	V_{IN} = 2.7V to 5.5V		2	—	—	V
I_{SINK}	EN Input Leakage	V_{EN} = 0V to 5.5V		—	—	1	µA
I_{LEAK-O}	Output Leakage Current	Disabled, V_{OUT} = 0V		—	0.5	1	µA
t_R	Output Turn-On Rise Time	C_L = 1µF, R_{LOAD} = 5Ω		—	0.6	1.5	ms
t_F	Output Turn-Off Fall Time	C_L = 1µF, R_{LOAD} = 5Ω		—	0.05	0.3	ms
$t_{D(ON)}$	Output Turn-On Delay Time	C_L = 100µF, R_{LOAD} = 5Ω		—	0.2	0.5	ms
$t_{D(OFF)}$	Output Turn-Off Delay Time	C_L = 100µF, R_{LOAD} = 5Ω		—	0.1	0.3	ms
R_{FLG}	FLG Output FET On-Resistance	I_{FLG} = 10mA		—	20	40	Ω
I_{FOH}	FLG Off Current	V_{FLG} = 5V		—	0.01	1	µA
t_{Blank}	FLG Blanking Time	C_L = 10µF		4	7	15	ms
R_{DIS}	Discharge Resistance (Note 7)	V_{IN} = 5V, disabled, I_{OUT} = 1mA		—	100	—	Ω
T_{SHDN}	Thermal Shutdown Threshold	Enabled, R_{LOAD} = 1kΩ		—	+140	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—		—	+25	—	°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-8 (Note 8)		—	115	—	°C/W
		MSOP-8EP (Note 9)		—	75	—	
		U-DFN3030-8 (Type E) (Note 9)		—	60	—	

Notes:
6. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
7. The discharge function is active when the device is disabled (when enable is deasserted or during power-up/power-down when V_{IN} < V_{UVLO}). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.
8. Test condition for SO-8: Device mounted on FR-4 substrate PCB with minimum recommended pad layout.
9. Test condition for MSOP-8EP and U-DFN3030-8 (Type E): Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Typical Performance Characteristics

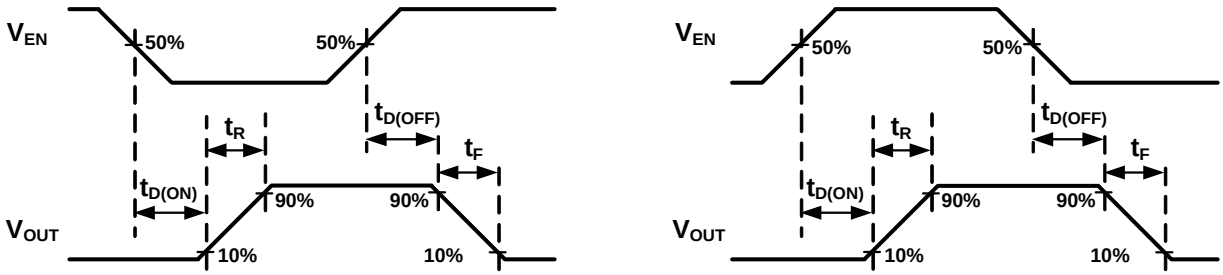


Figure 1. Voltage Waveforms: AP2162A (Left), AP2172A (Right)

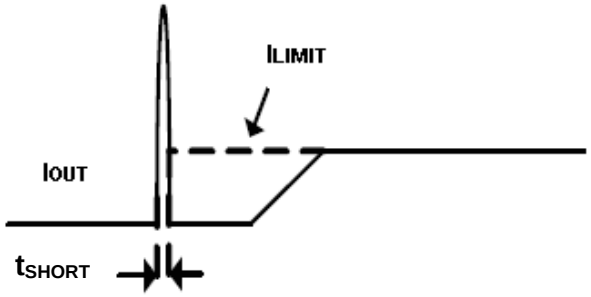
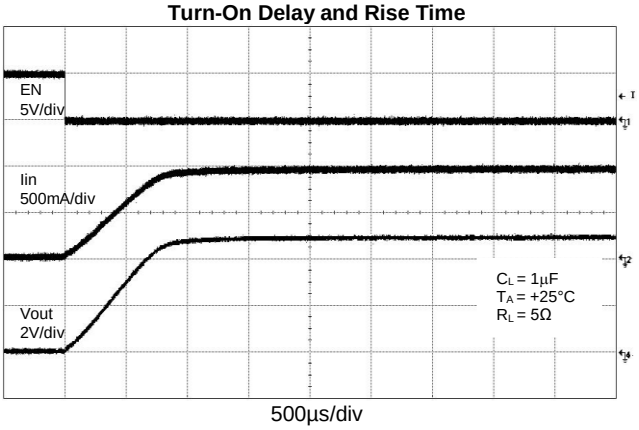


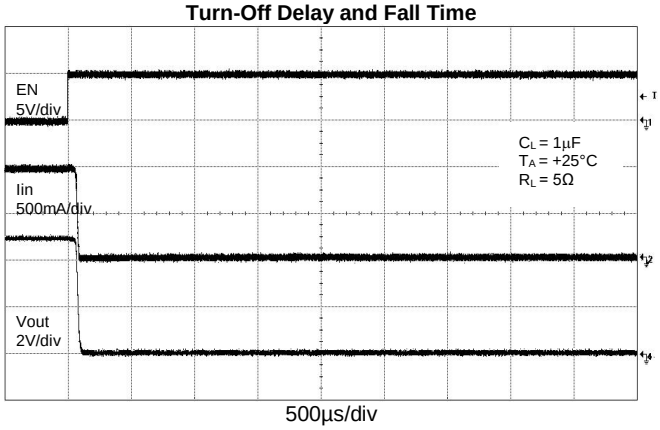
Figure 2. Response Time to Short-Circuit Waveform

All Enable Plots are for AP2162A Active Low

Turn-On Delay and Rise Time

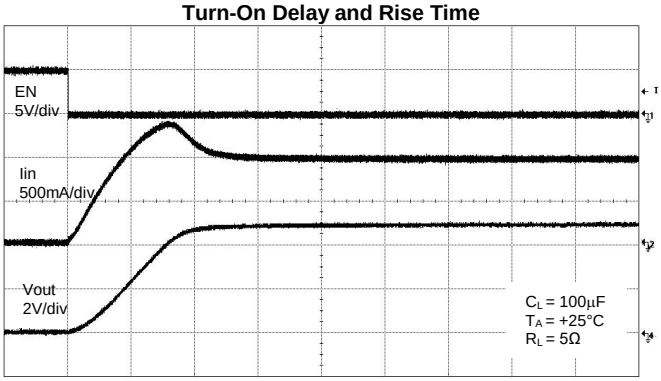


Turn-Off Delay and Fall Time

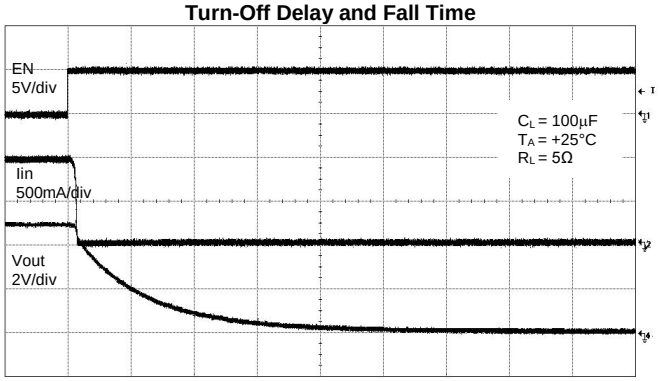


Typical Performance Characteristics (continued)

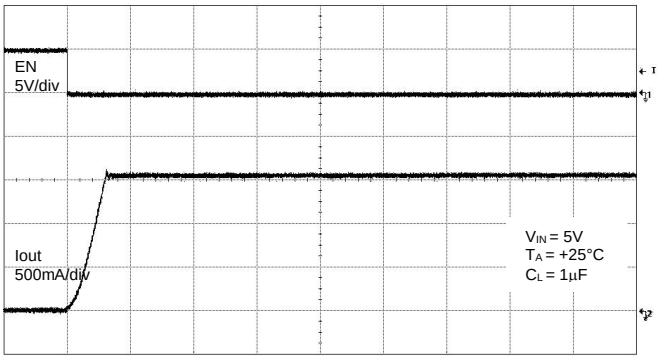
Turn-On Delay and Rise Time



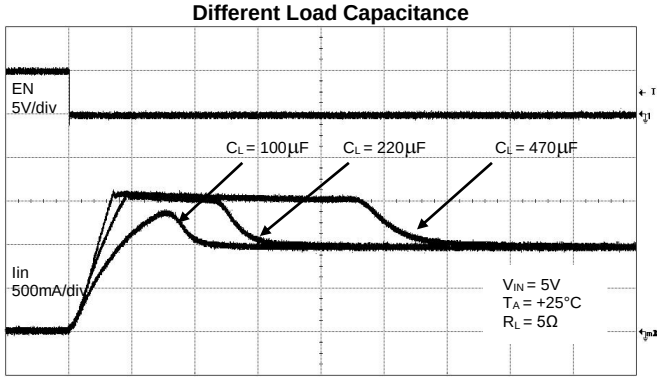
Turn-Off Delay and Fall Time



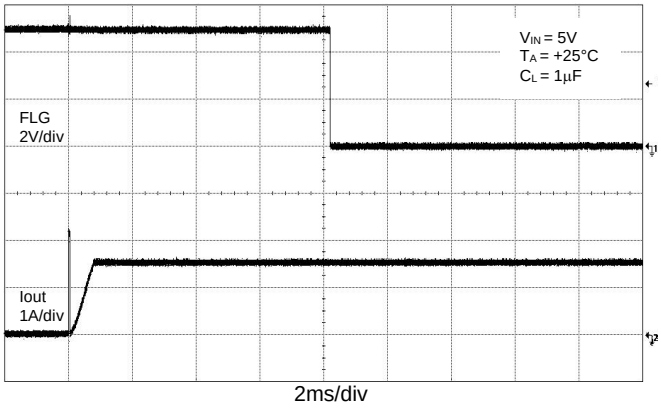
Short-Circuit Current, Device Enabled Into Short



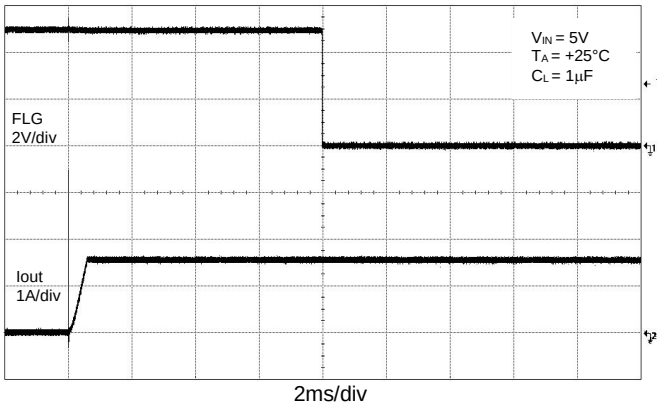
Inrush Current with Different Load Capacitance



2Ω Load Connected to Enabled Device

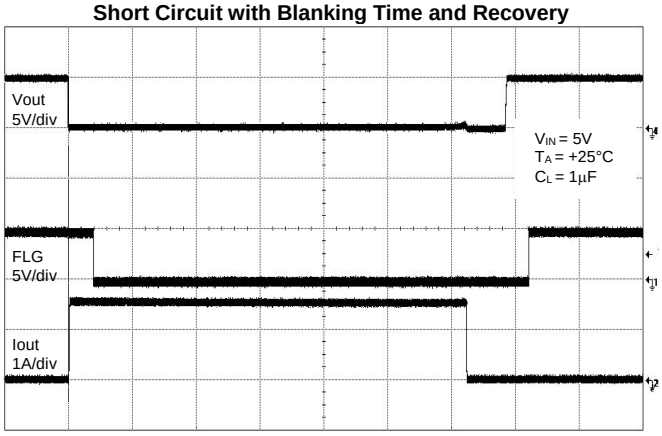


1Ω Load Connected to Enabled Device

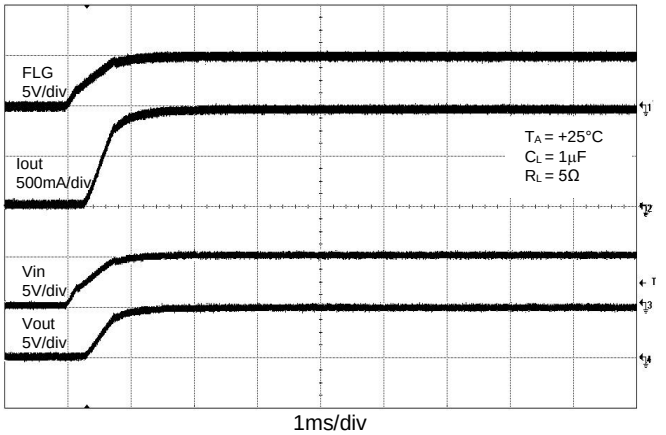


Typical Performance Characteristics (continued)

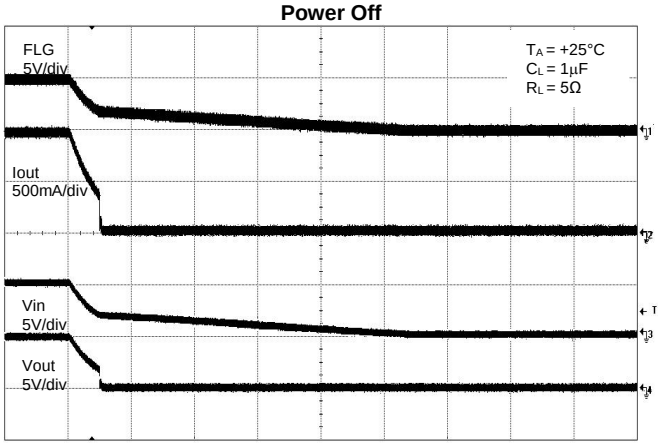
Short Circuit with Blanking Time and Recovery



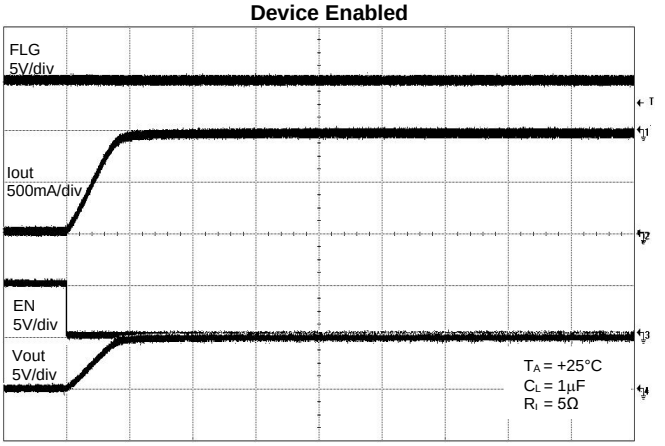
Power On



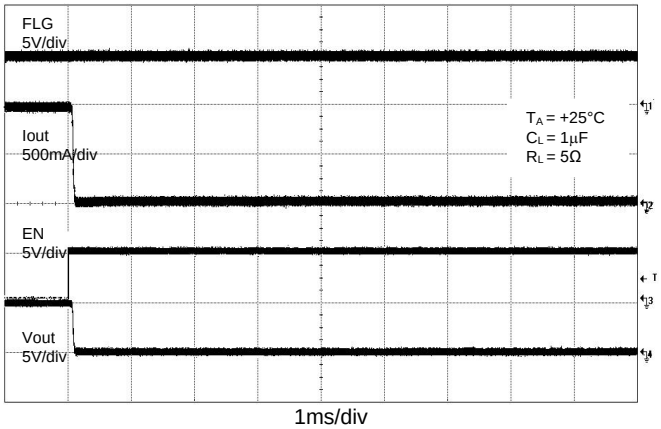
Power Off



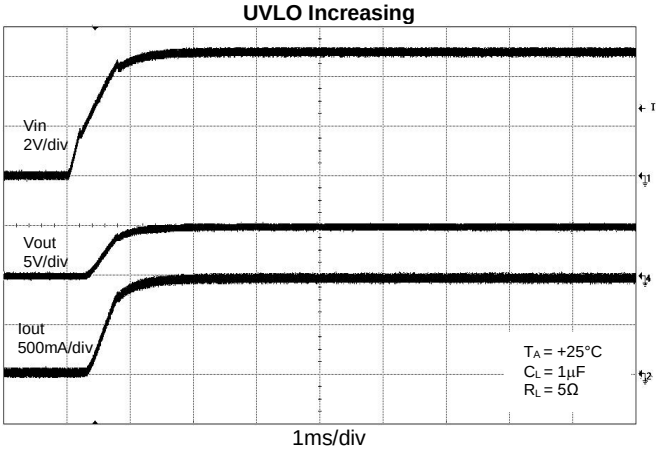
Device Enabled



Device Disabled

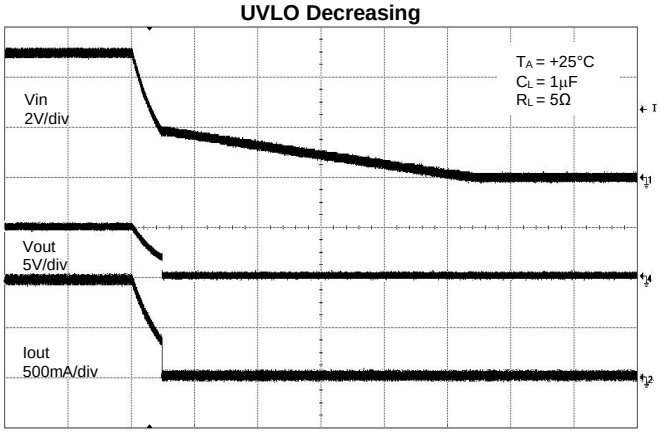


UVLO Increasing



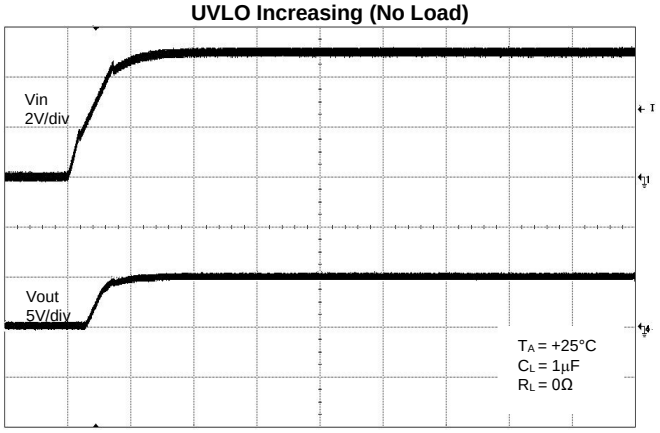
Typical Performance Characteristics (continued)

UVLO Decreasing



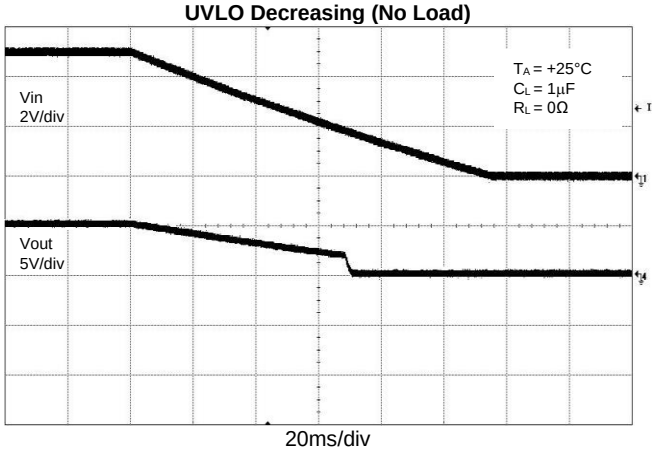
10ms/div

UVLO Increasing (No Load)



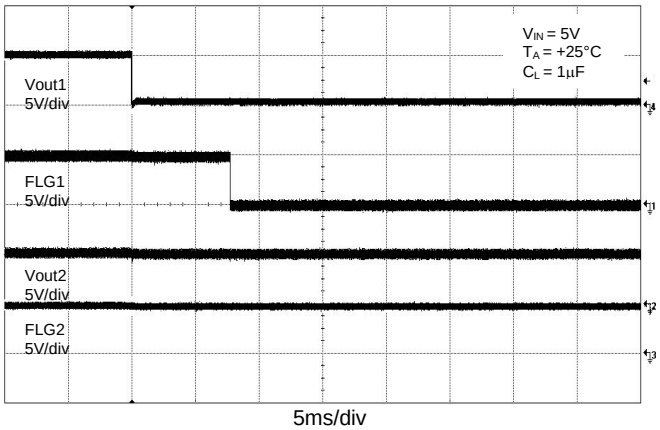
1ms/div

UVLO Decreasing (No Load)



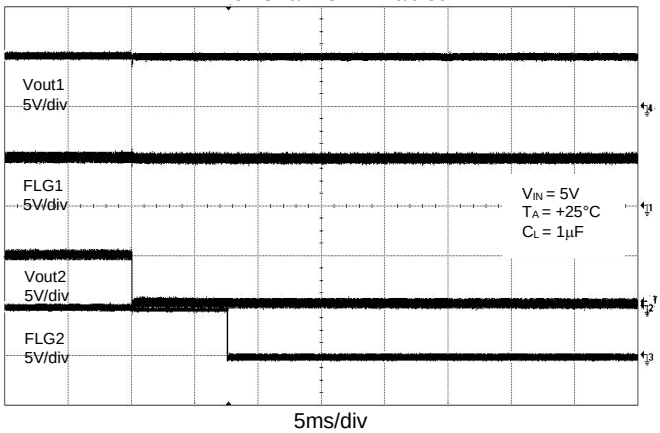
20ms/div

Channel 1 Enabled and Shorted with Channel 2 Enabled



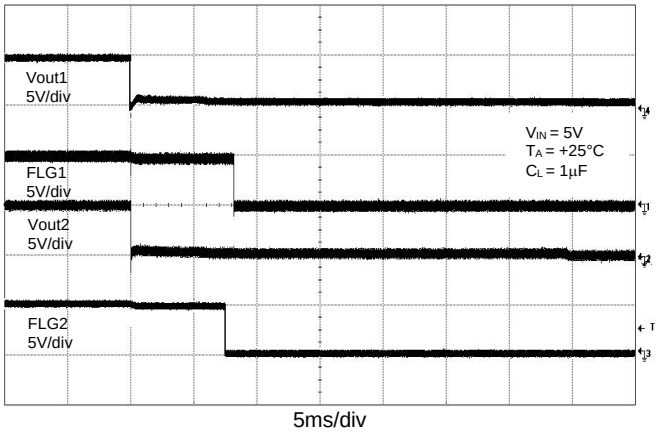
5ms/div

Channel 2 Enabled and Shorted with Channel 1 Enabled



5ms/div

Channels 1 and 2 Enabled and Shorted



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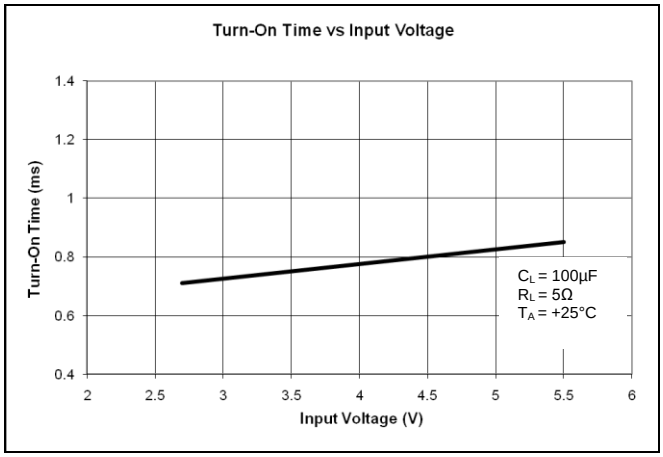
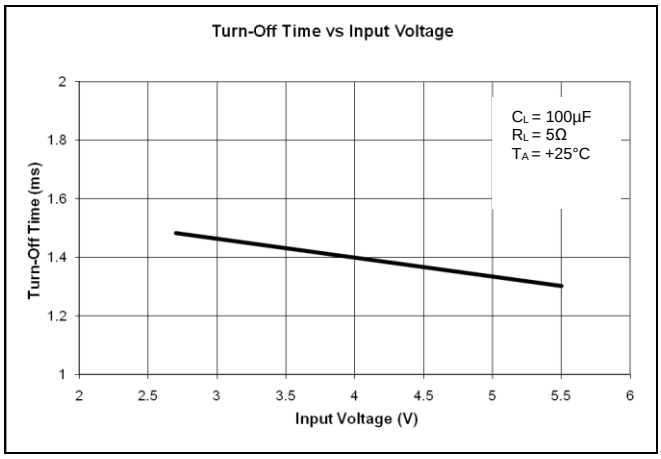
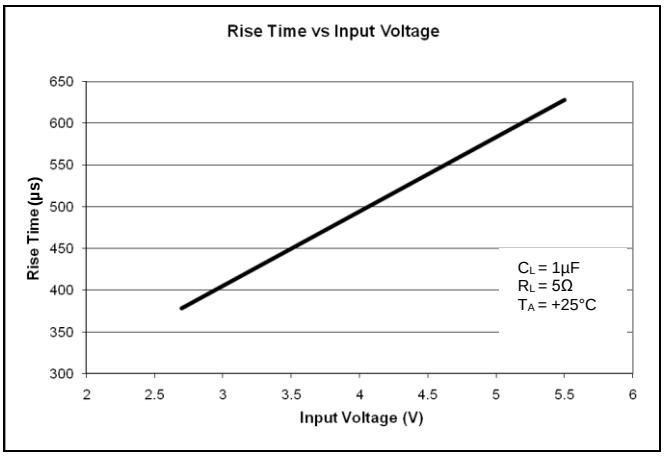
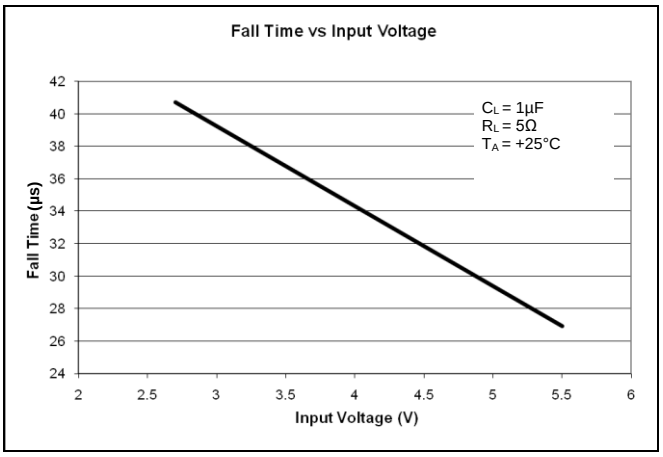
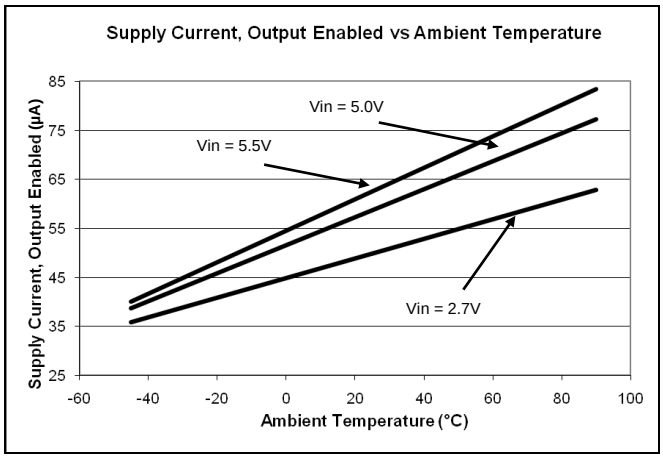
Typical Performance Characteristics (continued)

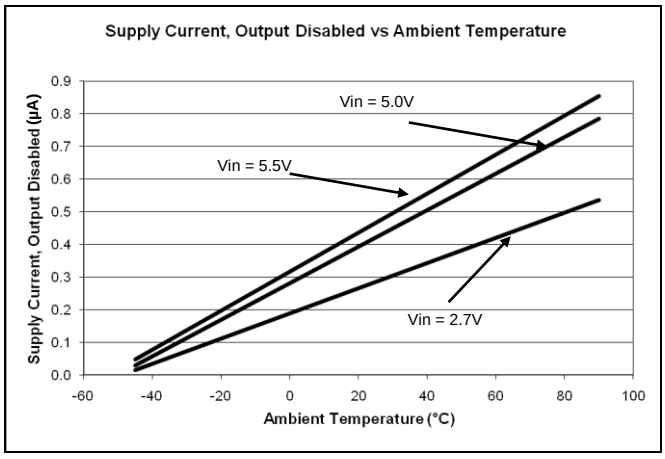




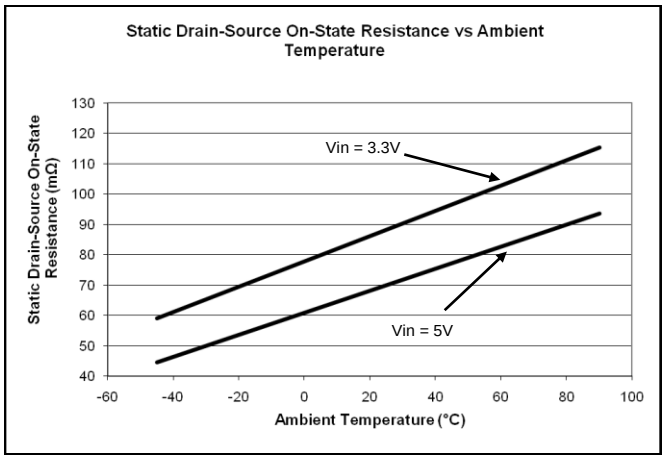


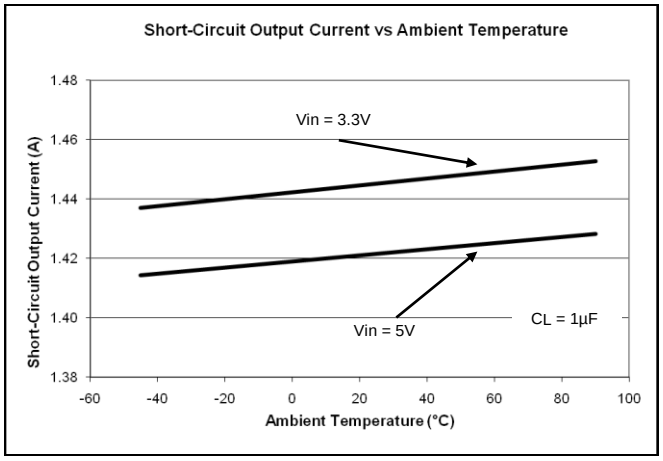


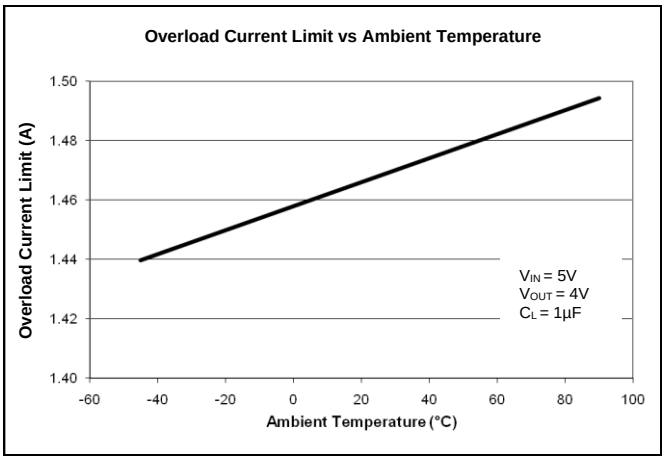


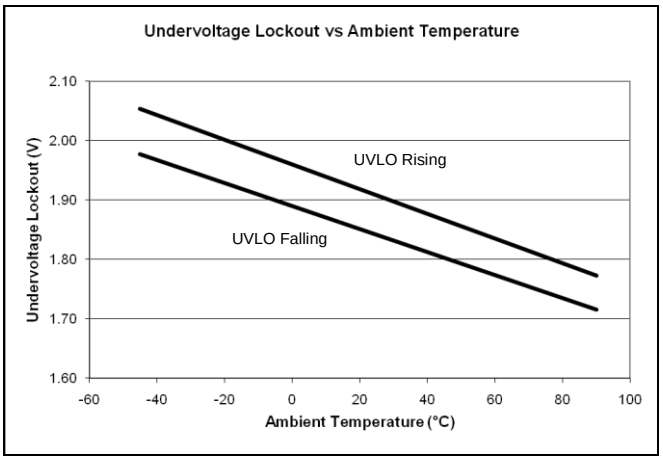


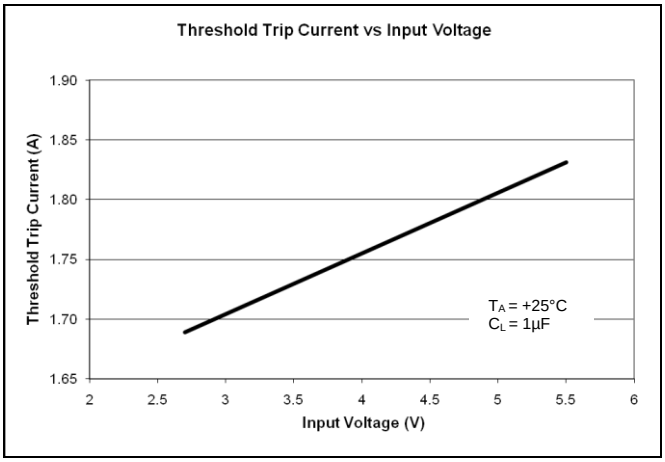
Typical Performance Characteristics (continued)

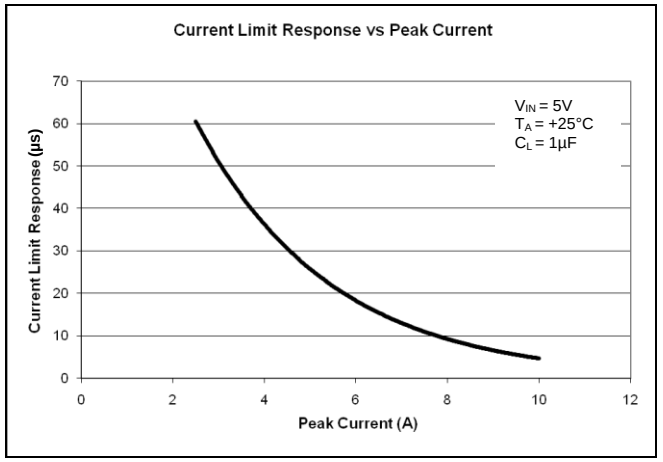












Application Information

Power Supply Considerations

A 0.1µF to 1µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Overcurrent and Short-Circuit Protection

An internal sensing FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before V_{IN} has been applied. The AP2162A/AP2172A senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT}.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher inrush current may flow for a very short period of time before the current limit function can react. The input capacitor(s) rapidly discharge through the device, activating current limit circuitry. Protection is achieved by momentarily opening the pMOS high-side power switch and then gradually turning it on. After the current limit function has tripped (reached the overcurrent trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT}. The threshold for activating current limiting is 1.4A typical per channel.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIG}) is reached or until the thermal limit of the device is exceeded. The AP2162A/AP2172A is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current-limit mode and is set at I_{LIMIT}.

FLG Response

When an overcurrent or overtemperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7ms deglitch timeout. The FLG output remains low until both overcurrent and overtemperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary overcurrent condition, which does not trigger the FLG due to the 7ms deglitch timeout. The AP2162A/AP2172A is designed to eliminate false overcurrent reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2162A/AP2172A implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an overcurrent or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately +25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an overtemperature shutdown or overcurrent occurs with 7ms deglitch.

Application Information (continued)

Undervoltage Lockout (UVLO)

Undervoltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Discharge Function

The discharge function of the device is active when enable is disabled or deasserted. The discharge function with the nMOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

Host/Self-Powered Hubs

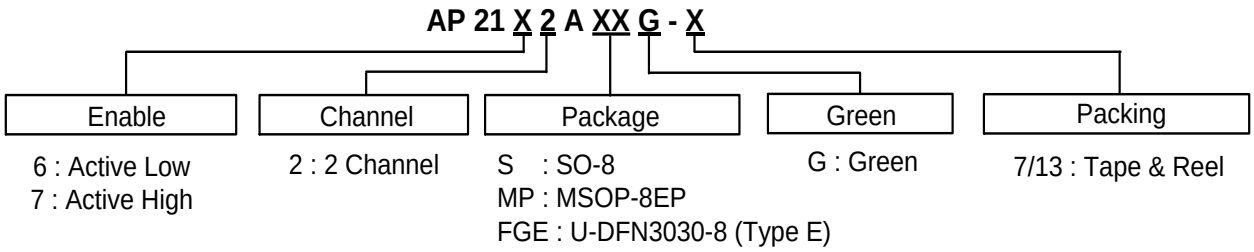
Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports. This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2162A/AP2172A, these devices can be used to provide a softer startup to devices being hot-plugged into a powered system. The UVLO feature of the AP2162A/AP2172A also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2162A/AP2172A between the VCC input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

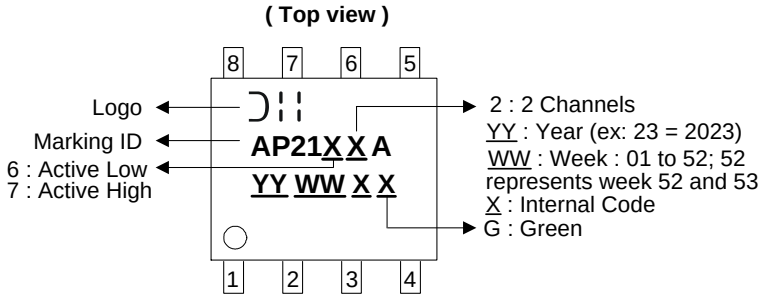
Ordering Information



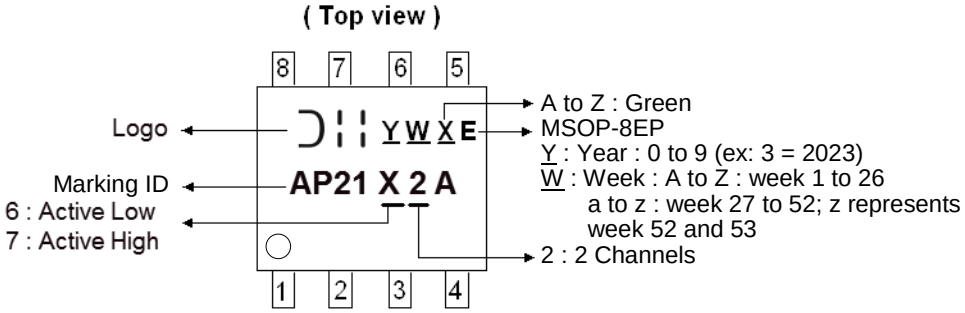
Part Number	Part Number Suffix	Package Code	Package	Packing	
				Qty.	Carrier
AP21X2ASG-13	-13	S	SO-8	250	13” Tape & Reel
AP21X2AMPG-13	-13	MP	MSOP-8EP	2500	13” Tape & Reel
AP21X2AFGEG-7	-7	FGE	U-DFN3030-8 (Type E)	3000	7” Tape & Reel

Marking Information

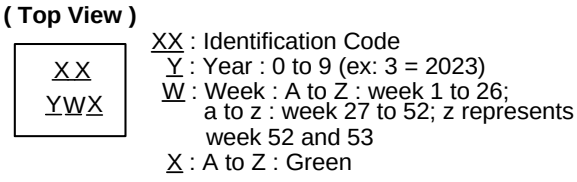
(1) SO-8



(2) MSOP-8EP



(3) U-DFN3030-8 (Type E)

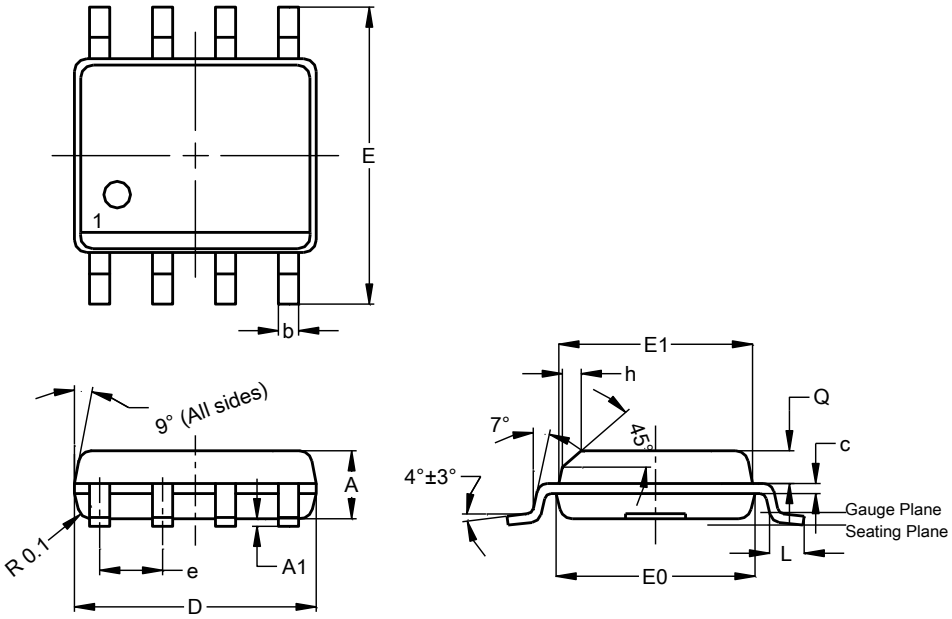


Part Number	Package	Identification Code
AP2162AFGEG-7	U-DFN3030-8 (Type E)	AC
AP2172AFGEG-7	U-DFN3030-8 (Type E)	AD

Package Outline Dimensions

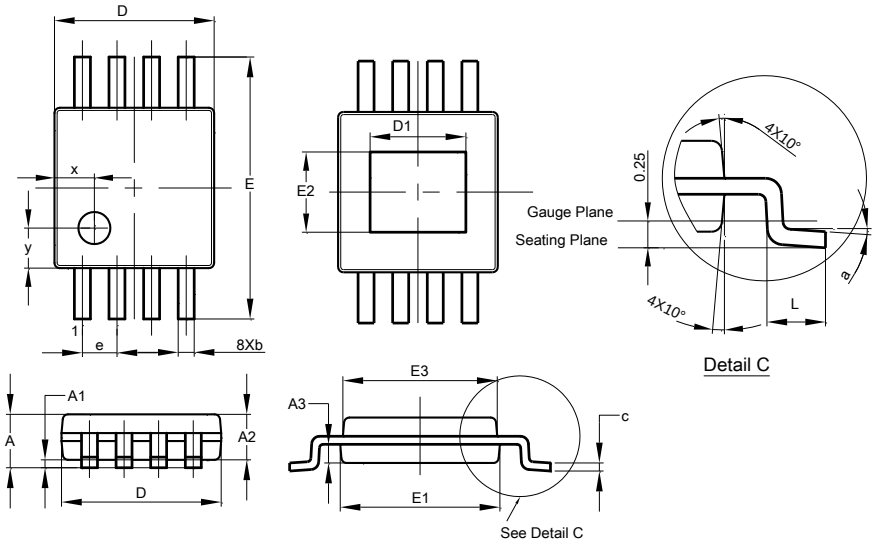
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

(2) Package Type: MSOP-8EP

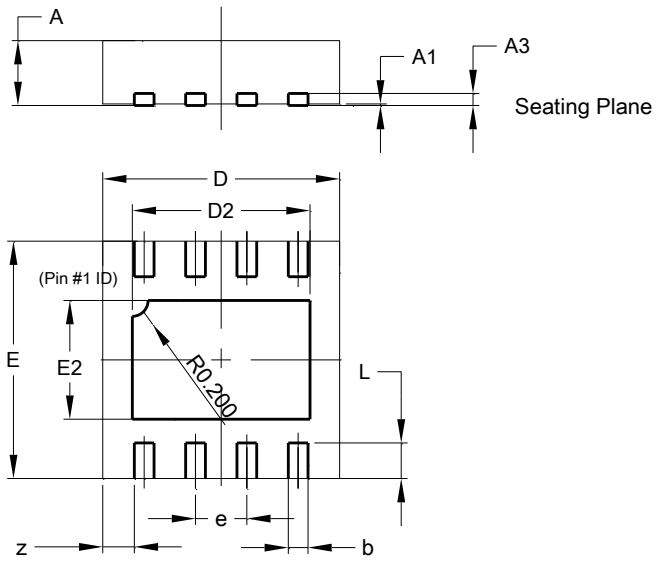


MSOP-8EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

Package Outline Dimensions (continued)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(3) Package Type: U-DFN3030-8 (Type E)

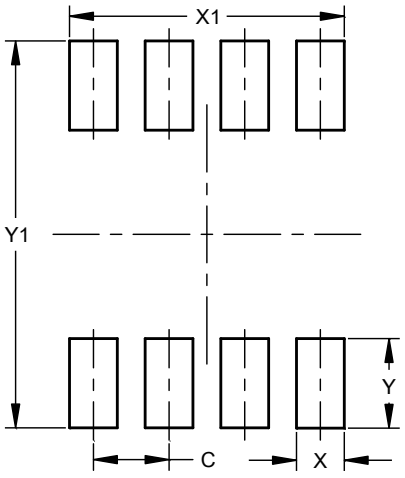


U-DFN3030-8 (Type E)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.65
L	0.30	0.60	0.45
z	-	-	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8

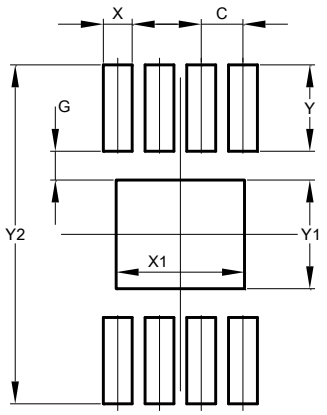


Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

Suggested Pad Layout (continued)

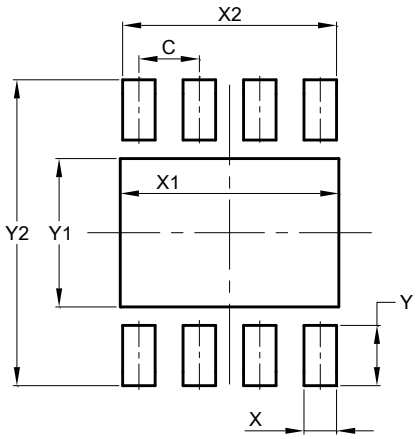
Please see http://www.diodes.com/package-outlines.html for the latest version.

(2) Package Type: MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

(3) Package Type: U-DFN3030-8 (Type E)



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	2.350
X2	2.300
Y	0.650
Y1	1.600
Y2	3.300

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals:
  - SO-8: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
  - MSOP-8EP: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
  - U-DFN3030-8 (Type E): Finish – NiPdAu Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight:
  - SO-8: 0.077 grams (Approximate)
  - MSOP-8EP: 0.026 grams (Approximate)
  - U-DFN3030-8 (Type E): 0.018 grams (Approximate)

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