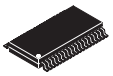


SLUS571 − SEPTEMBER 2003

# DUAL CHANNEL, SYNCHRONOUS STEP-DOWN PWM CONTROLLER

## FEATURES

- **High Efficiency − No Current Sense Resistor Required, $R_{DS(on)}$ Overcurrent Detection with Temperature Compensation**
- **Adjustable Output Voltage Down to 0.9 V**
- **Voltage-Mode PWM Control: Maximum 500-kHz Operation**
- **180° Out-of-Phase Control**
- **Individual Standby and Soft-Start for Each Channel − Easy Power Sequencing**
- **Overvoltage and Undervoltage Protection**
- **Built-In Boot-Strap Diode**
- **Built-In 5-V Linear Regulator**
- **Accurate ± 1% 0.85-V Reference**

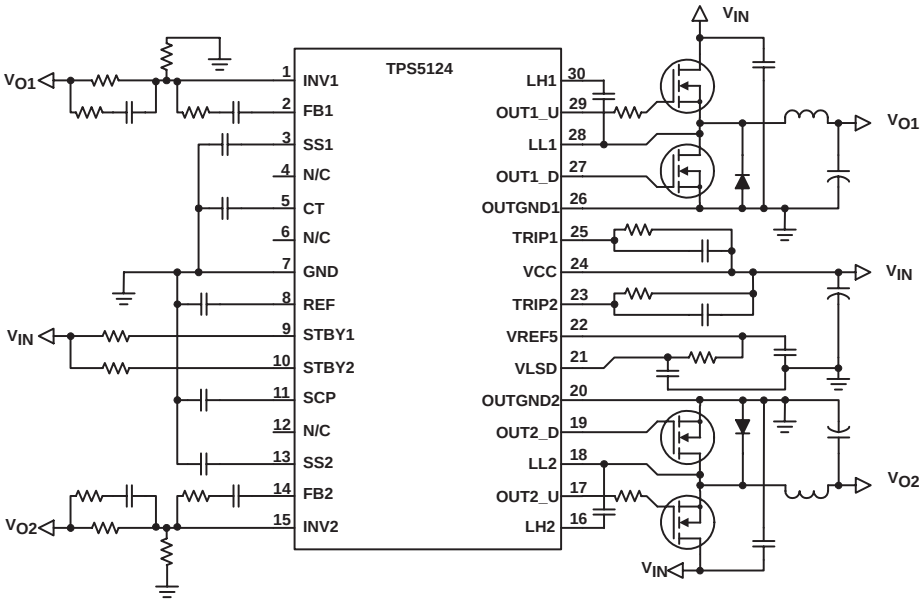
## APPLICATIONS

- **Consumer Game Systems**
- **DSP Applications**
- **Digital Set-Top Box**
- **VGA and Sound Cards**

## DESCRIPTION

The TPS5124 is dual independent high efficiency synchronous step-down controller. It supports a low-voltage/high-current power supply applica−tions that use either a 5-V or 12-V bus voltage. Since both controllers of the TPS5124 operate 180 degree out-of-phase, the input current ripple is minimized resulting in a smaller input capacitance and reduced power supply cost.

The current protection circuit detects the drain-to-source voltage drop across the high-side and low-side power MOSFET while it is conducting. Also, the current protection circuit has a temperature coefficient to compensate for the $R_{DS(on)}$ variation of the MOSFET. This resistor-less current protection and built-in boot diode simplify the system design and reduces the external parts count. Other features such as undervoltage lockout, overvoltage, undervoltage, and programmable short-circuit protection promote system reliability.




UDG−03123

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS

−40°C ≤ $T_A$ ≤ 85°C, all voltage values are with respect to the network ground terminal unless otherwise noted. (1)

| | | TPS5124 | UNIT |
|---|---|---|---|
| Input voltage range | VCC, STBY1, STBY2, TRIP1, TRIP2 | −0.3 to 16 | V |
| | LH1, LH2 wrt GND | −0.3 to 22 | |
| | LH1, LH2 (wrt the corresponding LL terminal) | −0.3 to 6 | |
| | SS1, SS2, CT, INV1, INV2, SCP, VLSD | −0.3 to 6 | |
| Ouput voltage range | OUT1_U, OUT2_U | −1 to 22 | |
| | OUT1_U, OUT2_U (wrt the corresponding LL terminal) | −0.3 to 6 | |
| | LL1, LL2 | −1 to 16 | |
| | OUT1_D, OUT2_D, VREF5, FB1, FB2 | −0.3 to 6 | |
| | OUTGND1, OUTGND2 | −0.3 to 0.3 | |
| | REF | −0.3 to 3 | |
| Output current range | VREF5 | 50 | mA |
| | VREF | 5 | |
| Operating free-air temperature range, $T_A$ | | −40 to 85 | °C |
| Storage temperature range, $T_{stg}$ | | −55 to 150 | |
| Junction temperature range, $T_J$ | | −40 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 6.5 | | 15 | V |
| | (when VLSD is connected to VCC) | 4.5 | | 5.5 | |
| Input voltage range | INV1, INV2, CT, SS1, SS2, SCP, FB1, FB2, OUT1_D, OUT2_D, VLSD | −0.1 | | 5.9 | |
| | OUT1_U, OUT2_U, LH1, LH2 | −0.1 | | 21 | |
| | TRIP1, TRIP2, LL1, LL2, STBY1, STBY2 | −0.1 | | 15 | |
| Operating frequency, $f_{OSC}$ | | | 300 | 500 | kHz |
| Operating free-air temperature range, $T_A$ | | −40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

$T_J$ = −40°C to 85°C, $V_{CC}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{CC}$ | Supply current | $T_A$ = 25°C, $V_{CT}$ = $V_{INV1}$=$V_{INV2}$ = 0 V | | 1.1 | 1.5 | mA |
| $I_{CCS}$ | $V_{IN}$ standby current | $V_{STBY1}$ = $V_{STBY2}$ = 0 V | | 0.1 | 10.0 | μA |
| **5-V REGULATOR** | | | | | | |
| $V_{VREF5}$ | Output voltage | $T_A$ = 25°C, 7.5 V ≤ $V_{CC}$ ≤ 15 V, 0 mA ≤ $I_O$ ≤ 10 mA | 4.8 | 5.0 | 5.2 | V |
| $V_{LN5}$ | Line regulation | 7.5 V ≤ $V_{CC}$ ≤ 15 V, $I_O$ =10 mA | | | 20 | mV |
| $V_{LD5}$ | Load regulation | 1 mA ≤ $I_O$ ≤ 10 mA | | | 40 | |
| $I_{OS}$ | Short-circuit output current | $V_{REF5}$ = 0 V, $T_A$ = 25°C | 65 | | | mA |
| $V_{THH}$ | UVLO threshold voltage | high-to-low | 3.6 | | 4.2 | V |
| $V_{THL}$ | | low-to-high | 3.5 | | 4.1 | V |
| $V_{HYS}$ | Hysteresis | | 30 | | 150 | mV |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference voltage | | | 0.85 | | V |
| $V_{REF(tol)}$ | Reference voltage tolerance | $I_{REF}$ = 50 μA, $T_A$ = 25°C | -0.5% | | 0.5% | |
| $V_{REF(ln)}$ | Line regulation | 6.5 V ≤ $V_{CC}$ ≤ 15 V, $I_{REF}$ = 50 μA | | 0.03 | 3.00 | mV |
| $V_{REF(ld)}$ | Load regulation | 0.1 μA ≤ $I_{REF}$ ≤ 1 mA | | 0.15 | 5.00 | |
| **CONTROL** | | | | | | |
| $V_{IH}$ | High-level input voltage | STBY1, STBY2 | 2.2 | | | V |
| $V_{IL}$ | Low-level input voltage | STBY1, STBY2 | | | 0.3 | |
| **OUTPUT VOLTAGE MONITOR** | | | | | | |
| | OVP comparator threshold voltage | | 0.90 | 0.95 | 1.00 | V |
| | UVP comparator threshold voltage | | 0.58 | 0.66 | 0.74 | |
| | Timer latch current source | Overvoltage protection | −4 | −8 | −12 | μA |
| | | Undervoltage protection | −1 | −1.7 | −2.3 | |
| **OSCILLATOR** | | | | | | |
| $f_{OSC}$ | Frequency | $C_T$ = 47 pF, $T_A$ = 25°C | | 300 | | kHz |
| $V_{OSC(h)}$ | High-level output voltage | DC | 1.0 | 1.1 | 1.2 | V |
| | | $f_{OSC}$ = 300 kHz | | 1.14 | | |
| $V_{OSC(l)}$ | Low-level output voltage | DC | 0.4 | 0.5 | 0.6 | |
| | | $f_{OSC}$ = 300 kHz | | 0.46 | | |
| **ERROR AMPLIFIER** | | | | | | |
| $V_{IO}$ | Input offset voltage | $T_A$ = 25°C | | 2 | 10 | mV |
| | Open-loop voltage gain | | 50 | | | dB |
| | Unity gain bandwidth | | | 2.5 | | MHz |
| $I_{SINK}$ | Output sink current | $V_O$ = 2.5 V | 2 | 4 | | mA |
| $I_{SRC}$ | Output source current | $V_O$ = 2.5 V | −2 | −4 | | |
| **DUTY CONTROL** | | | | | | |
| | Maximum duty cycle | $f_{OSC}$ = 300 kHz, $V_{(INV1)}$ = $V_{(INV2)}$ = 0 V | | 80% | | |

## ELECTRICAL CHARACTERISTICS(continued)

$T_J$ = −40°C to 85°C, $V_{CC}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT DRIVER** | | | | | | |
| | OUT_U sink current | $V_{(OUTx\_U)} - V_{(LLx)}$ = 3 V | | 1.2 | | A |
| | OUT_U source current | $V_{(LHx)} - V_{(OUTx\_U)}$ = 3 V | | −1.2 | | |
| | OUT_D sink current | $V_{(OUTx\_D)}$ = 3 V | | 1.5 | | |
| | OUT_D source current | $V_{(OUTx\_D)}$ = 2 V | | −1.5 | | |
| **SOFT START** | | | | | | |
| $I_{SOFT}$ | Soft-start current | | −1.3 | −2.3 | −2.9 | µA |
| **CURRENT PROTECTION** | | | | | | |
| $I_{TRIP}$ | TRIP current | $T_A$ = 25°C | 11 | 13 | 15 | µA |
| TC | TRIP current temperature coefficient | $T_A$ = 25°C | | 3400 | | ppm/°C |

## AVAILABLE OPTIONS

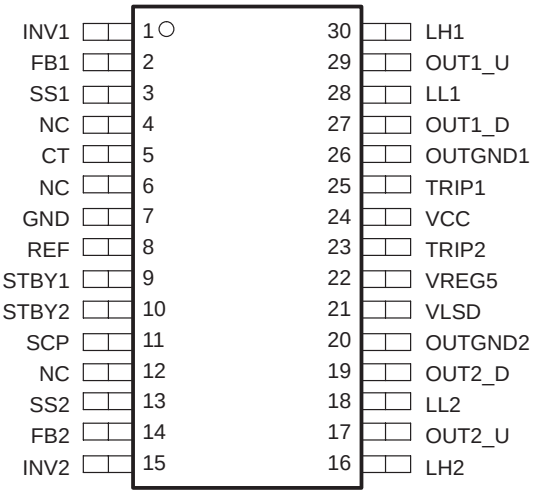
| $T_A$ | PACKAGED DEVICES(1) |
|---|---|
| | PLASTIC TSSOP (DBT) |
| −40°C to 85°C | TPS5124DBT |

(1) The DBT package is available taped and reeled. Add an R suffix to the device type (e.g. TPS5124DBTR) to order quantities of 2,000 devices per reel.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING |
|---|---|---|---|
| 30-pin DBT | 874 mW | 7.0 mW/°C | 454 mW |

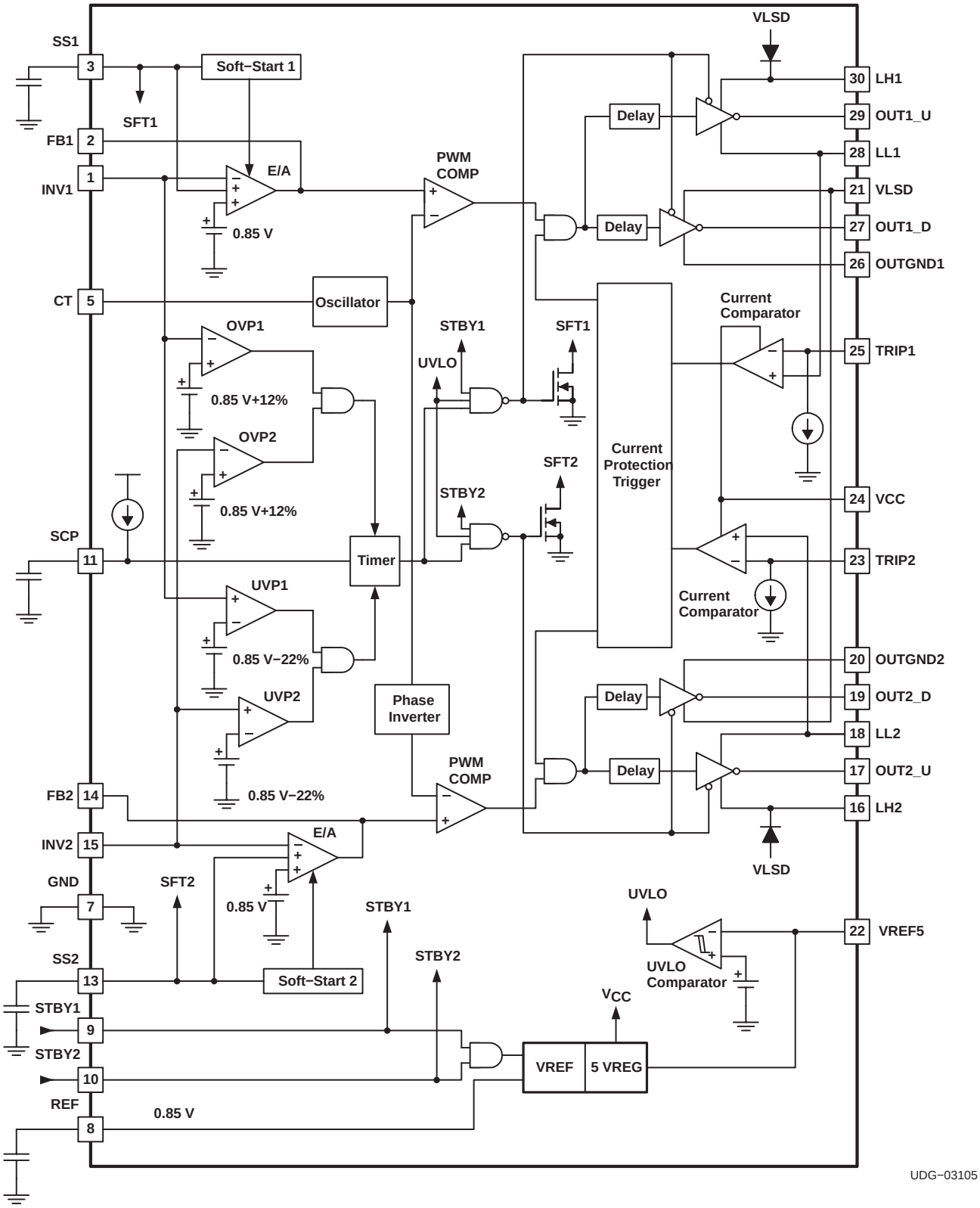
**DBT PACKAGE**
**(TOP VIEW)**



## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CT | 5 | I/O | External capacitor from CT to GND adjusts frequency of the triangle oscillator. |
| FB1 | 2 | O | Feedback output of SBRC−Channel 1 error amplifier. |
| FB2 | 14 | O | Feedback output of SBRC−Channel 2 error amplifier. |
| GND | 7 | − | Signal GND. |
| INV1 | 1 | I | Inverting inputs of Channel 1 error amplifier and OVP1/UVP1 comparator. |
| INV2 | 15 | I | Inverting inputs of Channel 2 error amplifier and OVP2/UVP2 comparator. |
| LH1 | 30 | I/O | Bootstrap capacitor connection for Channel 1 high-side gate driver. |
| LH2 | 16 | I/O | Bootstrap capacitor connection for Channel 2 high-side gate driver. |
| LL1 | 28 | I/O | CH1 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator. |
| LL2 | 18 | I/O | CH2 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator. |
| NC | 4,6,12 | − | No connection. |
| OUT1_D | 27 | O | Gate drive output for Channel 1 low-side MOSFETs. |
| OUT2_D | 19 | O | Gate drive output for Channel 2 low-side MOSFETs. |
| OUT1_U | 29 | O | Gate drive output for Channel 1 high-side MOSFETs. |
| OUT2_U | 17 | O | Gate drive output for Channel 2 high-side MOSFETs. |
| OUTGND1 | 26 | − | Ground for Channel 1 MOSFET drivers. |
| OUTGND2 | 20 | − | Ground for Channel 2 MOSFET drivers. |
| REF | 8 | O | 0.85-V reference voltage output. This 0.85-V reference voltage is used to set the output voltage and the reference for the overvoltage and undervoltage protections. This reference voltage is dropped down from the internal 5-V regulator. |
| SCP | 11 | I/O | Fault latch timer pin. An external capacitor connected between SCP and GND sets SCP enable time up. |
| SS1 | 3 | I/O | Soft start control for Channel 1. Connect an external capacitor between this pin and GND to specify SOFT-START time. |
| SS2 | 13 | I/O | Soft start control for Channel 2. Connect an external capacitor between this pin and GND to specify SOFT-START time. |
| STBY1 | 9 | I | Standby control input for Channel 1. It can be switched into standby mode by grounding the STBY1 pin. |
| STBY2 | 10 | I | Standby control input for Channel 2. It can be switched into standby mode by grounding the STBY2 pin. |
| TRIP1 | 25 | I | External resistor connection for Channel 1 output current protection control. |
| TRIP2 | 23 | I | External resistor connection for Channel 2 output current protection control. |
| VCC | 24 | I | Supply voltage input |
| VLSD | 21 | I | Supply voltage input for low side driver. Typically connected to VREF5 with R-C filter when $V_{VCC}$ is between 6.5V and 15V and connected to VCC with filter when $V_{VCC}$ is between 4.5 V and 5.5 V. |
| VREF5 | 22 | O | 5V linear regulator output. When $V_{VCC}$ is between 4.5V and 5.5V should be connected to VCC. |

## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### INPUT VOLTAGE RANGE

TPS5124 supports two input voltage ranges. When $V_{VCC}$ is between 6.5 V and 15 V, VLSD is connected to VREF5 with R-C filter (see Figure 1). When $V_{VCC}$ is between 4.5 V and 5.5 V, VLSD is connected to VCC with R-C filter and VREF5 is connected to VCC. (see Figure2).

### REFERENCE VOLTAGE (0.85 V)

This 0.85-V reference voltage is used to set the output voltage and the reference for the overvoltage and undervoltage protections. This reference voltage is dropped down from the internal 5V regulator.

### PWM OPERATION

TPS5124 includes dual synchronous buck regulator controllers (SBRC) that operate 180° out of phase and same frequency. Both channels have individual standby and softstart controller.

### 5-V REGULATOR

An internal linear voltage regulator is used for the reference voltage and power supply of internal circuit. When this regulator is connected to the VLSD pin, it is used for powering the low-side driver and powering the high-side driver through the built-in bootstrap diode or external bootstrap circuit. It is active if either STBY1 or STBY2 is HIGH and has a tolerance of 4 %.

### ERROR AMPLIFIER

Each channel has its own error amplifier to regulate the output voltage of the synchronous buck converter. The unity gain bandwidth is 2.5 MHz. This decreases the amplifier delay during fast load transients and contributes to a fast transient response.

### LOW-SIDE DRIVER

The low-side driver is designed to drive high current and low $R_{DS(on)}$ N-channel MOSFET(s). The maximum drive voltage is 5 V from the VLSD pin. The current rating of the driver is typically 1.5 A at source and sink.

### HIGH-SIDE DRIVER

The high-side driver is designed to drive high current and low $R_{DS(on)}$ N−channel MOSFET(s). The current rating of the driver is 1.2 A (typ.) at source and sink. When configured as a floating driver a bias voltage is delivered from the VSLD pin through built-in bootstrap diode or external bootstrap circuit. When the MOSFET needs high gate threshold voltage, it is useful to add the external schottky diodes which provide a higher voltage for the gate drive than using the built-in diodes. The instantaneous drive current is supplied by the flying capacitor between the LH and LL pins since a bias power supply does not usually have low impedance. The maximum voltage between the OUTx_U and LLx pins is about 5.5 V when the VSLD pin is connected to the VREF5 pin. The maximum voltage that can be applied between the LH and OUTGND pins is 22 V.

### DEAD-TIME

The internally defined dead-time prevents shoot-through current flowing through the main power MOSFETs during switching transitions.

## FUNCTIONAL DESCRIPTION

### OVER CURRENT PROTECTION (OCP)

Over current protection (OCP) is achieved by comparing the drain-to-source voltage of the high-side and low-side MOSFET to a set-point voltage, which is defined by both the internal current source, $I_{TRIP}$, and the external resistor connected between the VCC and TRIP pins. $I_{TRIP}$ has a typical value of 13 μA at 25°C. When the low-side MOSFET's drain-to-source voltage exceeds the set-point voltage during low-side conduction, the high-side current comparator becomes active, and the low-side on pulse is extended until this voltage comes back below the threshold. If the set-point voltage is exceeded during high-side conduction in the following cycle, the current limit circuit terminates the high-side driver pulse. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated to latch both the high-side and low-side drivers OFF. In the TPS5124, trip current ($I_{TRIP}$) has a temperature coefficient of 3400 ppm/°C in order to compensate for temperature drift of the MOSFET on-resistance.

### OVER VOLTAGE PROTECTION (OVP)

For over voltage protection (OVP), the TPS5124 monitors the INV pin voltage. When the INV pin voltage is higher than 0.95 V (0.85 V +12%), the OVP comparator output goes low and the SCP timer starts to charge an external capacitor connected to SCP pin. After a set time, the SCP circuit latches the high-side MOSFET driver to OFF state and low-side MOSFET drivers to ON state. The timer source current for the OVP latch is 8 μA(typ.), and the time−up voltage is 1.185 V (typ.). The OVP timer is designed to be five times faster than the under voltage protection timer described below.

### UNDER VOLTAGE PROTECTION (UVP)

For under voltage protection (UVP), the TPS5124 monitors the INV pin voltage. When the INV pin voltage is lower than 0.66 V (0.85 V – 22%), the UVP comparator output goes low, and the SCP timer starts to charge the external capacitor connected to SCP pin. Also, when the current comparator triggers the OCP, the UVP comparator detects the under voltage output and starts the SCP capacitor charge, too. After a set time, the SCP circuit latches both of the MOSFET drivers to the OFF state. The timer latch source current for UVP is 1.6 μA (typ.), and the time-up voltage is also 1.185 V (typ.).

### SCP (TIMER)

When an OVP or UVP comparator output goes low, the SCP circuit starts to charge the SCP capacitor. If the SCP pin voltage goes beyond a constant level, the TPS5124 latches the MOSFET drivers. At this time, the state of MOSFET is different depending on the OVP alert and the UVP alert. The enable time used to latch the MOSFET drivers is decided by the value of the SCP capacitor. The charging constant current value depends on whether it is an OVP alert or a UVP alert as shown in the following equation:

$$I_{SCP(ovp)} = I_{SCP(uvp)} \times 5 \quad (1)$$

### SOFT START

Soft-start ramp up of the SBRC is controlled by the SSx pin voltage. After the STBY pin is raised to a HIGH level, an internal current source charges up an external capacitor connected between the SSx and GND pins. The soft-start time is easily calculated by the supply current and the capacitance value.

## FUNCTIONAL DESCRIPTION

### STANDBY

The SBRC controller can be switched into standby mode separately by grounding STBY pin.

**Table 1. Standby Logic**

| STBY1 | STBY2 | SBRC (CH1) | SBRC (CH2) | 5-V REGULATOR |
|---|---|---|---|---|
| L | L | DISABLED | DISABLED | DISABLED |
| L | H | DISABLED | ENABLED | ENABLED |
| H | L | ENABLED | DISABLED | ENABLED |
| H | H | ENABLED | ENABLED | ENABLED |

### UNDERVOLTAGE LOCK OUT (UVLO)

For undervoltage lock out (UVLO), the TPS5124 monitors VREF5 voltage. When the VREF5 voltage decreases below about 4.1 V, the output stages of both SBRC are turned off. This state is not latched and the operation recovers immediately after the input voltage becomes higher than about 4.2 V again. The typical hysteresis voltage is 40 mV.

### PHASE INVERTER

The SBRC (CH2) of the TPS5124 operates in the same phase as the internal triangular oscillator output while the SBRC (CH1) operates 180° out of phase. When the SBRC (CH1) and the SBRC (CH2) share the same input power supply, the TPS5124 reduces input current ripple and enables the input capacitor value smaller.

### OSCILLATOR

TPS5124 has a triangle oscillator generator internal to the device. The oscillation frequency is set by the size of the capacitor connected to the CT pin.

## APPLICATION INFORMATION

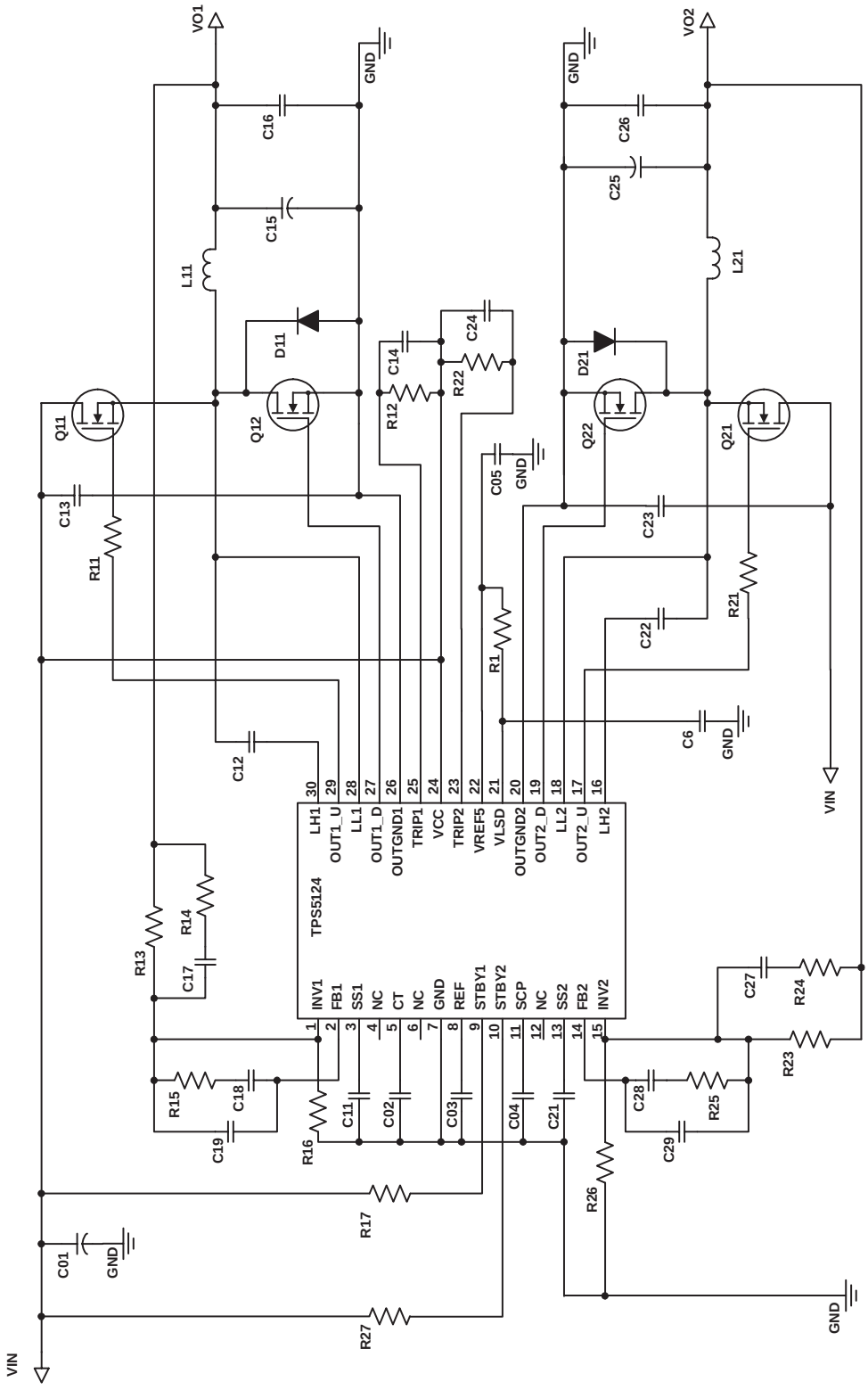



**Figure 1. Simplified Application Schematic ($V_{IN}$ = 12 V[typ])**

## APPLICATION INFORMATION

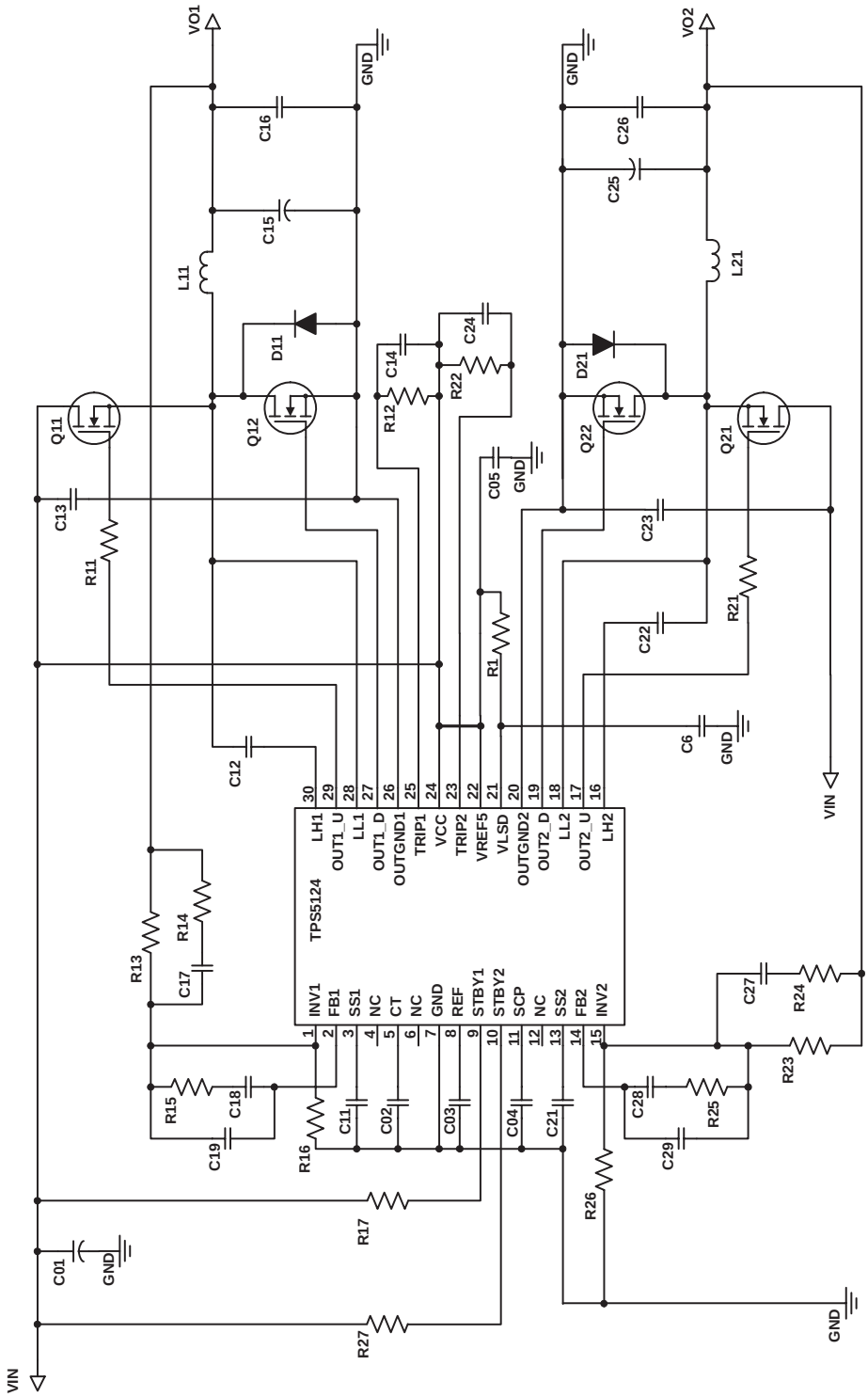



**Figure 2. Simplified Application Schematic ($V_{IN}$ = 5 V[typ])**

## APPLICATION INFORMATION

**SUPPLY CURRENT vs JUNCTION TEMPERATURE**

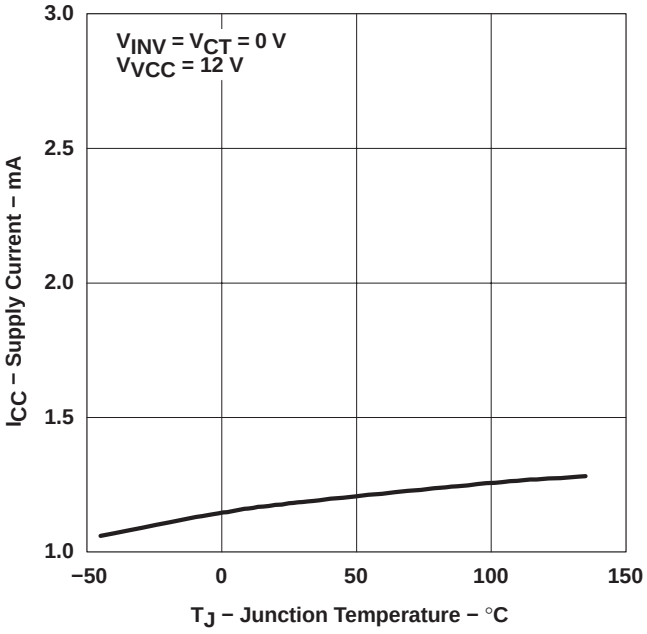



Figure 3

**SHUTDOWN SUPPLY CURRENT vs JUNCTION TEMPERATURE**

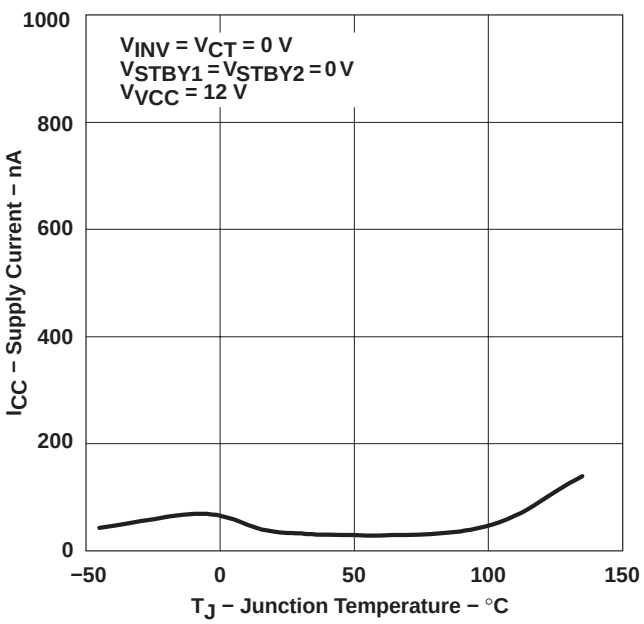



Figure 4

**SCP CURRENT vs JUNCTION TEMPERATURE**

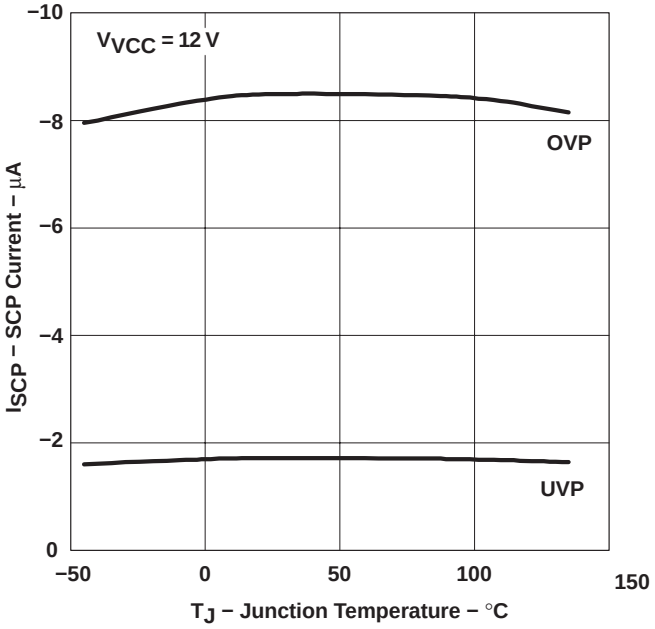



Figure 5

**TRIP CURRENT vs JUNCTION TEMPERATURE**

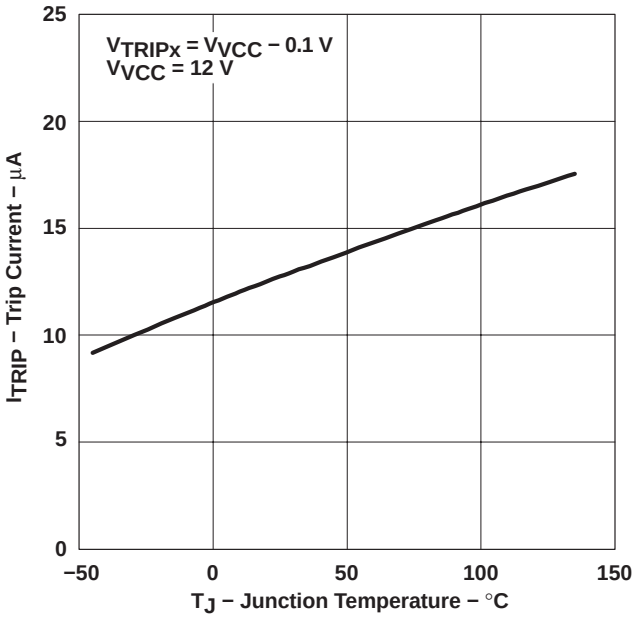



Figure 6

## APPLICATION INFORMATION

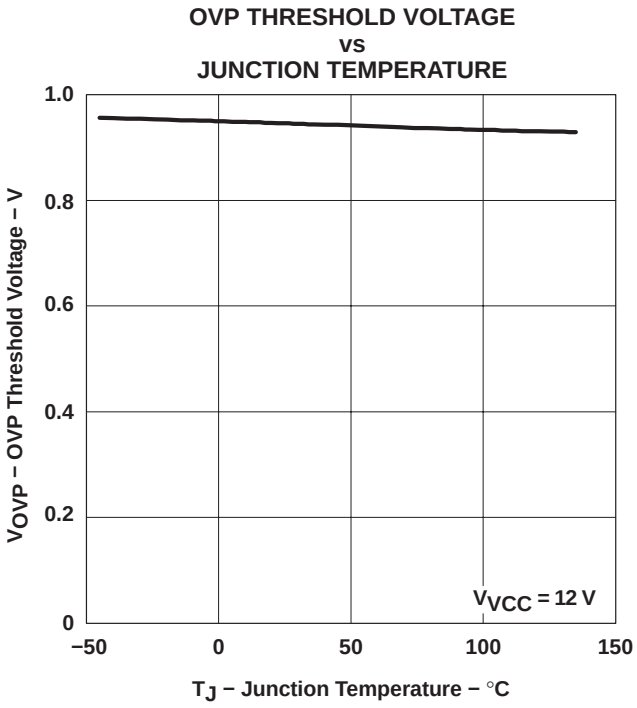



Figure 7

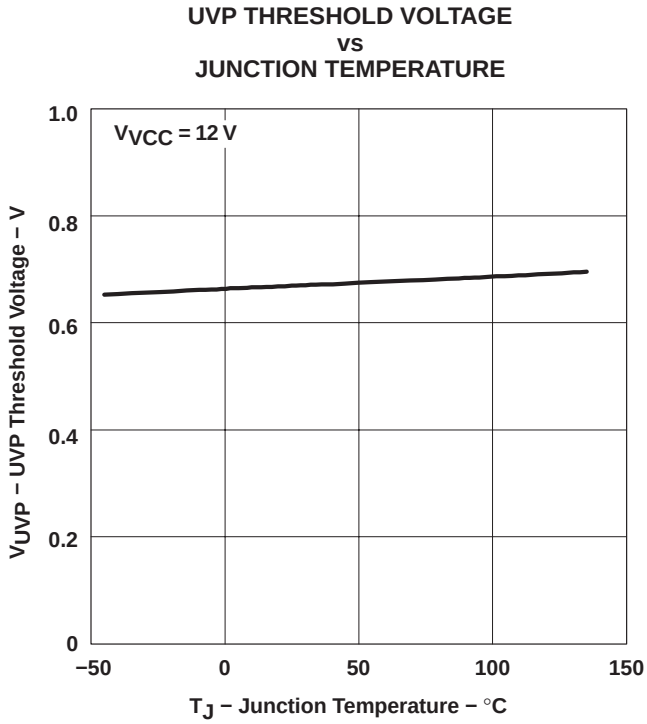



Figure 8

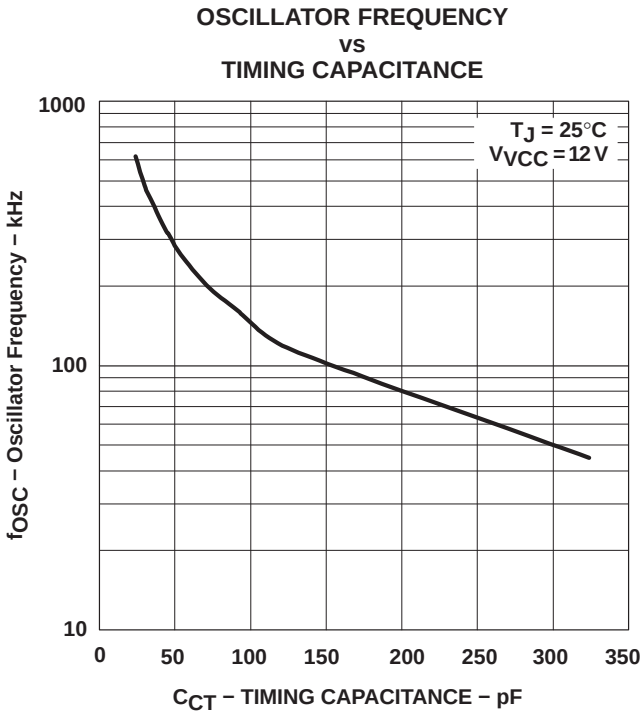



Figure 9

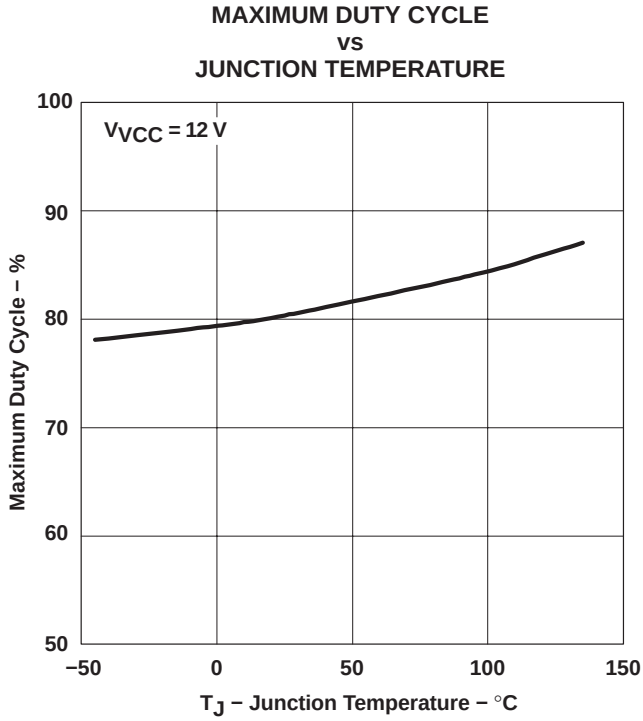



Figure 10

## APPLICATION INFORMATION

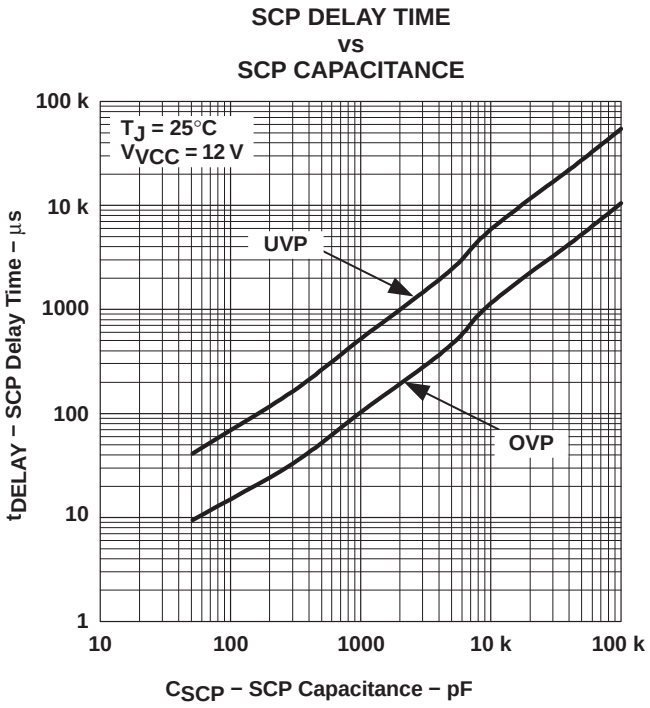



Figure 11

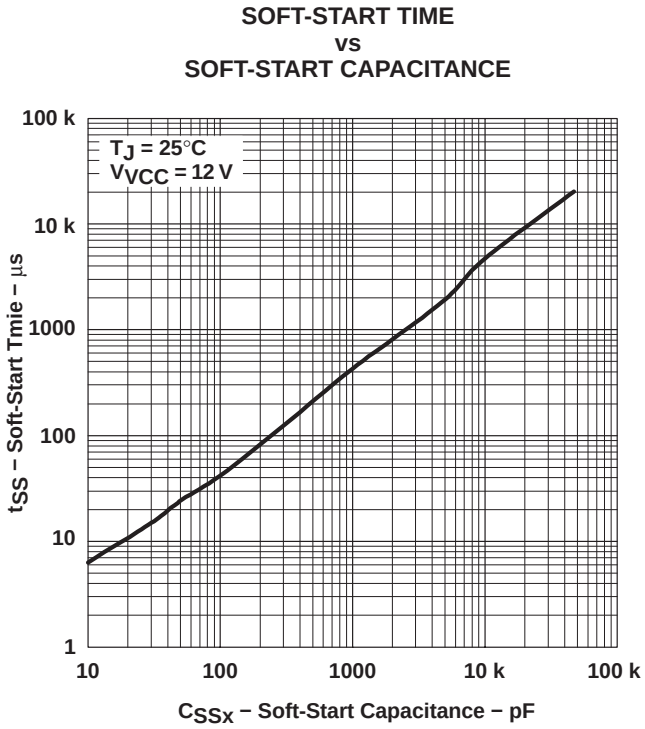



Figure 12

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS5124DBT | ACTIVE | TSSOP | DBT | 30 | 60 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS5124 | Samples |
| TPS5124DBTR | ACTIVE | TSSOP | DBT | 30 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS5124 | Samples |
| TPS5124DBTRG4 | ACTIVE | TSSOP | DBT | 30 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PS5124 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

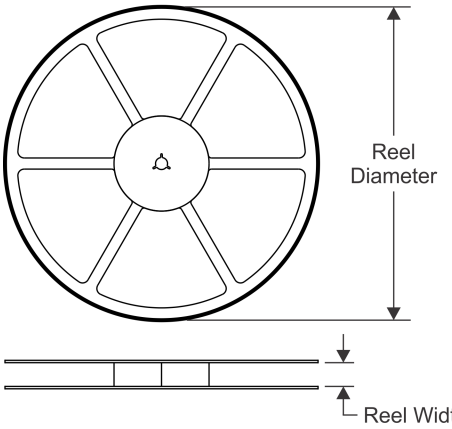
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

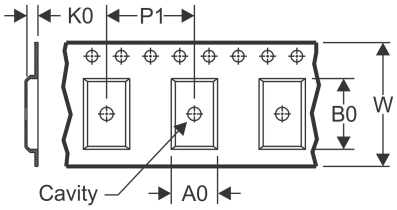
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

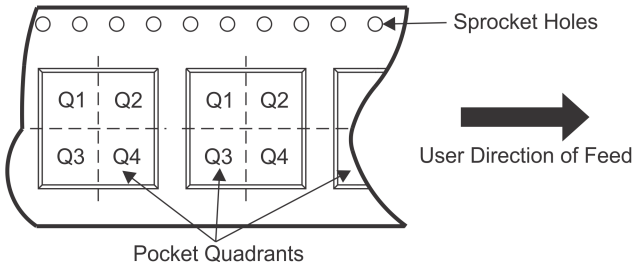



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

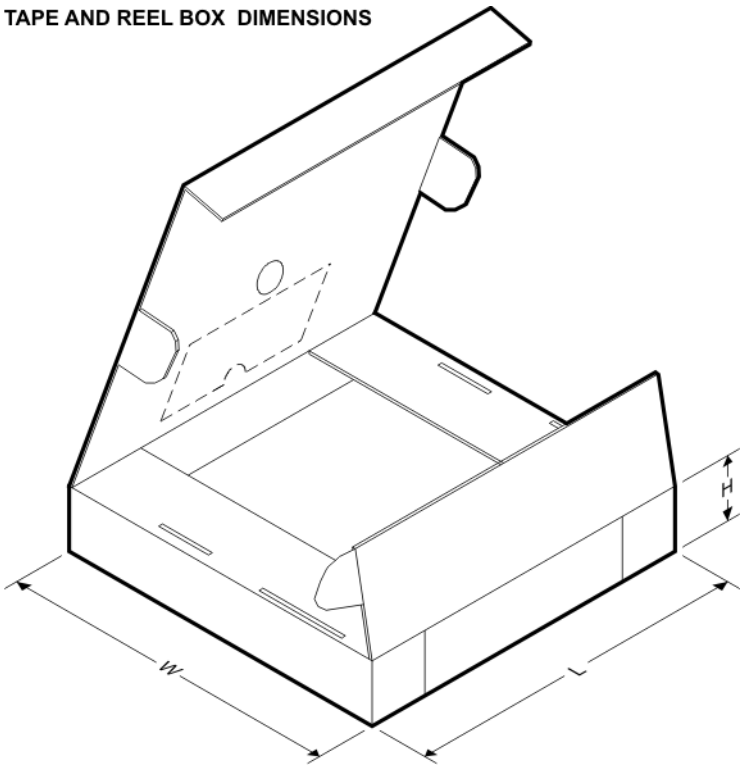
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS5124DBTR | TSSOP | DBT | 30 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

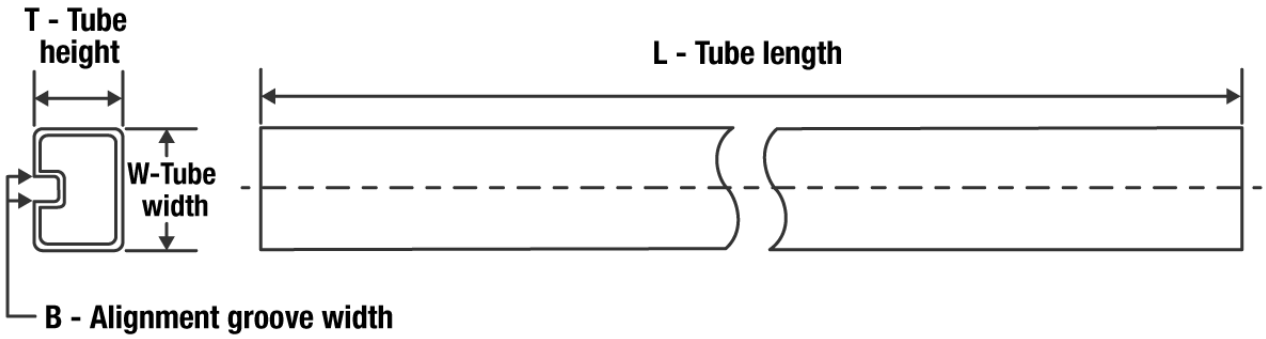
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS5124DBTR | TSSOP | DBT | 30 | 2000 | 367.0 | 367.0 | 38.0 |

## TUBE




*All dimensions are nominal

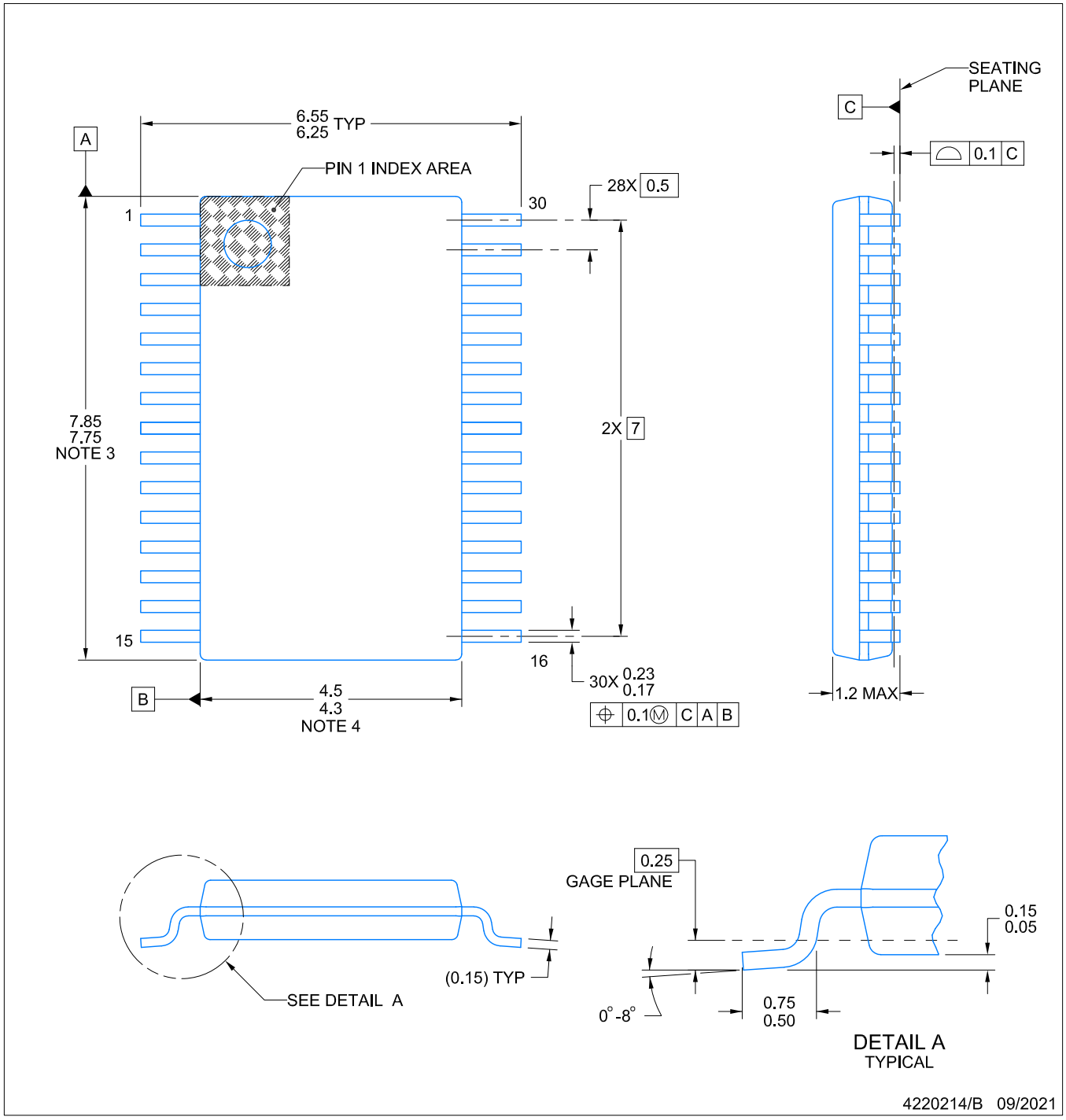
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS5124DBT | DBT | TSSOP | 30 | 60 | 530 | 10.2 | 3600 | 3.5 |

# PACKAGE OUTLINE

## DBT0030A

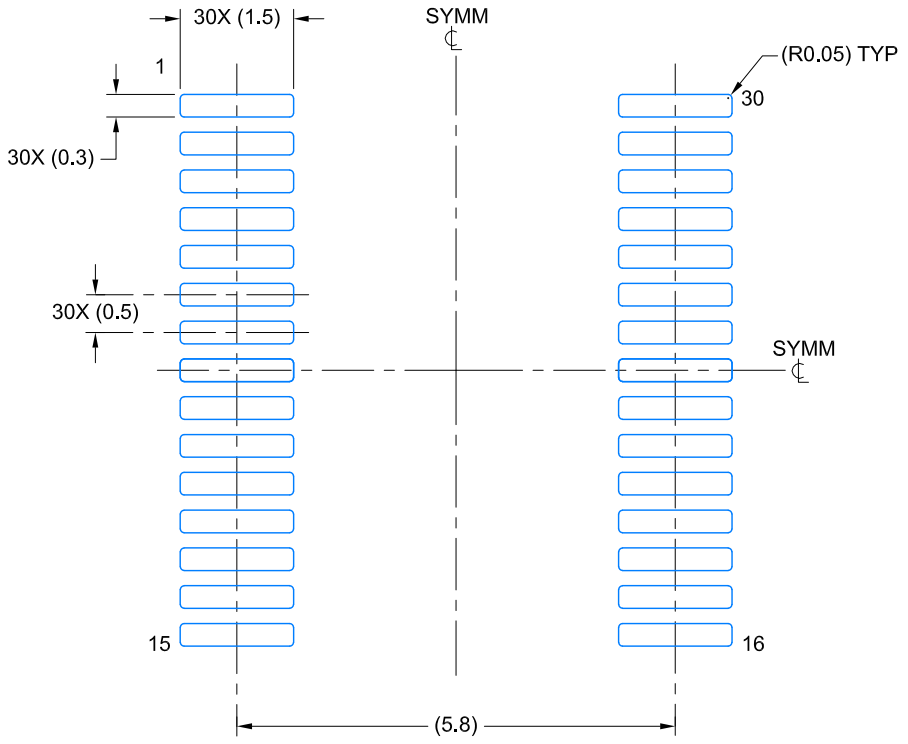
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

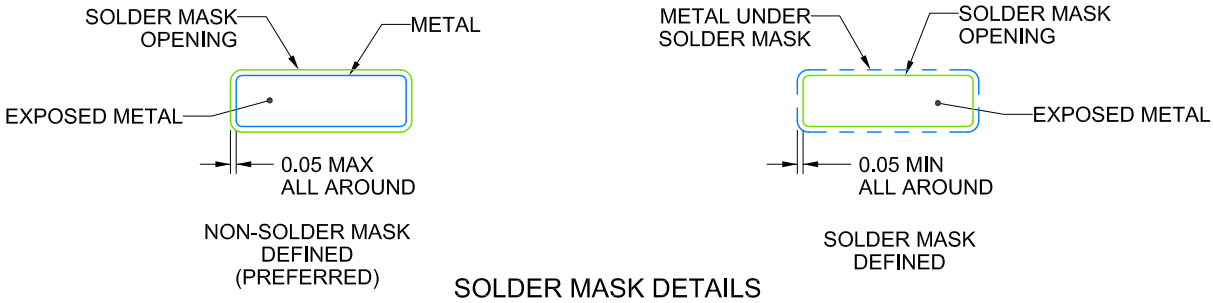



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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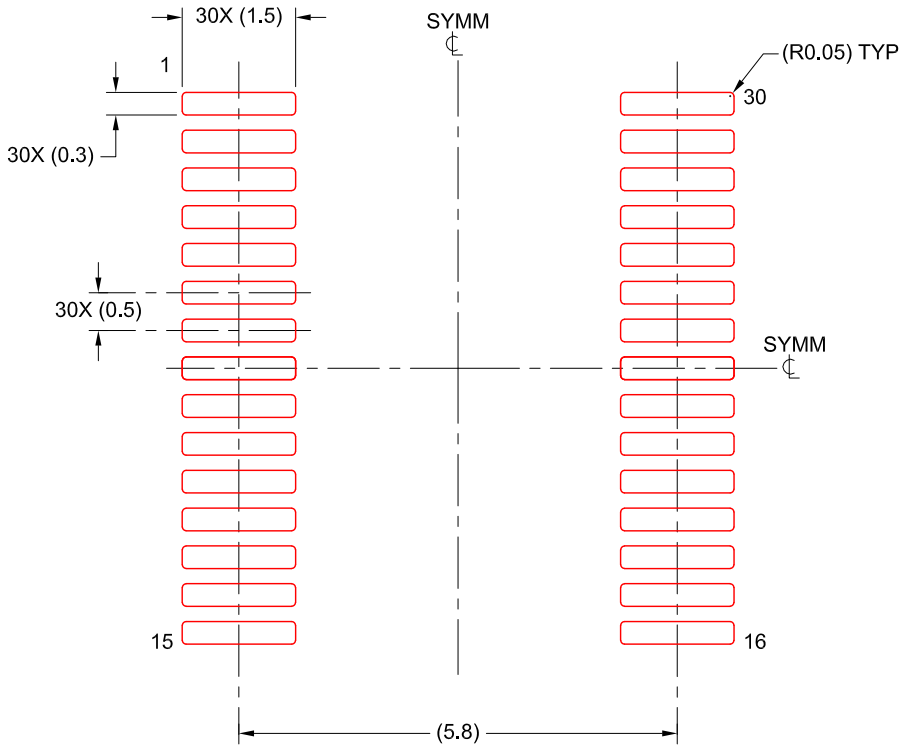
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265