

Single and Dual Low Voltage, Rail-to-Rail Input and Output, Operational Amplifiers

LMV931, LMV932

The LMV931 Single and LMV932 Dual are CMOS low-voltage operational amplifiers which can operate on single-sided power supplies (1.8 V to 5.0 V) with rail-to-rail input and output swing. Both devices come in small state-of-the-art packages and require very low quiescent current making them ideal for battery-operated, portable applications such as notebook computers and hand-held instruments. Rail-to-Rail operation provides improved signal-to-noise performance plus the small packages allow for closer placement to signal sources thereby reducing noise pickup.

The single LMV931 is offered in space saving SC70-5 package. The dual LMV932 is in either a Micro8 or SOIC package. These small packages are very beneficial for crowded PCB's.

Features

- Performance Specified on Single-Sided Power Supply: 1.8 V, 2.7 V, and 5 V
- Small Packages:
 - LMV931 in a SC-70
 - LMV932 in a Micro8 or SOIC-8
- No Output Crossover Distortion
- Extended Industrial Temperature Range: -40°C to +125°C
- Low Quiescent Current 210 μ A, Max Per Channel
- No Output Phase-Reversal from Overdriven Input
- These are Pb-Free Devices

Typical Applications

- Notebook Computers, Portable Battery-Operated Instruments, PDA's
- Active Filters, Low-Side Current Monitoring

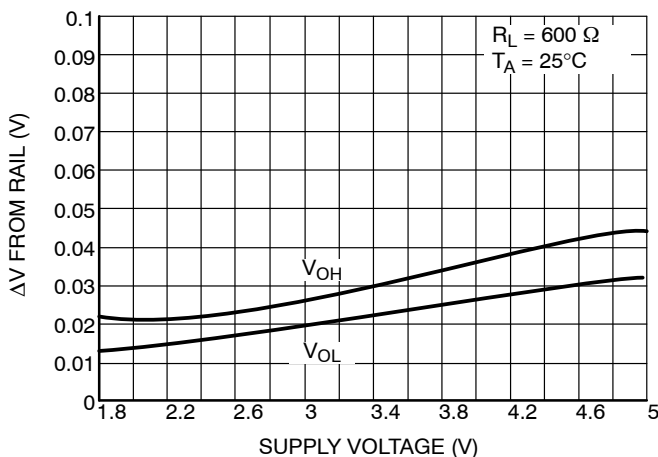
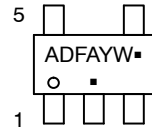
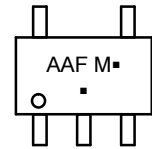


Figure 1. Output Voltage Swing vs. Supply Voltage

MARKING DIAGRAMS

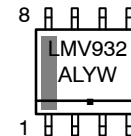
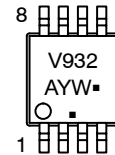
LMV931 (Single)



M = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

LMV932 (Dual)



A = Assembly Location
Y = Year
L = Wafer Lot
W = Work Week
▪ = Pb-Free Package

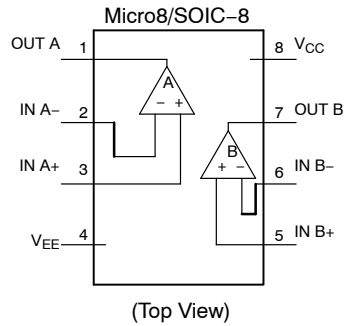
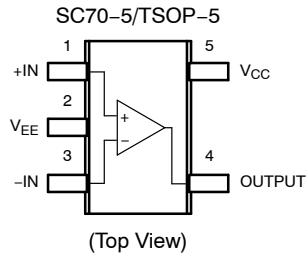
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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PIN CONNECTIONS



MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Supply Voltage (Operating Range $V_S = 1.8\text{ V to }5.5\text{ V}$)	5.5	V
V_{IDR}	Input Differential Voltage	\pm Supply Voltage	V
V_{ICR}	Input Common Mode Voltage Range	$-0.5\text{ to }(V_{CC}) + 0.5$	V
	Maximum Input Current	10	mA
t_{SO}	Output Short Circuit (Note 1)	Continuous	
T_J	Maximum Junction Temperature (Operating Range $-40^\circ\text{C to }85^\circ\text{C}$)	150	$^\circ\text{C}$
θ_{JA}	Thermal Resistance:	SC-70 TSOP-5 Micro8	$^\circ\text{C/W}$
T_{stg}	Storage Temperature	$-65\text{ to }150$	$^\circ\text{C}$
	Mounting Temperature (Infrared or Convection $\leq 30\text{ sec}$)	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ESD data available upon request.

1. Continuous short-circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V_{CC} or V_{EE} will adversely affect reliability.

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1.8 V DC ELECTRICAL CHARACTERISTICS (Note 2) Unless otherwise noted, all min/max limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 1.8\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	LMV931 (Single) (-40°C to $+125^\circ\text{C}$)		1	6	mV
		LMV932 (Dual) (-40°C to $+125^\circ\text{C}$)		1	7.5	
Input Offset Voltage Average Drift	TCV_{IO}			5.5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	-40°C to $+125^\circ\text{C}$		< 1		nA
Input Offset Current	I_{IO}	-40°C to $+125^\circ\text{C}$		< 1		nA
Supply Current (per Channel)	I_{CC}	In Active Mode		75	185	μA
		-40°C to $+125^\circ\text{C}$			205	
Common Mode Rejection Ratio	CMRR	$0\text{ V} \leq V_{CM} \leq 0.6\text{ V}$, $1.4\text{ V} \leq V_{CM} \leq 1.8\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
		$-0.2\text{ V} \leq V_{CM} \leq 0\text{ V}$, $1.8\text{ V} \leq V_{CM} \leq 2\text{ V}$	50	70		
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} \leq V^+ \leq 5\text{ V}$, $V_{CM} = 0.5\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
Input Common-Mode Voltage Range	VCM	For CMRR $\geq 50\text{ dB}$ and $T_A = 25^\circ\text{C}$	$V_{EE} - 0.2$	-0.2 to 2.1	$V_{CC} + 0.2$	V
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{EE}		V_{CC}	
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{EE} + 0.2$		$V_{CC} - 0.2$	
Large Signal Voltage Gain LMV931 (Single)	A_V	$R_L = 600\ \Omega$ to 0.9 V , $V_O = 0.2\text{ V}$ to 1.6 V , $V_{CM} = 0.5\text{ V}$	77	101		dB
		-40°C to $+125^\circ\text{C}$	73			
		$R_L = 2\text{ k}\Omega$ to 0.9 V , $V_O = 0.2\text{ V}$ to 1.6 V , $V_{CM} = 0.5\text{ V}$	80	105		
		-40°C to $+125^\circ\text{C}$	75			
Large Signal Voltage Gain LMV932 (Dual)	A_V	$R_L = 600\ \Omega$ to 0.9 V , $V_O = 0.2\text{ V}$ to 1.6 V , $V_{CM} = 0.5\text{ V}$	75	90		dB
		-40°C to $+125^\circ\text{C}$	72			
		$R_L = 2\text{ k}\Omega$ to 0.9 V , $V_O = 0.2\text{ V}$ to 1.6 V , $V_{CM} = 0.5\text{ V}$	78	100		
		-40°C to $+125^\circ\text{C}$	75			
Output Swing	V_{OH}	$R_L = 600\ \Omega$ to 0.9 V , $V_{IN} = \pm 100\text{ mV}$	1.65	1.72		V
		-40°C to $+125^\circ\text{C}$	1.63			
	V_{OL}	$R_L = 600\ \Omega$ to 0.9 V , $V_{IN} = \pm 100\text{ mV}$		0.077	0.105	
		-40°C to $+125^\circ\text{C}$			0.12	
	V_{OH}	$R_L = 2\text{ k}\Omega$ to 0.9 V , $V_{IN} = \pm 100\text{ mV}$	1.75	1.77		
		-40°C to $+125^\circ\text{C}$	1.74			
	V_{OL}	$R_L = 2\text{ k}\Omega$ to 0.9 V , $V_{IN} = \pm 100\text{ mV}$		0.24	0.035	
		-40°C to $+125^\circ\text{C}$			0.04	
Output Short Circuit Current	I_O	Sourcing, $V_O = 0\text{ V}$, $V_{IN} = +100\text{ mV}$	4.0	30		mA
		-40°C to $+125^\circ\text{C}$	3.3			
		Sinking, $V_O = 1.8\text{ V}$, $V_{IN} = -100\text{ mV}$	7.0	60		
		-40°C to $+125^\circ\text{C}$	5.0			

2. Guaranteed by design and/or characterization.

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1.8 V AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 1.8\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	SR	(Note 3)		0.35		V/ μS
Gain Bandwidth Product	GBWP			1.4		MHz
Phase Margin	Θ_m			67		$^\circ$
Gain Margin	Gm			7		dB
Input-Referred Voltage Noise	e_n	$f = 50\text{ kHz}$, $V_{CM} = 0.5\text{ V}$		60		nV/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion	THD	$f = 1\text{ kHz}$, $A_V = +1$, $R_L = 600\ \Omega$, $V_O = 1\text{ V}_{PP}$		0.023		%
Amplifier-to-Amplifier Isolation		(Note 4)		123		dB

3. Connected as voltage follower with input step from V_{EE} to V_{CC} . Number specified is the slower of the positive and negative slew rates.
4. Input referred, $R_L = 100\text{ k}\Omega$ connected to $V_S/2$. Each amp excited in turn with 1 kHz to produce $V_O = 3\text{ V}_{PP}$. (For Supply Voltages $< 3\text{ V}$, $V_O = V_{CC}$).

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2.7 V DC ELECTRICAL CHARACTERISTICS (Note 5) Unless otherwise noted, all min/max limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 2.7\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	LMV931 (Single) (-40°C to $+125^\circ\text{C}$)		1	6	mV
		LMV932 (Dual) (-40°C to $+125^\circ\text{C}$)		1	7.5	
Input Offset Voltage Average Drift	TCV_{IO}			5.5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	-40°C to $+125^\circ\text{C}$		< 1		nA
Input Offset Current	I_{IO}	-40°C to $+125^\circ\text{C}$		< 1		nA
Supply Current (per Channel)	I_{CC}	In Active Mode		80	190	μA
		-40°C to $+125^\circ\text{C}$			210	
Common Mode Rejection Ratio	CMRR	$0\text{ V} \leq V_{CM} \leq 1.5\text{ V}$, $2.3\text{ V} \leq V_{CM} \leq 2.7\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
		$-0.2\text{ V} \leq V_{CM} \leq 0\text{ V}$, $2.7\text{ V} \leq V_{CM} \leq 2.9\text{ V}$	50	70		
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} \leq V^+ \leq 5\text{ V}$, $V_{CM} = 0.5\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
Input Common-Mode Voltage Range	VCM	For CMRR $\geq 50\text{ dB}$ and $T_A = 25^\circ\text{C}$	$V_{EE} - 0.2$	-0.2 to 3.0	$V_{CC} + 0.2$	V
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{EE}		V_{CC}	
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{EE} + 0.2$		$V_{CC} - 0.2$	
Large Signal Voltage Gain LMV931 (Single)	A_V	$R_L = 600\ \Omega$ to 1.35 V , $V_O = 0.2\text{ V}$ to 2.5 V	87	104		dB
		-40°C to $+125^\circ\text{C}$	86			
		$R_L = 2\text{ k}\Omega$ to 1.35 V , $V_O = 0.2\text{ V}$ to 2.5 V	92	110		
		-40°C to $+125^\circ\text{C}$	91			
Large Signal Voltage Gain LMV932 (Dual)	A_V	$R_L = 600\ \Omega$ to 1.35 V , $V_O = 0.2\text{ V}$ to 2.5 V	78	90		dB
		-40°C to $+125^\circ\text{C}$	75			
		$R_L = 2\text{ k}\Omega$ to 1.35 V , $V_O = 0.2\text{ V}$ to 2.5 V	81	100		
		-40°C to $+125^\circ\text{C}$	78			
Output Swing	V_{OH}	$R_L = 600\ \Omega$ to 1.35 V , $V_{IN} = \pm 100\text{ mV}$	2.55	2.62		V
		-40°C to $+125^\circ\text{C}$	2.53			
	V_{OL}	$R_L = 600\ \Omega$ to 1.35 V , $V_{IN} = \pm 100\text{ mV}$		0.083	0.11	
		-40°C to $+125^\circ\text{C}$			0.13	
	V_{OH}	$R_L = 2\text{ k}\Omega$ to 1.35 V , $V_{IN} = \pm 100\text{ mV}$	2.65	2.675		
		-40°C to $+125^\circ\text{C}$	2.64			
	V_{OL}	$R_L = 2\text{ k}\Omega$ to 1.35 V , $V_{IN} = \pm 100\text{ mV}$		0.025	0.04	
		-40°C to $+125^\circ\text{C}$			0.045	
Output Short Circuit Current	I_O	Sourcing, $V_o = 0\text{ V}$, $V_{IN} = \pm 100\text{ mV}$	20	65		mA
		-40°C to $+125^\circ\text{C}$	15			
		Sinking, $V_o = 0\text{ V}$, $V_{IN} = -100\text{ mV}$	18	75		
		-40°C to $+125^\circ\text{C}$	12			

5. Guaranteed by design and/or characterization.

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2.7 V AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 2.7\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	SR	(Note 6)		0.4		V/ μS
Gain Bandwidth Product	GBWP			1.4		MHz
Phase Margin	Θ_m			70		$^\circ$
Gain Margin	Gm			7.5		dB
Input-Referred Voltage Noise	e_n	$f = 50\text{ kHz}$, $V_{CM} = 1.0\text{ V}$		57		$\text{nV}/\sqrt{\text{Hz}}$
Total Harmonic Distortion	THD	$f = 1\text{ kHz}$, $A_V = +1$, $R_L = 600\ \Omega$, $V_O = 1\text{ V}_{PP}$		0.022		%
Amplifier-to-Amplifier Isolation		(Note 7)		123		dB

6. Connected as voltage follower with input step from V_{EE} to V_{CC} . Number specified is the slower of the positive and negative slew rates.
 7. Input referred, $R_L = 100\text{ k}\Omega$ connected to $V_S/2$. Each amp excited in turn with 1 kHz to produce $V_O = 3\text{ V}_{PP}$. (For Supply Voltages $< 3\text{ V}$, $V_O = V_{CC}$).

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5 V DC ELECTRICAL CHARACTERISTICS (Note 8) Unless otherwise noted, all min/max limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	LMV931 (Single) (-40°C to $+125^\circ\text{C}$)		1	6	mV
		LMV932 (Dual) (-40°C to $+125^\circ\text{C}$)		1	7.5	
Input Offset Voltage Average Drift	TCV_{IO}			5.5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	-40°C to $+125^\circ\text{C}$		< 1		nA
Input Offset Current	I_{IO}	-40°C to $+125^\circ\text{C}$		< 1		nA
Supply Current (per Channel)	I_{CC}	In Active Mode		95	210	μA
		-40°C to $+125^\circ\text{C}$			230	
Common-Mode Rejection Ratio	CMRR	$0\text{ V} \leq V_{CM} \leq 3.8\text{ V}$, $4.6\text{ V} \leq V_{CM} \leq 5.0\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
		$-0.2\text{ V} \leq V_{CM} \leq 0\text{ V}$, $5.0\text{ V} \leq V_{CM} \leq 5.2\text{ V}$	50	70		
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} \leq V^+ \leq 5\text{ V}$, $V_{CM} = 0.5\text{ V}$	50	70		dB
		-40°C to $+125^\circ\text{C}$	50			
Input Common-Mode Voltage Range	VCM	For CMRR $\geq 50\text{ dB}$ and $T_A = 25^\circ\text{C}$	$V_{EE} - 0.2$	-0.2 to 5.3	$V_{CC} + 0.2$	V
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{EE}		V_{CC}	
		For CMRR $\geq 50\text{ dB}$ and $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{EE} + 0.3$		$V_{CC} - 0.3$	
Large Signal Voltage Gain LMV931 (Single)	A_V	$R_L = 600\ \Omega$ to 2.5 V , $V_O = 0.2\text{ V}$ to 4.8 V	88	102		dB
		-40°C to $+125^\circ\text{C}$	87			
		$R_L = 2\text{ k}\Omega$ to 2.5 V , $V_O = 0.2\text{ V}$ to 4.8 V	94	113		
		-40°C to $+125^\circ\text{C}$	93			
Large Signal Voltage Gain LMV932 (Dual)	A_V	$R_L = 600\ \Omega$ to 2.5 V , $V_O = 0.2\text{ V}$ to 4.8 V	81	90		dB
		-40°C to $+125^\circ\text{C}$	78			
		$R_L = 2\text{ k}\Omega$ to 2.5 V , $V_O = 0.2\text{ V}$ to 4.8 V	85	100		
		-40°C to $+125^\circ\text{C}$	82			
Output Swing	V_{OH}	$R_L = 600\ \Omega$ to 2.5 V , $V_{IN} = \pm 100\text{ mV}$	4.855	4.89		V
		-40°C to $+125^\circ\text{C}$	4.835			
	V_{OL}	$R_L = 600\ \Omega$ to 2.5 V , $V_{IN} = \pm 100\text{ mV}$		0.12	0.16	
		-40°C to $+125^\circ\text{C}$			0.18	
	V_{OH}	$R_L = 2\text{ k}\Omega$ to 2.5 V , $V_{IN} = \pm 100\text{ mV}$	4.945	4.967		
		-40°C to $+125^\circ\text{C}$	4.935			
	V_{OL}	$R_L = 2\text{ k}\Omega$ to 2.5 V , $V_{IN} = \pm 100\text{ mV}$		0.037	0.065	
		-40°C to $+125^\circ\text{C}$			0.075	
Output Short-Circuit Current	I_O	Sourcing, $V_O = 0\text{ V}$, $V_{IN} = +100\text{ mV}$	55	65		mA
		-40°C to $+125^\circ\text{C}$	45			
		Sinking, $V_O = 5\text{ V}$, $V_{IN} = -100\text{ mV}$	58	80		
		-40°C to $+125^\circ\text{C}$	45			

8. Guaranteed by design and/or characterization.

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5 V AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $V_O = V_S/2$ and $R_L > 1\text{ M}\Omega$. Typical specifications represent the most likely parametric norm.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	SR	(Note 9)		0.48		V/ μS
Gain Bandwidth Product	GBWP			1.5		MHz
Phase Margin	Θ_m			65		$^\circ$
Gain Margin	Gm			8		dB
Input-Referred Voltage Noise	e_n	$f = 50\text{ kHz}$, $V_{CM} = 2\text{ V}$		50		nV/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion	THD	$f = 1\text{ kHz}$, $A_V = +1$, $R_L = 600\ \Omega$, $V_O = 1\text{ V}_{PP}$		0.022		%
Amplifier-to-Amplifier Isolation		(Note 10)		123		dB

9. Connected as voltage follower with input step from V_{EE} to V_{CC} . Number specified is the slower of the positive and negative slew rates.

10. Input referred, $R_L = 100\text{ k}\Omega$ connected to $V_S/2$. Each amp excited in turn with 1 kHz to produce $V_O = 3\text{ V}_{PP}$. (For Supply Voltages $< 3\text{ V}$, $V_O = V_{CC}$).

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TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

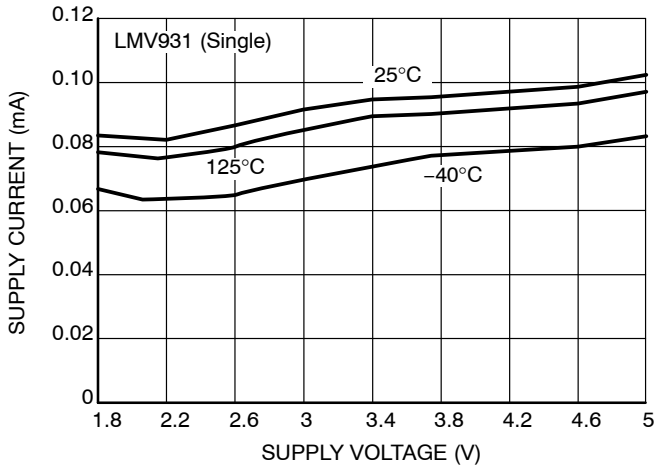


Figure 2. Supply Current vs. Supply Voltage

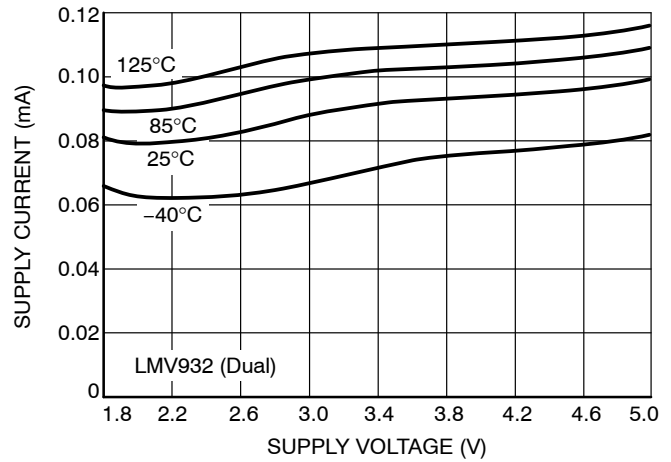


Figure 3. Supply Current vs. Supply Voltage

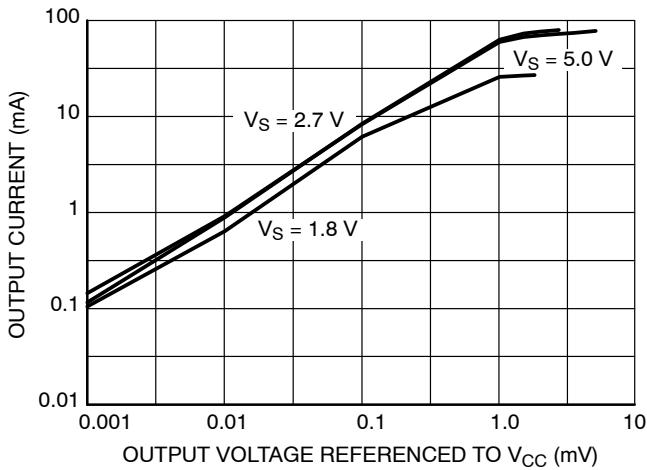


Figure 4. Sourcing Current vs. Output Voltage
($T_A = 25^\circ\text{C}$)

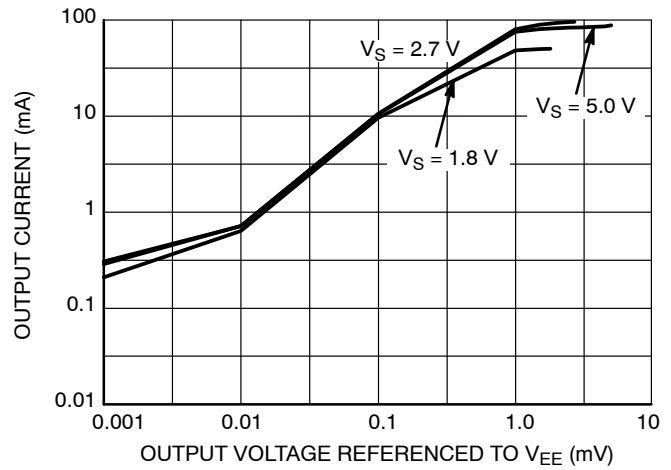


Figure 5. Sinking Current vs. Output Voltage
($T_A = 25^\circ\text{C}$)

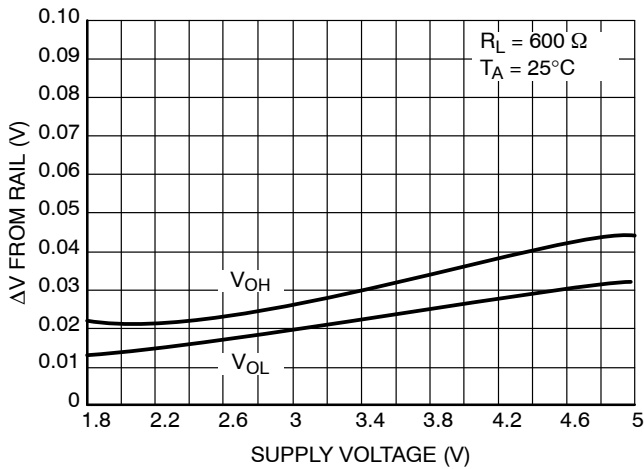


Figure 6. Output Voltage Swing vs. Supply Voltage

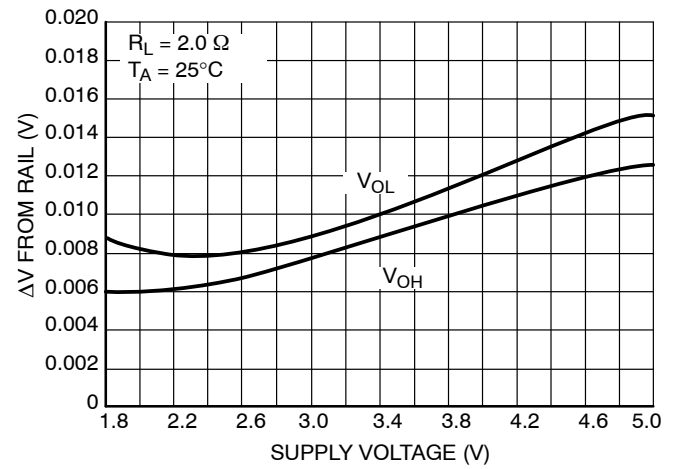


Figure 7. Output Voltage vs. Supply Voltage

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TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

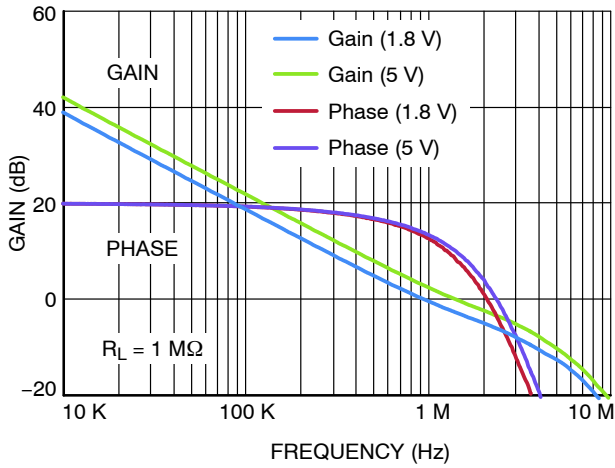


Figure 8. Open Loop Gain and Phase

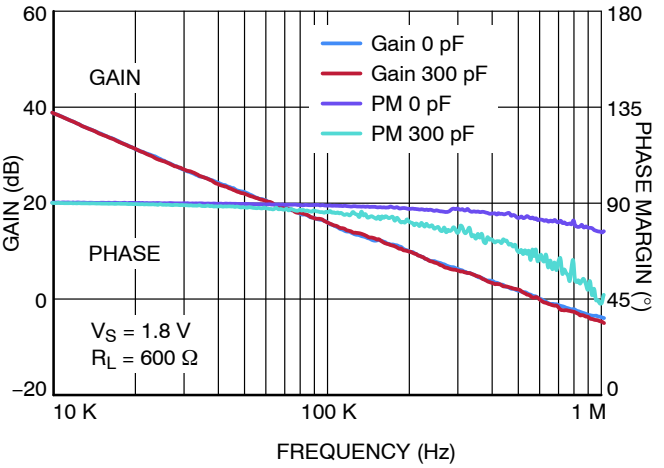


Figure 9. Frequency Response vs. CL

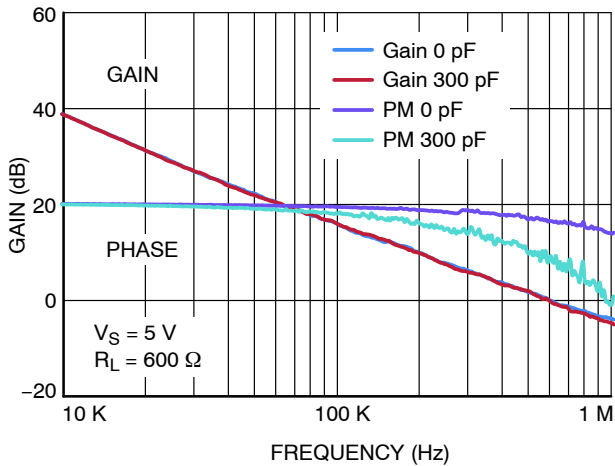


Figure 10. Frequency Response vs. CL

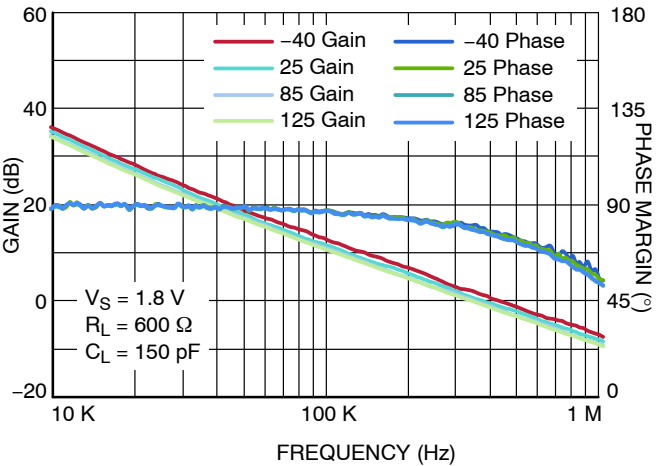


Figure 11. Gain and Phase vs. Temp

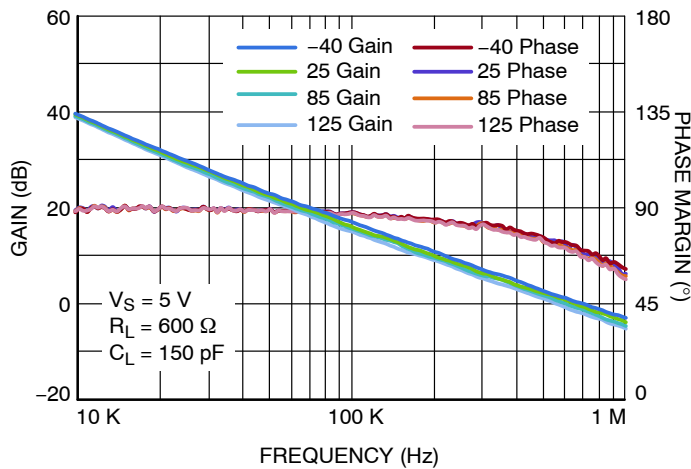


Figure 12. Gain and Phase vs. Temp

LMV931, LMV932

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

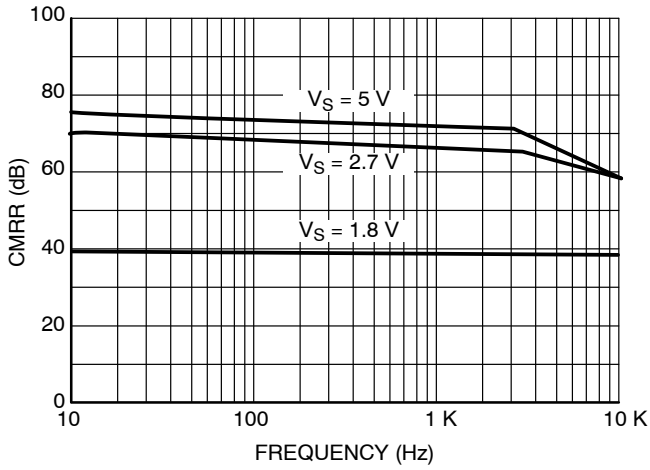


Figure 13. CMRR vs. Frequency

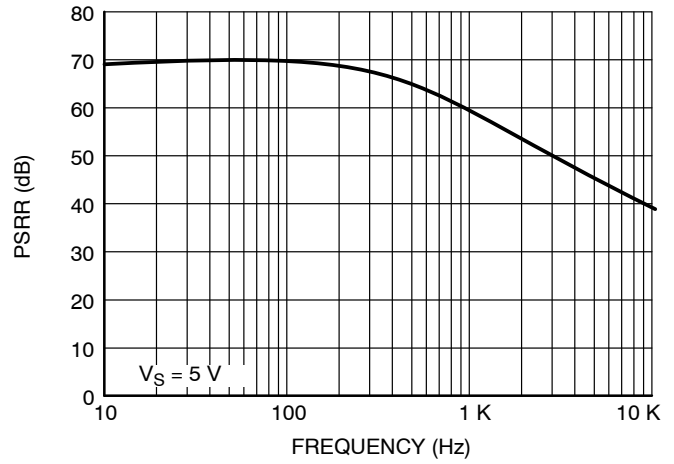


Figure 14. PSRR vs. Frequency

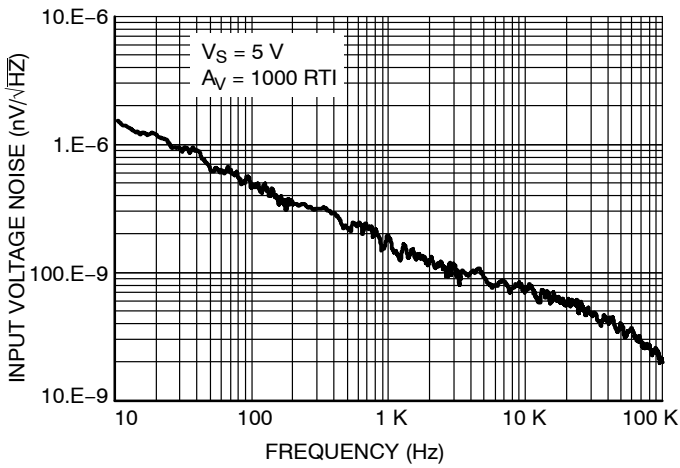


Figure 15. Input Voltage Noise vs. Frequency

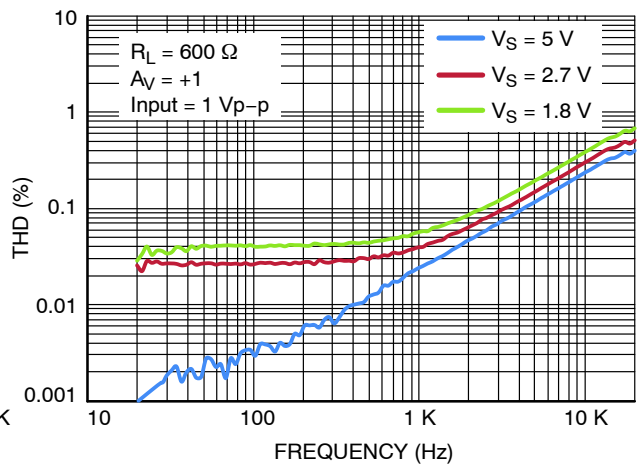


Figure 16. THD vs. Frequency

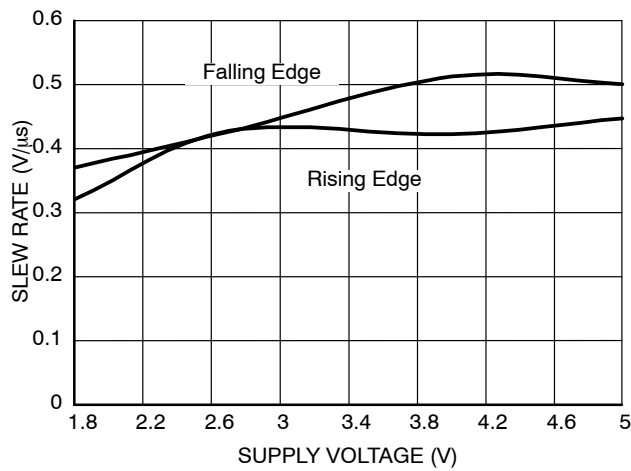


Figure 17. Slew Rate vs. Supply Voltage

LMV931, LMV932

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

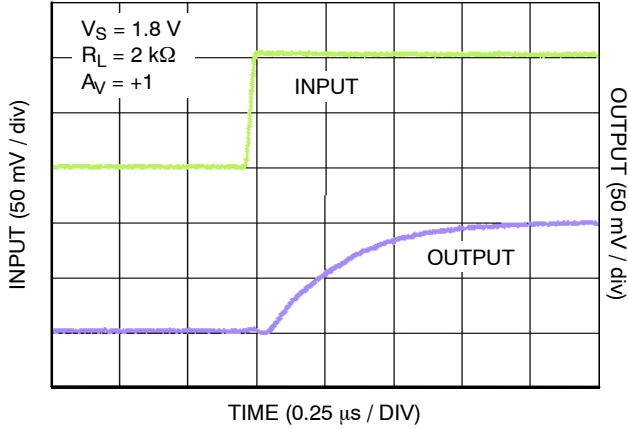


Figure 18. Small Signal Transient Response

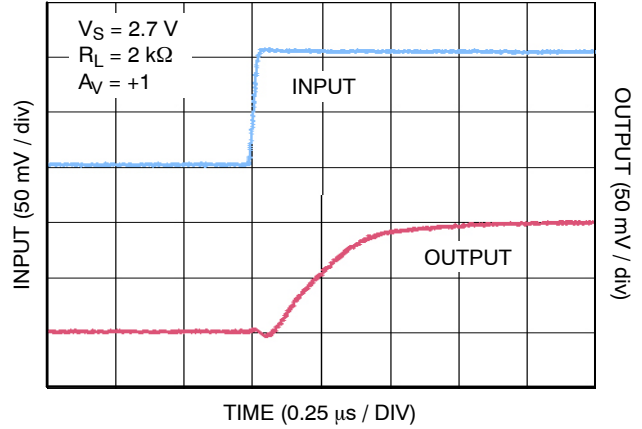


Figure 19. Small Signal Transient Response

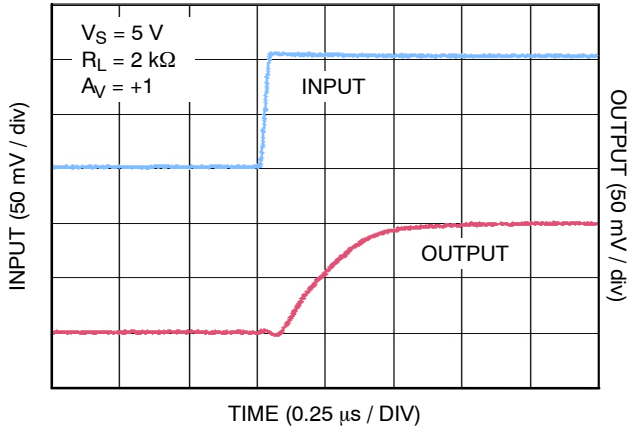


Figure 20. Small Signal Transient Response

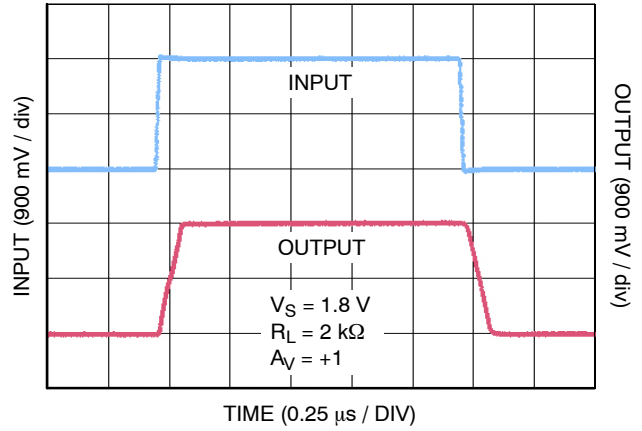


Figure 21. Large Signal Transient Response

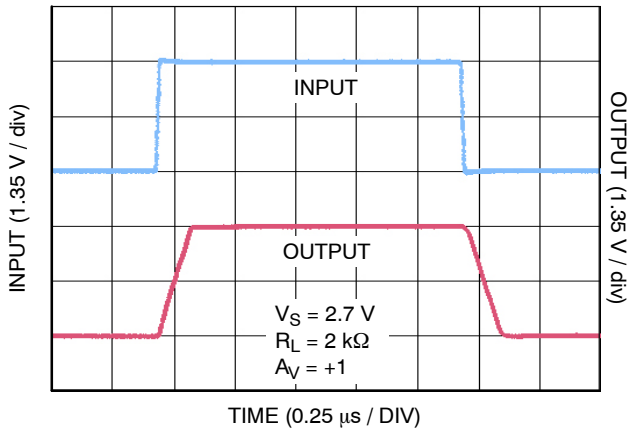


Figure 22. Large Signal Transient Response

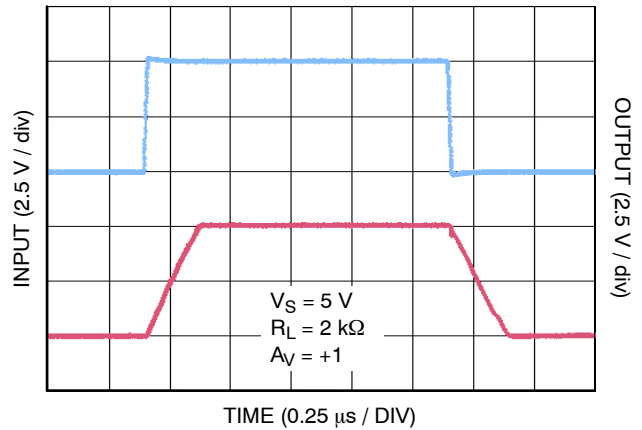


Figure 23. Large Signal Transient Response

LMV931, LMV932

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

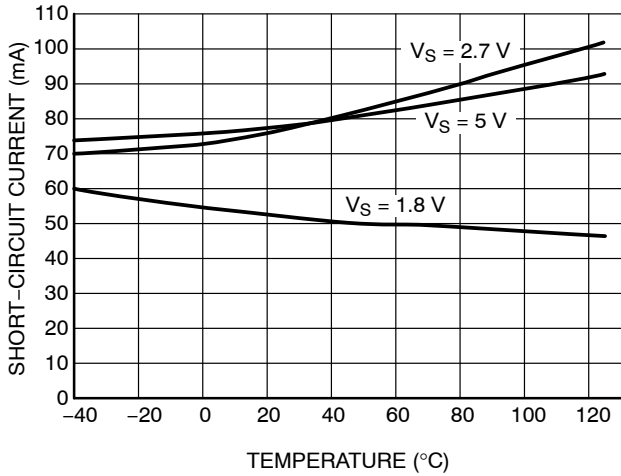


Figure 24. Short-Circuit vs. Temperature (Sinking)

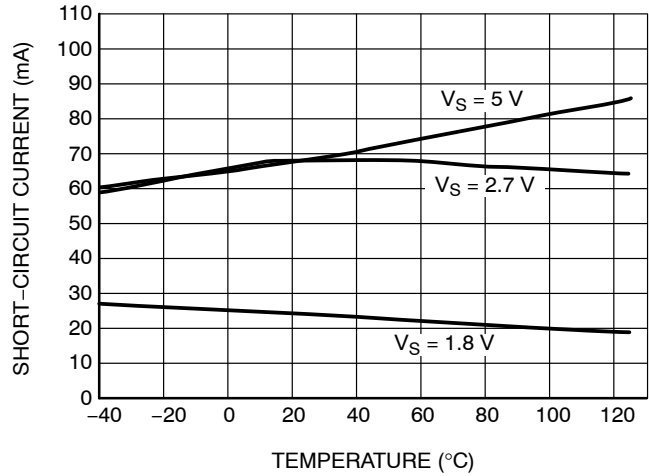


Figure 25. Short-Circuit vs. Temperature (Sourcing)

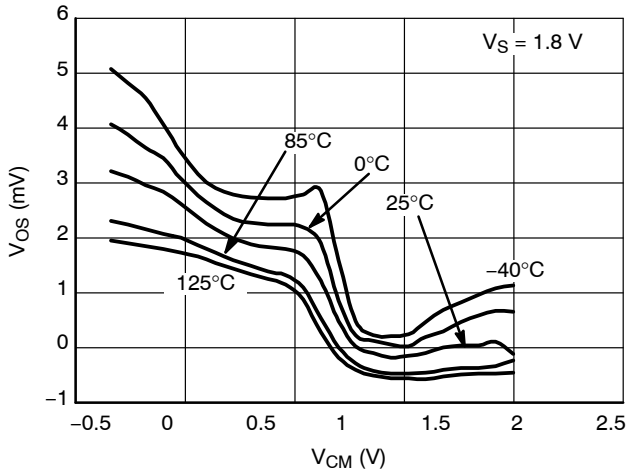


Figure 26. Offset Voltage vs. Common Mode Range V_{DD}

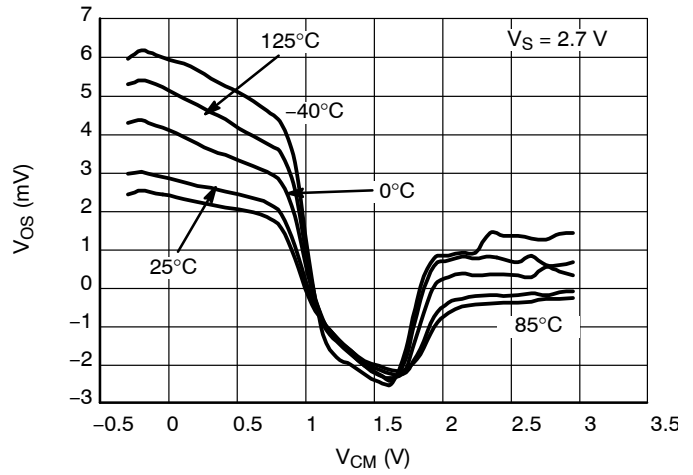


Figure 27. Offset Voltage vs. Common Mode Range

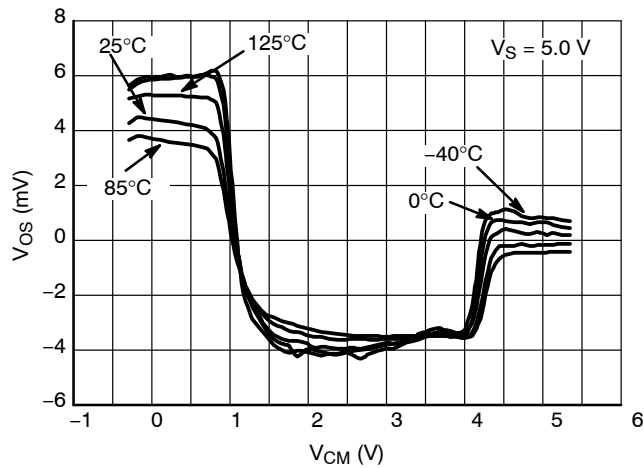


Figure 28. Offset Voltage vs. Common Mode Range

LMV931, LMV932

APPLICATION INFORMATION

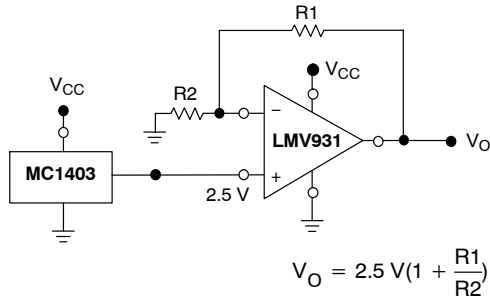


Figure 29. Voltage Reference

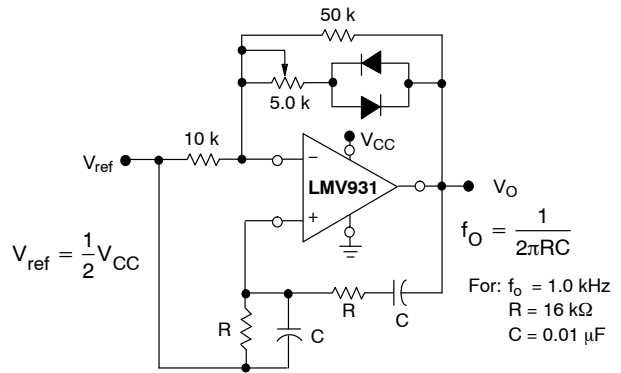


Figure 30. Wien Bridge Oscillator

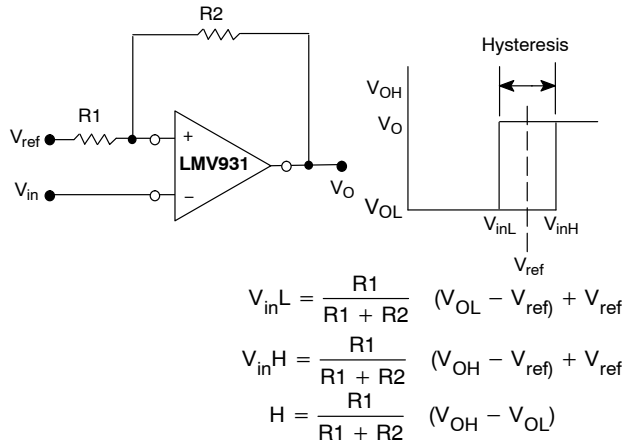
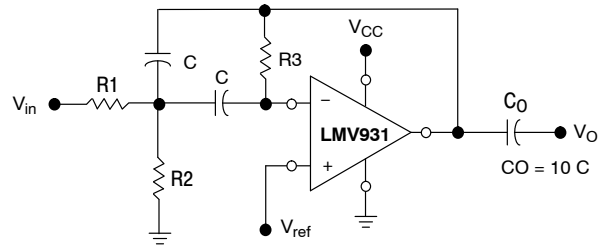


Figure 31. Comparator with Hysteresis



Given: f_o = center frequency
 $A(f_o)$ = gain at center frequency

Choose value f_o, C
 Then: $R3 = \frac{Q}{\pi f_o C}$
 $R1 = \frac{R3}{2 A(f_o)}$
 $R2 = \frac{R1 R3}{4Q^2 R1 - R3}$

For less than 10% error from operational amplifier,
 $((Q_o f_o)/BW) < 0.1$ where f_o and BW are expressed in Hz.
 If source impedance varies, filter may be preceded with
 voltage follower buffer to stabilize filter parameters.

Figure 32. Multiple Feedback Bandpass Filter

ORDERING INFORMATION

Order Number	Number of Channels	Number of Pins	Package Type	Shipping [†]
LMV931SQ3T2G	Single	5	SC70-5 (Pb-Free)	3000 / Tape & Reel
LMV931SN3T1G	Single	5	TSOP-5 (Pb-Free)	3000 / Tape & Reel
LMV932DMR2G	Dual	8	Micro8 (Pb-Free)	4000 / Tape & Reel
LMV932DR2G	Dual	8	SOIC-8 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

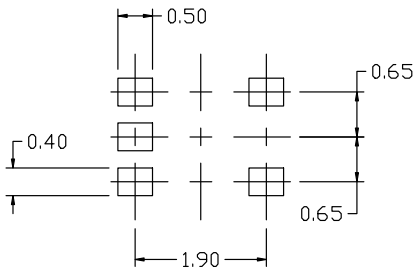
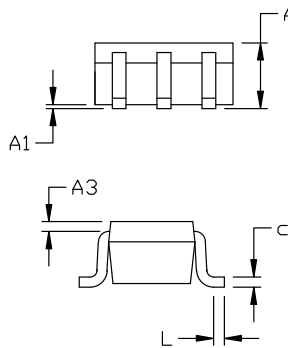
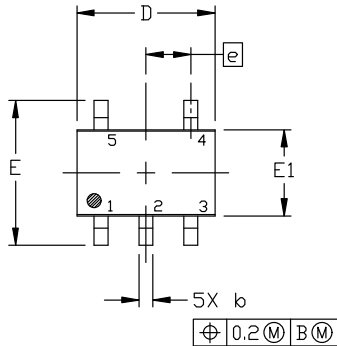
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

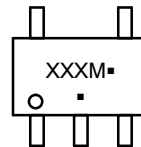
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 2:

- PIN 1. ANODE
- EMITTER
- BASE
- COLLECTOR
- CATHODE

STYLE 3:

- PIN 1. ANODE 1
- N/C
- ANODE 2
- CATHODE 2
- CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- DRAIN 1/2
- SOURCE 1
- GATE 1
- GATE 2

STYLE 5:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- BASE 2
- EMITTER 1
- COLLECTOR
- COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- COLLECTOR
- N/C
- BASE
- EMITTER

STYLE 9:

- PIN 1. ANODE
- CATHODE
- ANODE
- ANODE
- ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- | | |
|----------------------------|----------------------------|
| XXX = Specific Device Code | XXX = Specific Device Code |
| A = Assembly Location | M = Date Code |
| Y = Year | ■ = Pb-Free Package |
| W = Work Week | |
| ■ = Pb-Free Package | |

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

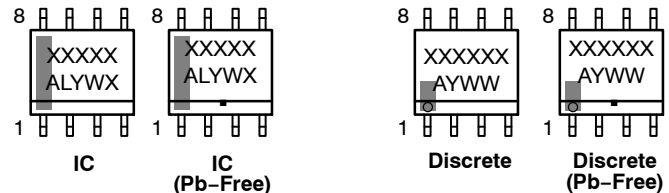
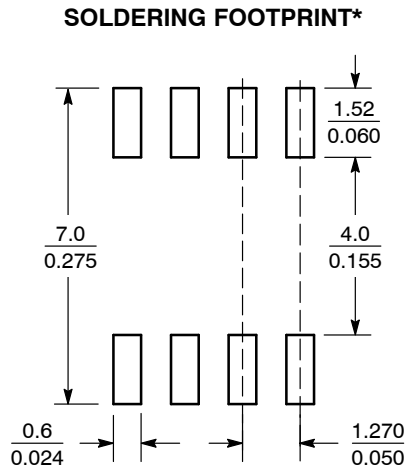
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

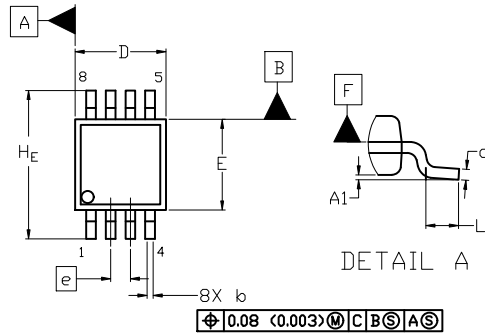
ON Semiconductor®



SCALE 2:1

Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW

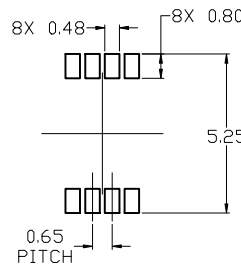


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$ (0.003) M C B S A S

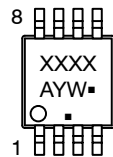


RECOMMENDED MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H_E</i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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