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## MCP2518FD

### Silicon Errata and Data Sheet Clarification

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The functionality of the MCP2518FD devices is described in the Device Data Sheet (DS20006027A), except for the anomalies described below.

#### 1. Module: SPI Module

##### Incorrect CRC for certain READ\_CRC commands:

There is a possible mismatch between the transmitted CRC and the actual CRC for the transmitted data, when data are updated at a specific time during the SPI READ\_CRC command.

In such cases, the transmitted CRC is wrong and a glitch occurs on the SDO line, shorter than 1 bit in length. The data transmitted are correct.

##### Fix/Work Around:

If a CRC mismatch occurs, re-issue the READ\_CRC command.

Only bits 7/15/23/31 of the following registers can be affected:

CiTXIF

CiRXIF

CiCON

CiTBC

CiINT

CiRXOVIF

CiTXATIF

CiTXREQ

CiTREC

CiBDIAG0

CiBDIAG1

CiTXQSTA

CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31. In these cases, the registers, CiTXIF, CiRXIF, CiRXOVIF, CiTXATIF and CiTXREQ, are not affected.

Bit 31 of RAM reads with CRC can also be affected. This can be avoided by reading from a receive FIFO only after the message has been loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

#### 2. Module: ECC Module

##### ECC Single Error Correction does not work in all cases:

##### Fix/Work Around:

Enable Single Error Correction (SEC) and Double Error Detection (DED) interrupts by setting SECIE and DEDIE. Handle SECIF as a detection interrupt and do not rely on the error correction. Instead, handle both interrupts as a notification that the RAM word at ERRADDR was corrupted.

#### 3. Module: SPI Module

##### SFR address rollover does not work:

The SFR address rollover, from 0x3FF to 0x000 and from 0xFFF to 0xE00, does not work. Instead, the address changes from 0x3FF to 0x400 and from 0xFFF to 0x000.

The address rollover for the RAM works as described.

##### Fix/Work Around:

None.

#### 4. Module: SPI/RAM Module

##### The SPI can write corrupted data to the RAM at fast SPI speeds:

Simultaneous activity on the CAN bus while writing data to RAM via the SPI interface, with high SCK frequency, can lead to corrupted data being written to RAM.

##### Fix/Work Around:

Ensure that FSCK is less than or equal to  $0.85 * (FSYSCLK/2)$ .

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## 5. Module: SPI/GPIO Module

### Writing multiple bytes to the IOCON register using one SPI `WRITE` instruction may overwrite LAT0 and LAT1:

Writing Byte 2 and Byte 3 of the IOCON register using one SPI `WRITE` instruction clears LAT0 and LAT1.

### **Fix/Work Around:**

When setting LAT0 or LAT1, do not use a multi-data byte SPI `WRITE` instruction.

Instead, write the bit fields in the IOCON register using single data byte SFR `WRITE` instructions.

## Clarifications/Corrections to the Data Sheet:

In the MCP2518FD Data Sheet (DS20006027A), the following clarifications and corrections should be noted.

None.

## APPENDIX A: REVISION HISTORY

### Revision C (October 2020)

- Corrections added to [SPI Module](#).

### Revision B (September 2020)

- Added [ECC Module](#), [SPI Module](#), [SPI/RAM Module](#) and [SPI/GPIO Module](#).

### Revision A (May 2018)

- Initial Release of this Document.

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NOTES:

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