AOZ5239QI

High-Current, High-Performance DrMOS Power Module

General Description

The AOZ5239QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra low ON resistance to minimize conduction loss. The compact 5x5 QFN package is optimally designed to minimize parasitic inductance for minimal EMI signature.

The AOZ5239QI is compatible with 3.3V and 5V PWM logic with Mid-state levels compatibility by using both the PWM and/or SMOD# can be used to control the power MOSFETs.

The bootstrap diode is integrated in the driver. The low side MOSFET can be driven into pulse skip mode to provide power saving operation when required. The pin-out is optimized for low inductance routing, keeping the parasitics and their effects to a minimum.

Features

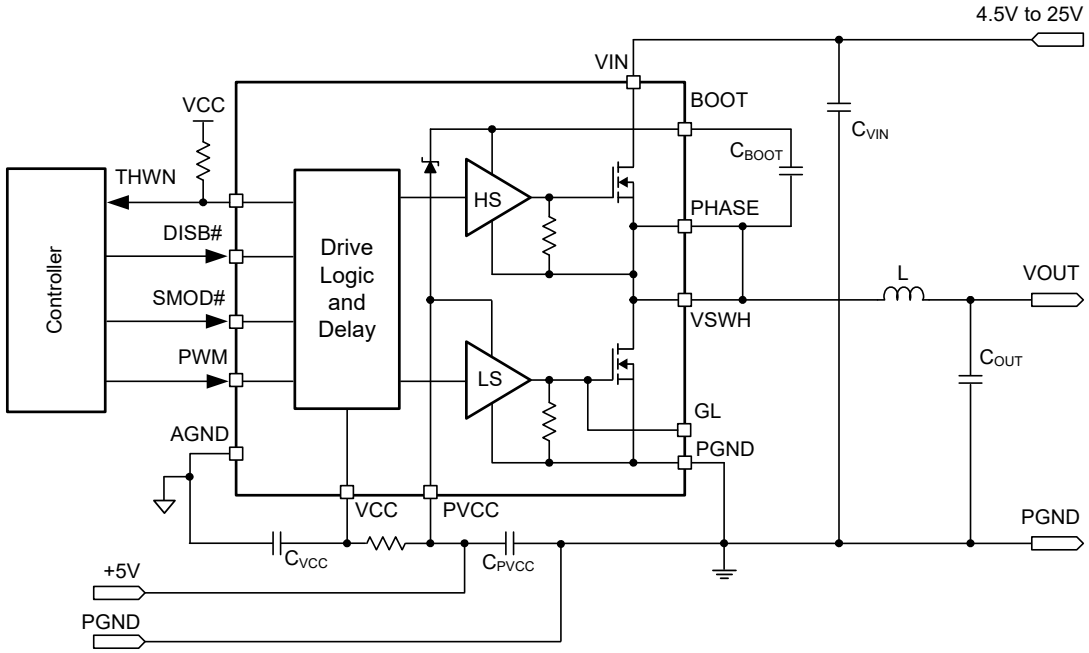
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- Up to 70A peak output current
- Continuous current up to 50A
- Integrated booststrap schottky diode
- Up to 2MHz switching operation
- Pulse Skip Mode for Light Load Efficiency
- Supports Intel ® Power State 4
- Thermal Warning Output
- Thermal Shutdown
- Tri-state PWM input compatible
- Under-Voltage LockOut protection
- Low Profile 5x5 QFN-31L package

Applications

- Desktop
- Notebook computers
- Graphic cards
- Video gaming console

Green Product

Typical Application Circuit

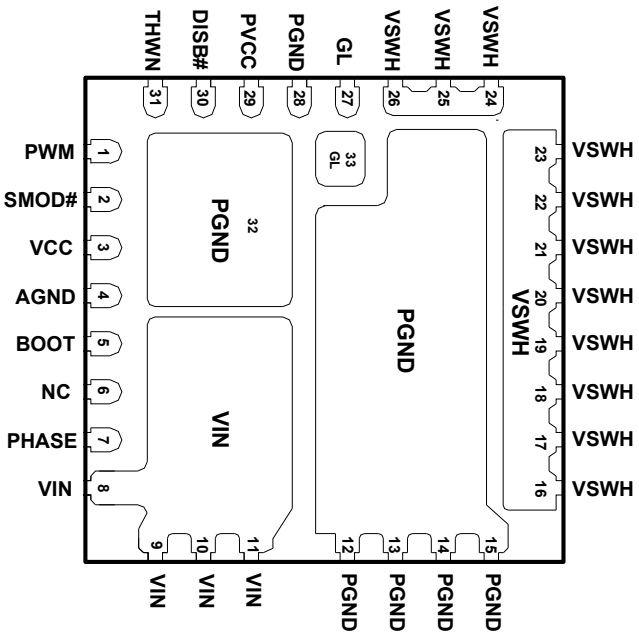


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5239QI	-40°C to +85°C	QFN5x5_31L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

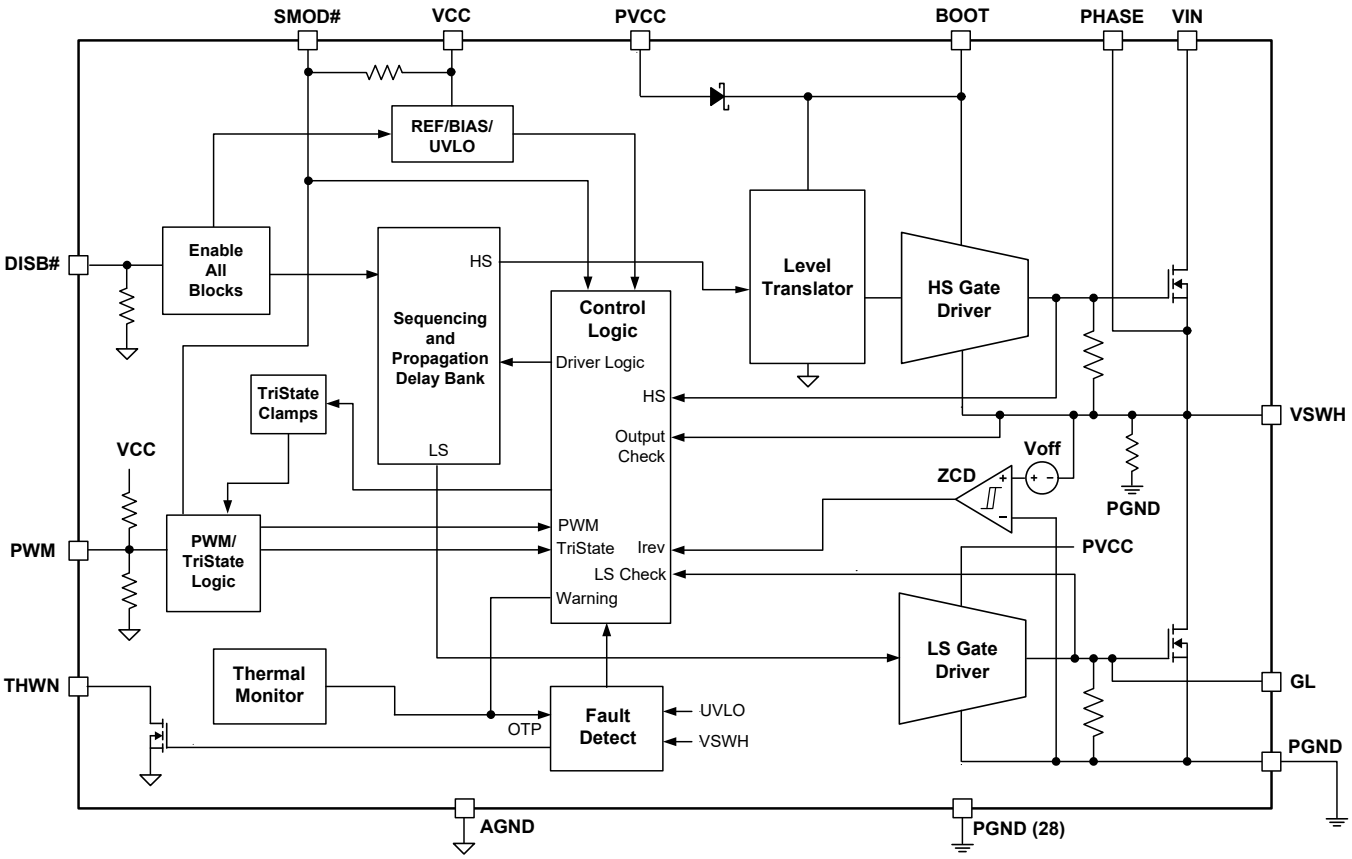


QFN5x5_31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC.
2	SMOD#	Skip Mode pin. 3−state input (see Table 1 LOGIC TABLE): SMOD# = High → The zero cross comparator and the state of PWM determine whether the AOZ5239QI performs Zero Cross Detection SMOD# = Mid → Connects PWM to internal resistor divider placing a bias voltage on an undrivern PWM pin. Otherwise, logic is equivalent to SMOD# in the high state. SMOD# = Low → Placing PWM into mid−state pulls the High and Low Side MOSFET gates low without delay. There is an internal pull−up resistor to VCC on this pin.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between V_{CC} (Pin 3) and AGND (Pin 4).
4	AGND	Signal Ground
5	BOOT	High Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	No Connect.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (pin5). It is required to be connected to Pin 16 - 26 externally on PCB.
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain Connection of HS MOSFET)
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source Connection of LS MOSFET).
16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	VSWH	Switching node connected to the source of High Side MOSFET and the drain of Low Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal. Ensure these pins are connected to pin 7 externally on PCB.
27, 33	GL	Low Side MOSFET Gate connection. This is for test purposes only.
28, 32	PGND	Power Ground pin for High Side and Low Side MOSFET Gate Drivers. Ensure to connect 1µF across PGND (pin 28) to each of the VCC (Pin 3) and to PVCC (Pin 29) independently.
29	PVCC	5V Power Rail for High Side and Low Side MOSFET Drivers. Ensure to position a 1µF MLCC directly between PVCC (Pin 29) and PGND (Pin 28).
30	DISB#	Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull−down resistor on this pin.
31	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver die reaches the Over Temperature Threshold, this pin is pulled low.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 6.5V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, SMOD#, DISB#)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 35V
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to PVCC
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 7V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-7V to 37V
Low Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low Side Gate Voltage Transient(1) (GL)	(PGND-2.5V) to (PVCC+0.3V)
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	125°C
ESD Rating(2)	1.5kV

Notes:

1. Peak voltages can be applied for 5ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage / MOSFET Driver Supply VCC, PVCC	4.5V to 5.5V
Control Inputs (PWM, SMOD#, DISB#)	0V to (VCC-0.3V)
Operating Frequency	200kHz to 2MHz

Electrical Characteristics[3]

T_A = 25°C, V_{IN} = 12V, P_{VCC} = V_{CC} = 5V, V_{CC} = P_{VCC} = 1.0µF, DISB# = 2.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Power Stage Power Supply		4.5		20	V
P_{VCC}	Driver Power Supply		4.5		5.5	V
V_{CC}	Low Voltage Bias Supply		4.5		5.5	V
$R_{\theta JC}$[4]	Thermal Resistance	PCB Temp = 100°C		2.5		°C / W
$R_{\theta JA}$[4]		AOS Demo Board		13.8		°C / W
VCC and PVCC Supply Current						
VCC_{UVLO}	Under-Voltage Lockout	PVCC=VCC Rising	2.9	3.1	3.3	V
V_{CC_HYST}	Under-Voltage Lockout Hysteresis			410		mV
I_{VCC_SW}	Operating Current	DISB# = 5V, 400kHz		1	2	mA
I_{VCC_SD}	Shutdown Bias Supply Current	DISB# = 0V, SMOD# = VCC		0.1	1	µA
		DISB# = 0V, SMOD# = 0V		11	13	µA
I_{VCC}	Control Circuit Bias Current	DISB# = 5V, VPWM = 0V			2	mA
I_{PVCC}	PVCC Operating Current	DISB# = 5V, 400kHz		22		mA
	PVCC Enabled, Non Switching	DISB# = 5V, PWM = 0V, V_{PHASE} = 0V		220	300	µA
	PVCC, Disabled	DISB# = 0V		0.1	1	µA
PWM Input						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising	2.65			V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling			0.7	V
R_{PWM}	PWM Pin Input Resistance	SMOD# = HI and LO	10			kΩ
		SMOD# = Mid State		63		kΩ
V_{PWM_TRI}	PWM Input Tri State Threshold Window	PWM = High Impedance	1.4		2.0	V
V_{PWM_BIAS}	PWM Input Bias Voltage	SMOD# = Mid State		1.7		V
t_{pdlGL}	PWM Propagation Delay, Rising	PWM = 2.25V to GL = 90%; SMOD# = LOW		25		ns
$t_{pdlVSWH}$	PWM Propagation Delay, Falling	PWM = 0.75V to VSWH = 90%		15		ns
$t_{PWM\_EXIT\_L}$	Exiting PWM Mid−state Propagation Delay, Mid−to−Low	PWM = Mid−to−Low to GL = 10%,		25	30	ns
$t_{PWM\_EXIT\_H}$	Exiting PWM Mid−state Propagation Delay, Mid−to−High	PWM = Mid−to−High to VSWH = 10%		15	35	ns
ZCD Function						
V_{ZCD}	Zero Cross Detect Threshold			-6		mV
$t_{BLNK\_}$	ZCD Blanking + Debounce Time	SMOD# = High		330		ns
DISB# Input						
$R_{DISB\#}$	Input Resistance	With respect to AGND		470		kΩ
V_{UPPER}	Upper Threshold				2.0	V
V_{LOWER}	Lower Threshold		0.8			V
	Hysteresis	$V_{UPPER} - V_{LOWER}$	200			mV
t_{ENABLE}	Enable Delay Time	Time from DISB# transitioning HI to when VSWH responds to PWM			40	µs
$t_{DISABLE}$	Disable Delay Time	Time from DISB# transitioning LOW to when both output MOSFETs are off		25	50	ns

Electrical Characteristics[3]

T_A = 25°C, V_{IN} = 12V, P_{VCC} = V_{CC} = 5V, V_{CC} = P_{VCC} = 1.0µF, DISB# = 2.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
SMOD# Input						
$V_{SMOD\#\_HI}$	SMOD# Input Voltage High		2.65			V
$V_{SMOD\#\_MID}$	SMOD# Input Voltage Mid−state		1.4		2.0	V
$V_{SMOD\#\_LO}$	SMOD# Input Voltage Low				0.7	V
$R_{SMOD\#\_UP}$	SMOD# Input Resistance	Pull−up resistance to VCC		470		kΩ
$t_{SMOD\#\_PD\_F}$	SMOD# Propagation Delay, Falling	SMOD# = Low to GL = 90%, PWM = Low		15	30	ns
$t_{SMOD\#\_PD\_R}$	SMOD# Propagation Delay, Rising	SMOD# = High to GL = 10%, PWM = Low		10	30	ns
Thermal Warning and Shutdown						
T_{THWN}	Thermal Warning Temperature	Temperature at Driver Die		150		°C
T_{THWN_HYS}	Thermal Warning Hysteresis			15		°C
T_{THDN}	Thermal Shutdown Temperature	Temperature at Driver Die		180		°C
T_{THDN_HYS}	Thermal Shutdown Hysteresis			25		°C
I_{THWN}	THWN Open Drain Current				5	mA
Non--Overlap Delays						
$t_{pdhVSWH}$	Non−overlap Delay, Leading Edge	GL Falling = 1V to VSWH Rsing = 1V		13		ns
t_{pdhGL}	Non−overlap Delay, Trailing Edge	VSWH Falling = 1V to GL Rising = 1V		12		ns
Boostrap Diode						
V_F	Forward Voltage	Forward Bias Current = 2.0 mA		300		mV

Notes:

3. All voltages are specified with respect to the corresponding PGND pin.
4. Characterization value. Not tested in production.

Table 1. Logic Table

DISB#	PWM	SMOD# [5]	GH (Not a Pin)	GL
L	X	X	L	L
H	H	X	H	L
H	L	X	L	H
H	MID	H OR MID	L	ZCD [6]
H	MID	L	L	L [7]

Notes:

5. PWM input is driven to mid−state with internal divider resistors when SMOD# is driven to mid−state and PWM input is undriven externally.
6. GL goes low following 80 ns de−bounce time, 250 ns blanking time and then VSWH exceeding ZCD threshold.
7. There is no delay before GL goes low.

Timing Diagram

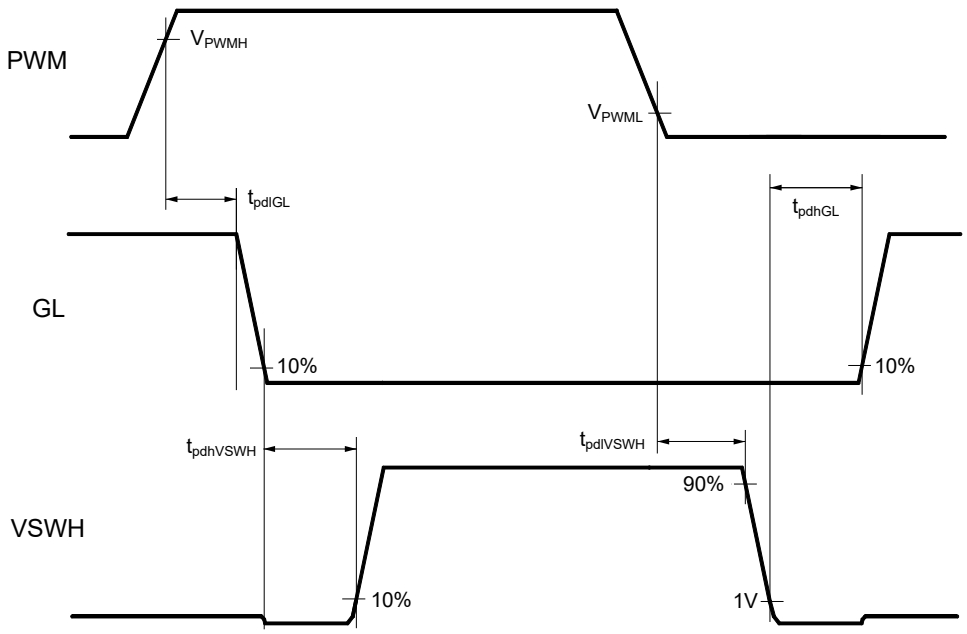


Figure 1. PWM Logic Timing Diagram (SMOD#=High)

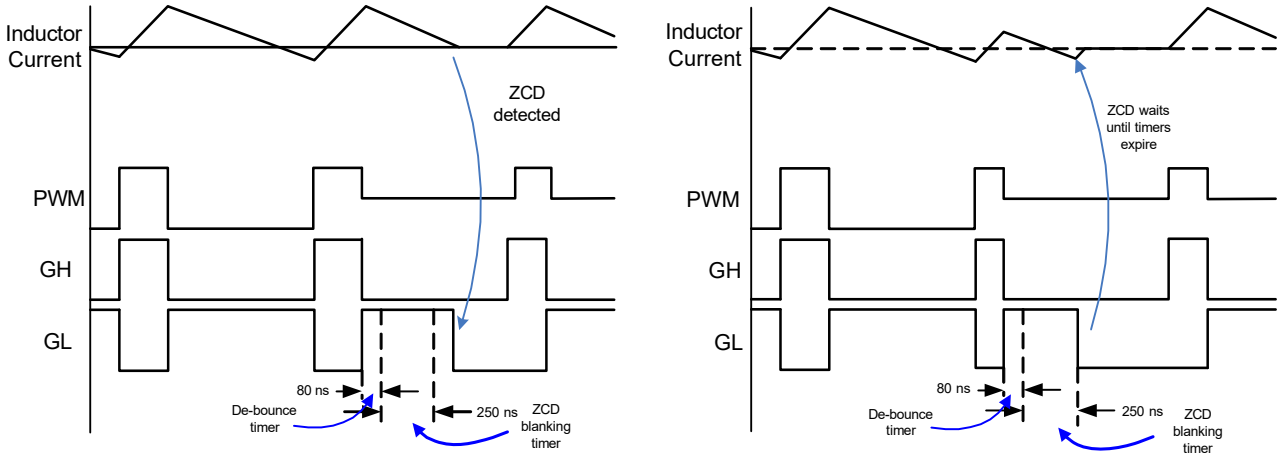


Figure 2. Tri-State Input Logic Timing Diagram(8)

Note:

8. If the Zero Current Detect circuit detects zero current after the ZCD Wait timer period, the GL is driven low by the Zero Current Detect signal. If the Zero Current Detect circuit detects zero current before the ZCD Wait timer period expires, the Zero Current detect signal is ignored and the GL is driven low at the end of the ZCD Wait timer period.

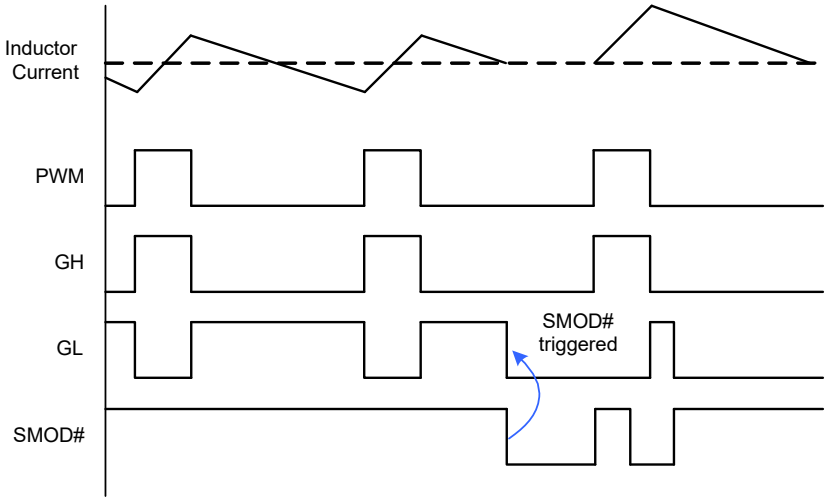


Figure 3. SMOD# Logic Timing Diagram(9)

Note:

9. If the SMOD# input is driven low at any time after the GL has been driven high, the SMOD# Falling edge triggers the GL to go low. If the SMOD# input is driven low while the GH is high, the SMOD# input is ignored.

Use with Controllers with 3-State PWM and No Zero Current Detection Capability:

Table 2. Logic Table: 3-State PWM Controllers with No Zero Cross Detect Function

PWM	SMOD#	GH (Not a Pin)	GL
H	H	H	L
MID	H	L	ZCD
L	H	L	H

This section describes operation with controllers that are capable of 3-states at their PWM output and relies on the AOZ5239QI to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5V or left disconnected. The SMOD# has an internal pull−up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid−state (floating).

Whenever PWM transitions to mid−state, GH turns off and GL turns on (VSWH is pulled low). GL stays on for the duration of the de−bounce timer and ZCD blanking timers. Once these timers expire, the AOZ5239QI monitors the VSWH voltage and turns GL off when VSWH exceeds the ZCD threshold voltage. By turning off the LS MOSFET, the body diode of the LS MOSFET allows positive current to go to zero but prevents negative current conduction.

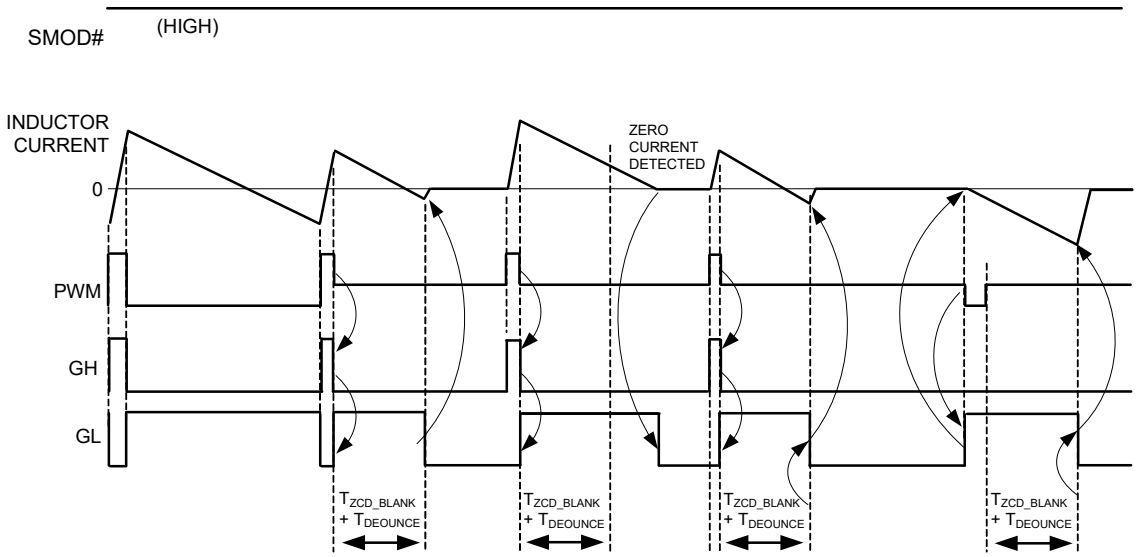


Figure 4. Timing Diagram: 3−state PWM Controller, No ZCD

Use with Controllers with 3-State PWM and Zero Current Detection Capability:

Table 3. Logic Table: 3-State PWM Controllers with ZCD

PWM	SMOD#	GH (Not a Pin)	GL
H	L	H	L
MID	L	L	L
L	L	L	H

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM). The SMOD# pin needs to be pulled low (below VSMOD#_LO).

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the AOZ5239QI to turn off the LS MOSFET. When the controller detects zero current, it needs to set PWM to mid−state, which causes the AOZ5239QI to pull both GH and GL to their off states without delay.

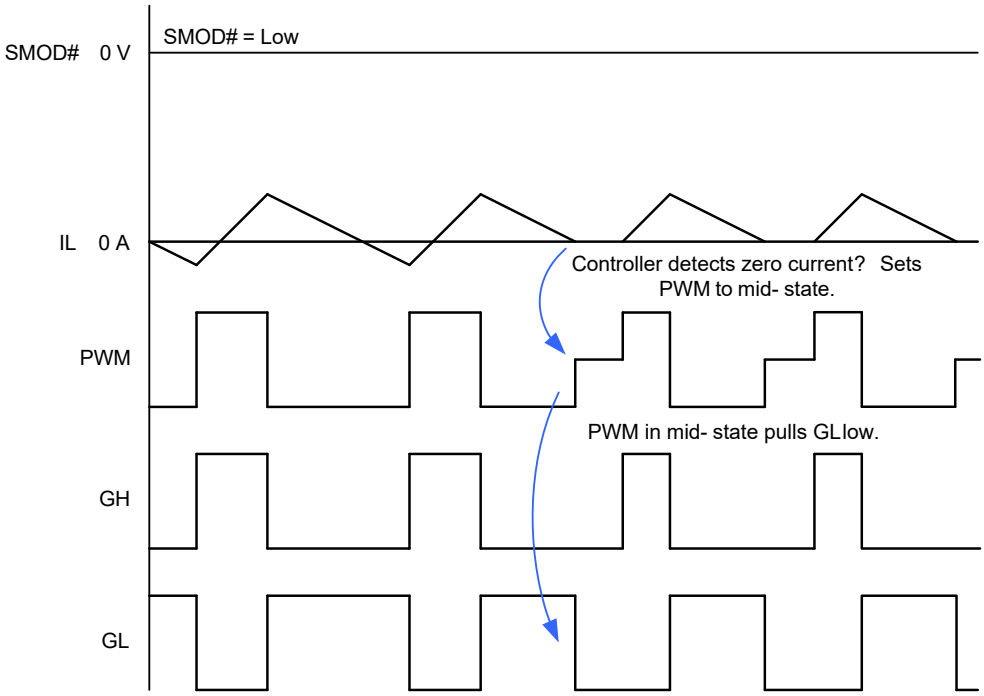


Figure 5. Timing Diagram: 3−state PWM Controller, with ZCD

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V, unless otherwise specified.

Figure 6. Efficiency vs. Load Current

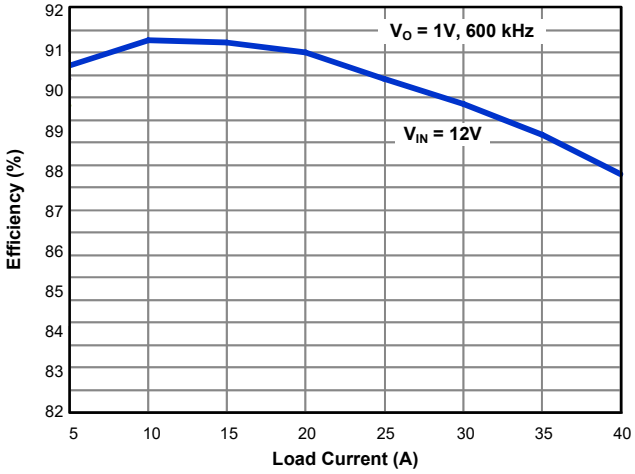


Figure 7. Module Loss Vs. Load Current

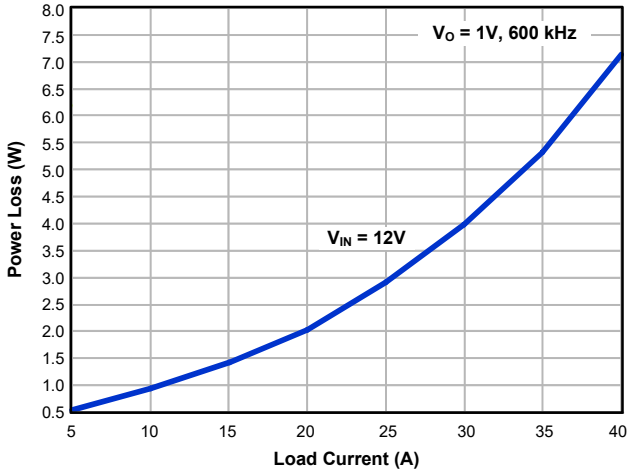


Figure 8. UVLO Threshold vs. Temperature

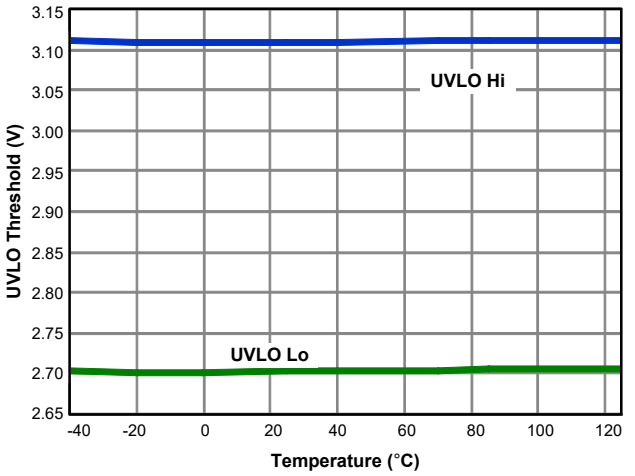


Figure 9. Supply Current vs. Switching Frequency

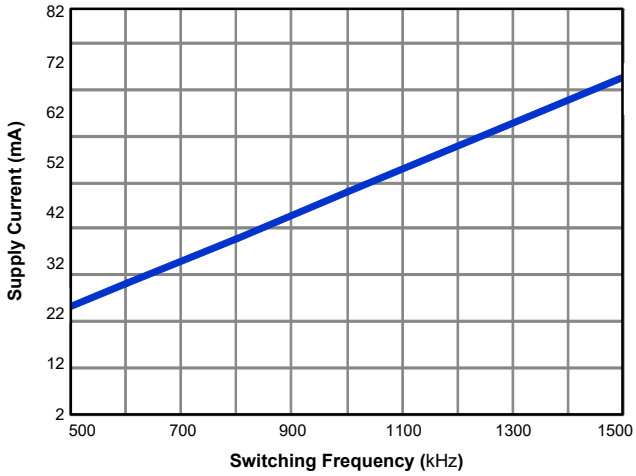


Figure 10. SMOD# Threshold vs. V_{CC}

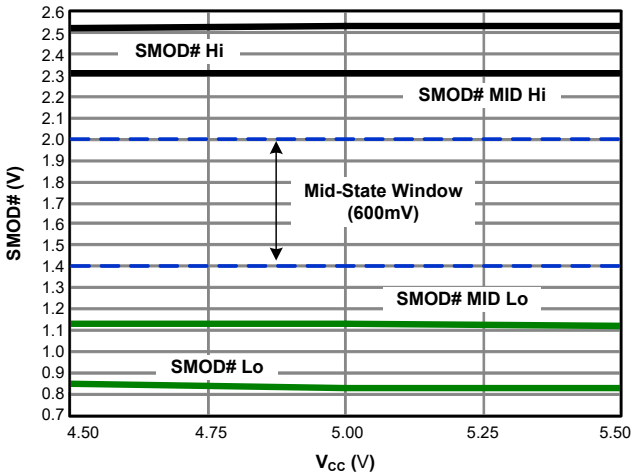
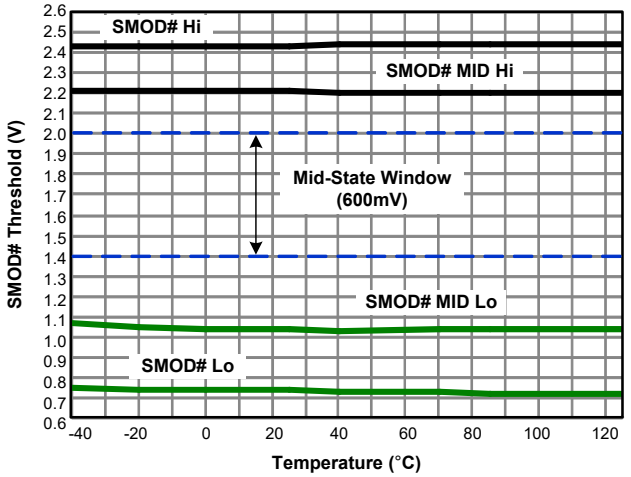


Figure 11. SMOD# Threshold vs. Temperature



Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V, unless otherwise specified

Figure 12. PWM Threshold vs V_{CC}

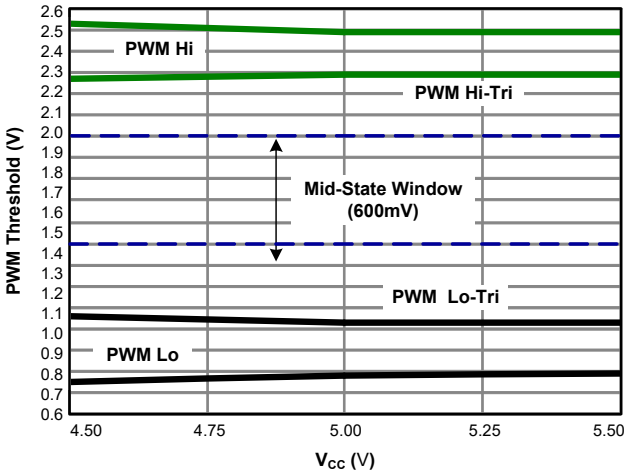


Figure 13. PWM Threshold vs. Temperature

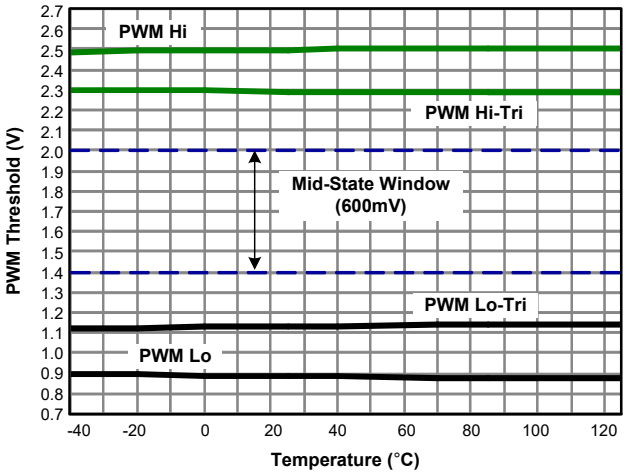
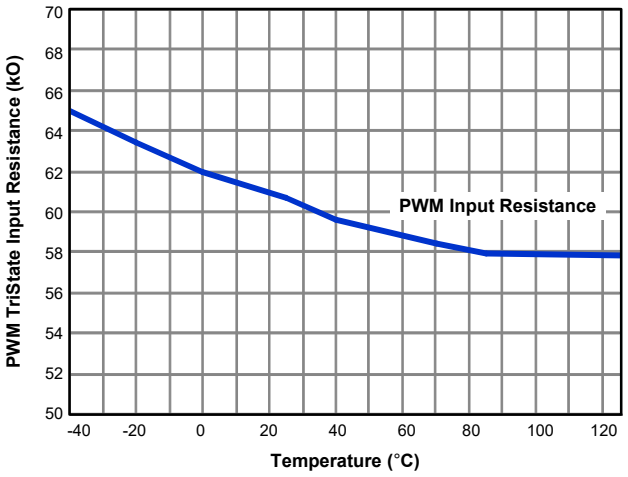


Figure 14. PWM Input Resistance vs. Temperature



Theory of Operation

The AOZ5239QI is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The AOZ5239QI supports numerous application control definitions including Pin Enable and alternately PWM Tristate Control. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

Low-Side Driver

The low−side driver drives an internal, ground−referenced low−RDS(on) N−Channel MOSFET. The voltage supply for the low−side driver is internally connected to the PVCC and PGND pins.

High-Side Driver

The high−side driver drives an internal, floating low−RDS(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH, PHASE) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the AOZ5239QI is starting up, the VSWH pin is at ground, allowing the bootstrap capacitor to charge up to PVCC through the bootstrap diode. When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the VSWH and PHASE pins rise. When the high−side MOSFET is turned fully on, the switch node will settle to VIN and the BOOT pin will settle to VIN + PVCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BOOT}) and an integrated diode to provide current to the HS Driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the bootstrap capacitor. An optional 1 to 4Ω resistor in series with C_{BOOT} is recommended to decrease VSWH overshoot.

Power Supply Decoupling

The AOZ5239QI will source relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (PVCC), a low−ESR capacitor should be placed near the PGND pins. A multi layer ceramic capacitor (MLCC) between 1µF and 4.7µF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1µF ceramic capacitor should be placed on this pin in close proximity to the AOZ5239QI. It is good practice to separate the VCC and PVCC decoupling capacitors with a resistor (10Ω typical) to avoid coupling driver noise to the analog and digital circuits that control driver function (See Figure 1).

Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETs which could result in a decrease in the power conversion efficiency or damage to the device.

The AOZ5239QI prevents cross conduction by monitoring the status of the MOSFET gates and applying the appropriate amount of non−overlap time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the low−side MOSFET gate (GL) starts to go low after a propagation delay (t_{pdlGL}). The time it takes for the low−side MOSFET to turn off is dependent on the low−side MOSFET gate charge. The high−side MOSFET source terminal (VSWH) begins to rise following a fixed time ($tpdh_{VSWH}$) after the GL voltage falls below the low−side MOSFET gate threshold.

When the PWM input pin is driven low, the LOW−side MOSFET drain terminal (VSWH) starts to go low after a propagation delay ($tpdl_{VSWH}$). The time it takes for the high−side MOSFET to turn off is dependent on the high−side MOSFET gate charge. The low−side MOSFET gate begins to rise after a fixed time ($tpdh_{GL}$) following the VSWH voltage falling edge below the 1V.

PWM Input

The PWM Input pin is a tri−state input used to control the HS MOSFET ON/OFF state. In conjunction with SMOD# pin, it also determines the state of the LS MOSFET. See Table1 for logic operation. The PWM in some cases must operate with frequency programming resistances to ground. These resistances can range from 10k to 300k depending on the application. When SMOD# is set to > VSMOD#_HI or to < VSMOD#_LO, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin. If SMOD# is set such that: VSMOD#_LO < SMOD# < VSMOD#_HI which means, SMOD# is in Mid−State, the undriven PWM pin will be set by its internal resistor network to its Mid-State voltage.

Disable Input (DISB#)

The DISB# pin is used to disable the High−Side MOSFET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Under-voltage Lockout

The VCC pin is monitored by an Under-voltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the AOZ5239QI.

Table 4. UVLO/DISB# Logic

UVLO	DISB#	DRIVER STATE
L	X	DISABLE (GL=GH=0)
H	L	DISABLE (GL=GH=0)
H	H	ENABLE (See Table 1)
H	OPEN	DISABLE (GL=GH=0)

Thermal Warning / Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN} Threshold (Temperature), the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops in accordance to the T_{HWN_HYS}, below T_{THWN}, the THWN pin will re-enter the open-drain output state. If the driver temperature exceeds T_{HDN} Temperature threshold, the part will enter thermal shutdown and turn off both upper and lower MOSFETs. Once the temperature falls in accordance to the T_{HDN_HYS}, below T_{HDN}, the part will resume normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven high, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low during the PWM cycle it prioritizes control of the low side MOSFET to allow discontinuous mode operation. The AOZ5239QI has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid−state. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.

PCB Layout Guidelines

AOZ5239QI is a high current module rated for operation up to 2 MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the HS MOSFET, LS MOSFET and the input bypass capacitor Cin. The PCB design is somewhat simplified because of the optimized pin out in AOZ5239QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS MOSFET, output inductor and output capacitor Cout is the next critical parameter, this requires second layer or “Inner 1” should always be an uninterrupted GND plane with sufficient GND vias placed as close as possible to by-pass capacitors GND pads.

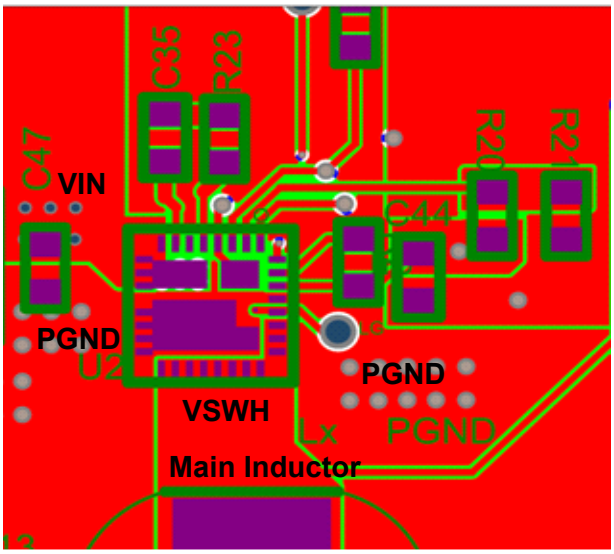


Figure 15. Top Layer of Demo Board, VIN, VSWH and PGND Copper Planes

As shown on Fig. 15, the top most layer of the PCB should comprise of copper flooding for the primary AC current loop that run along the VIN copper plane originating from the bypass capacitors which are mounted to a large PGND copper plane, also on the top most layer of the PCB. These copper planes also serve as heat dissipating elements as heat simply flows down to the VIN exposed pad and onto the top layer VIN copper plane which fans out to a wider area moving away from the 5x5 QFN package. Adding vias will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only

Due to the optimized bonding technique used on the AOZ5239QI internal package, the VIN input capacitors are optimally placed for AC current activities on both the primary and complimentary current loops. The return path of the current during the complimentary period flows through a non interrupted PGND copper plane that is symmetrically proportional to the VIN copper plane.

Due to the PGND exposed pad, heat is optimally dissipated simply by flowing down through the vertically structured lower MOSFET, through the exposed PGND pad and down to the PCB top layer PGND copper plane that also fans outward, moving away from the package.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spikes appear at the VSWH terminal which are caused by the large internal dI/dts produced through the in package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

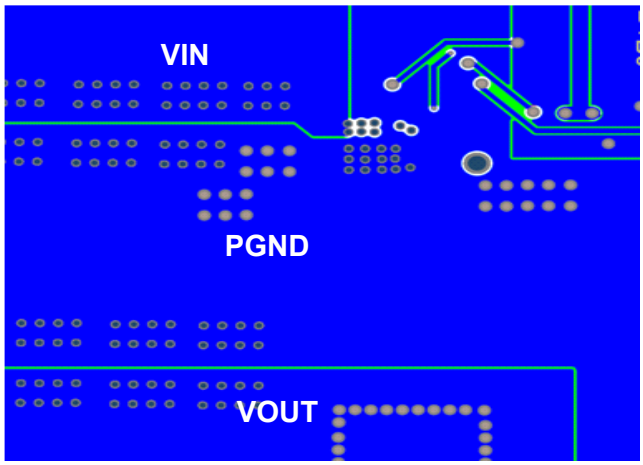


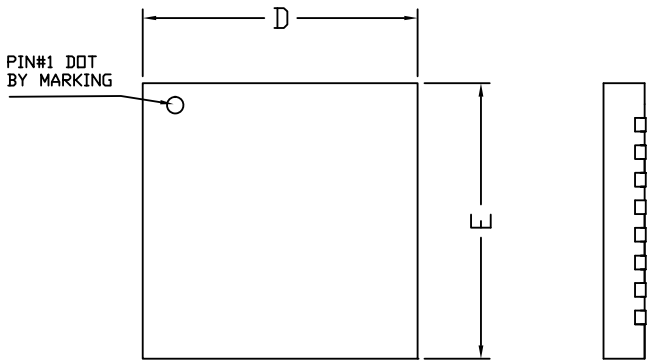
Figure 16. Bottom Layer PCB Layout

The AOZ5239QI can be operated at a switching frequency of up to 2 MHz. This implies that the inherent capacitive parameters of the High Side and Low Side MOSFETs need to be charged and discharge on each and every cycle. Due to the AC currents flowing in and out of the Input Capacitors, the exposed pads (VIN and PGND) would tend to heat up, hence requiring thermal venting.

Positioning vias through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

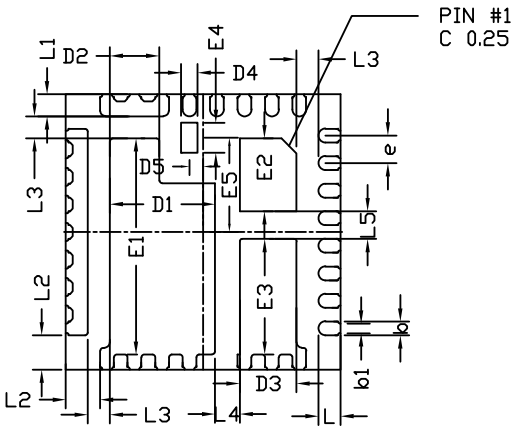
The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter vias. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

Package Dimensions, QFN5x5A_31L EP3_S

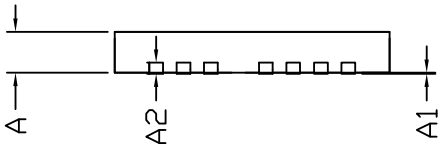


Top View

Side View

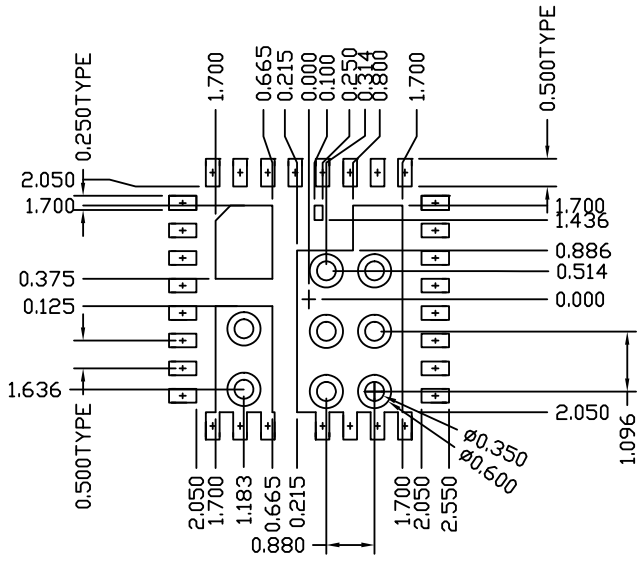


Bottom View



Side View

Recommended Land Pattern Via Placements



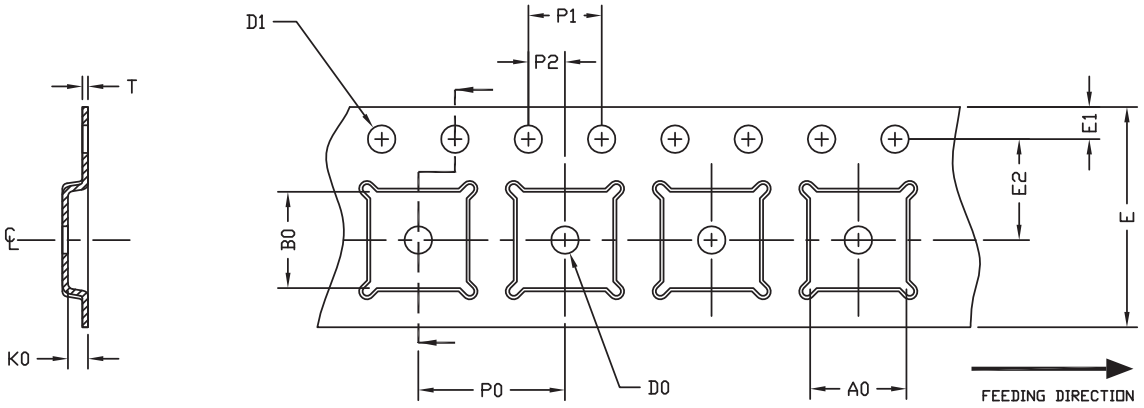
UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2		0.2REF			0.008REF	
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e		0.50BSC			0.02BSC	

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x5A_31L_EP3_S

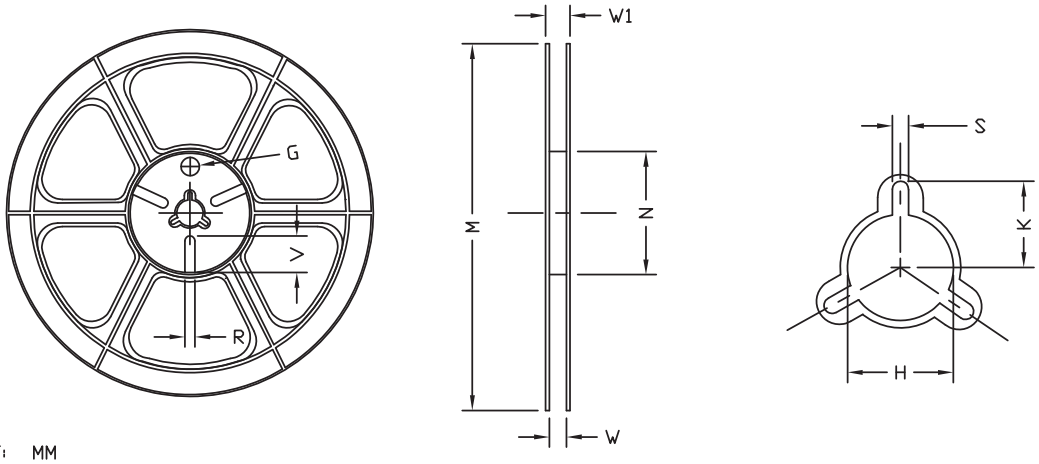
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

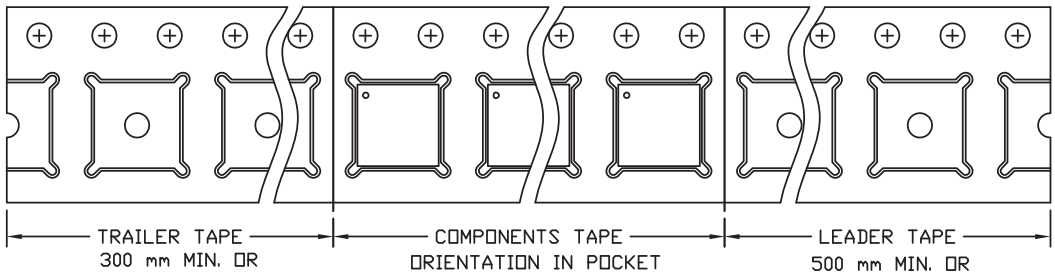


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

Leader/Trailer & Orientation

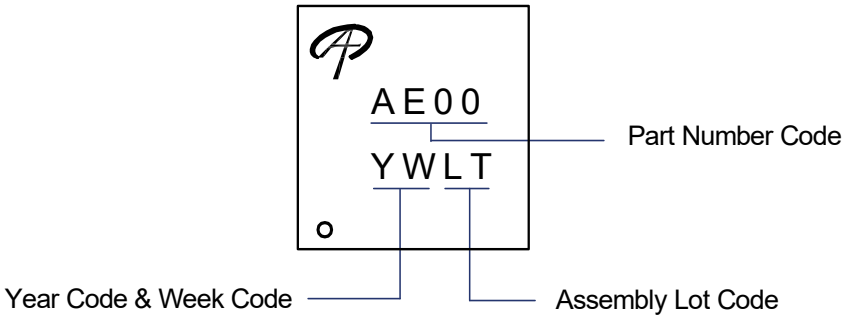
NORMAL



Unit Per Reel:
3000pcs

Part Marking

AOZ5239QI
(5mm x 5mm QFN)



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