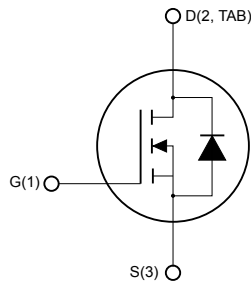
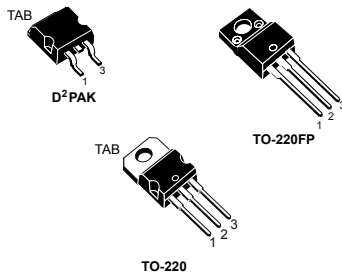


N-channel 500 V, 300 mΩ typ., 12 A MDmesh Power MOSFETs in a D²PAK, TO-220 and TO-220FP packages



NG1D2TS3



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STB12NM50T4	500 V	350 mΩ	12 A
STP12NM50			
STP12NM50FP			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Product status link

[STB12NM50T4](#)
[STP12NM50](#)
[STP12NM50FP](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220	TO-220FP	
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	12	12 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	7.5	7.5 ⁽¹⁾	
I _{DM} ⁽²⁾	Drain current pulsed	48	48 ⁽¹⁾	A
P _{TOT}	Total power dissipation at T _C = 25 °C	160	35	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)		2.5	kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
T _J	Operating junction temperature range	-65 to 150		°C
T _{stg}	Storage temperature range			°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 12 A, di/dt ≤ 400 A/μs, V_{DD} = 80% V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	2.78		3.57	°C/W
R _{thj-a}	Thermal resistance junction-ambient	62.5			°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	35			°C/W

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not repetitive (pulse width limited by T _J max)	6	A
E _{AS}	Single-pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AS} , V _{DD} = 50 V)	400	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			10	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		300	350	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1000	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	20	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	90	-	pF
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	20	-	ns
t_r	Rise Time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	10	-	ns
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	28	-	nC
Q_{gs}	Gate-source charge	(see Figure 14. Test circuit for gate charge behavior)	-	8	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC
R_g	Gate input resistance	$f = 1\text{ MHz}$, gate DC Bias = 0, test signal level = 20 mV, open drain	-	1.6	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 12\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	270		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	2.23		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	16.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	340		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	3		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	18		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and TO-220

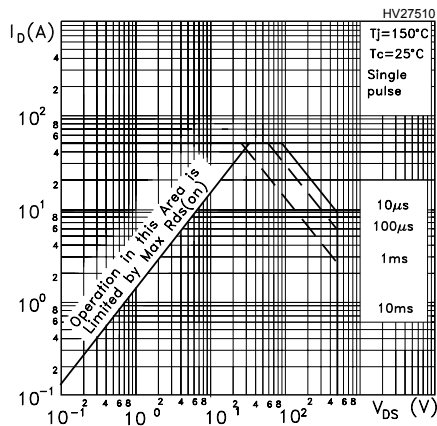


Figure 2. Thermal impedance for D²PAK and TO-220

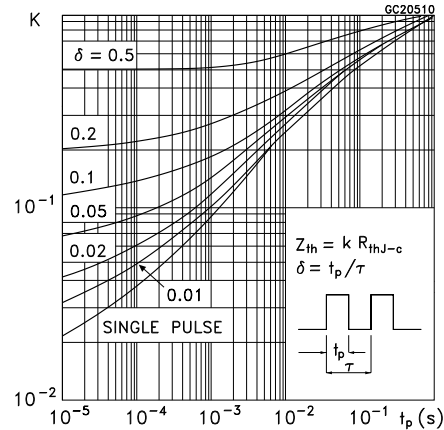


Figure 3. Safe operating area for TO-220FP

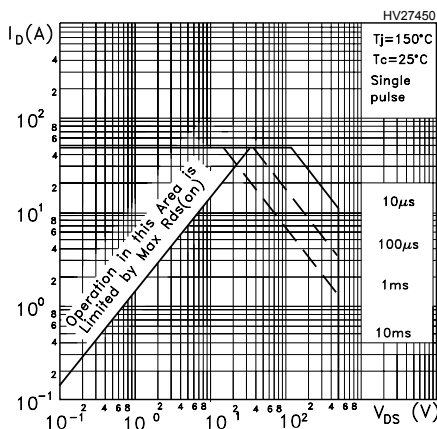


Figure 4. Thermal impedance for TO-220FP

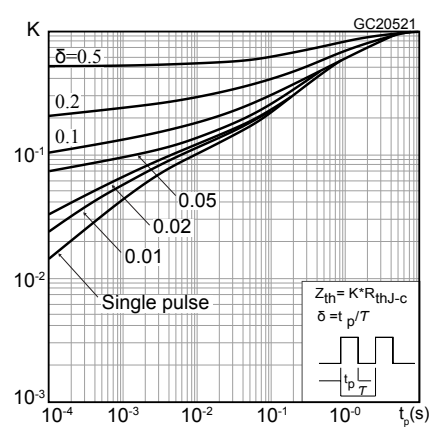


Figure 5. Output characteristics

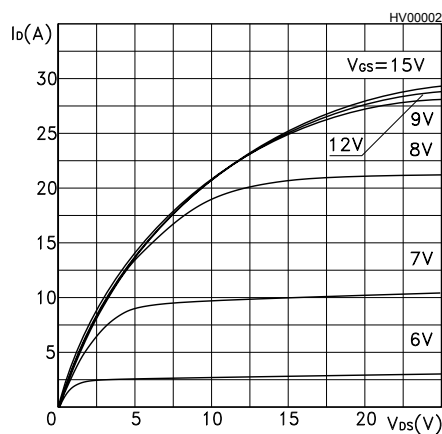


Figure 6. Transfer characteristics

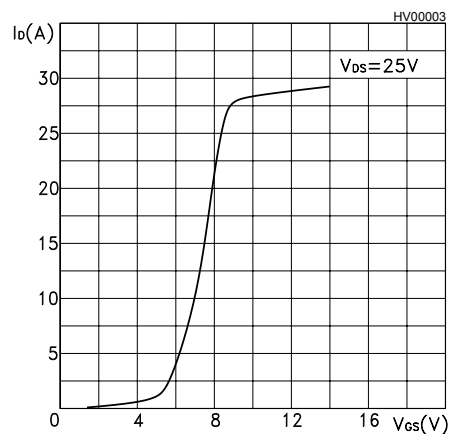
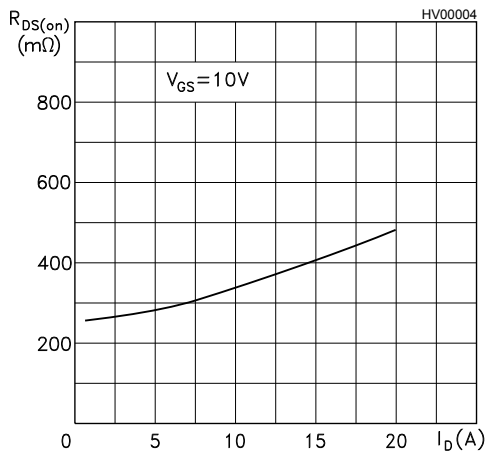
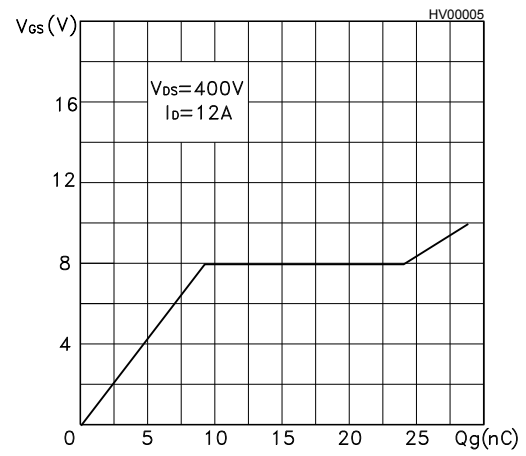
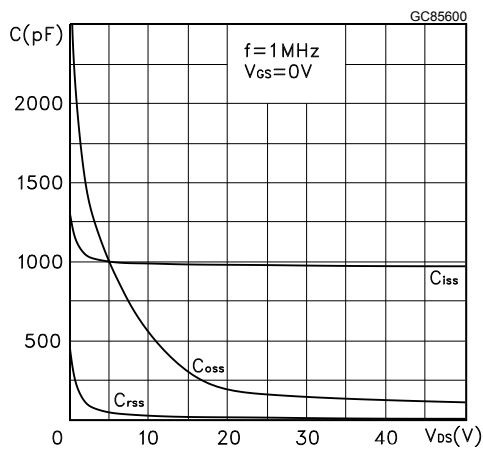
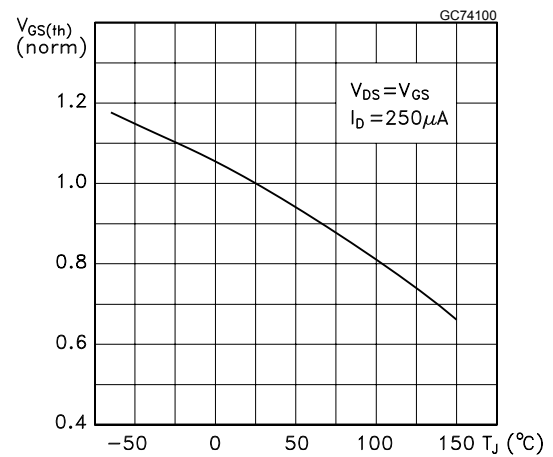
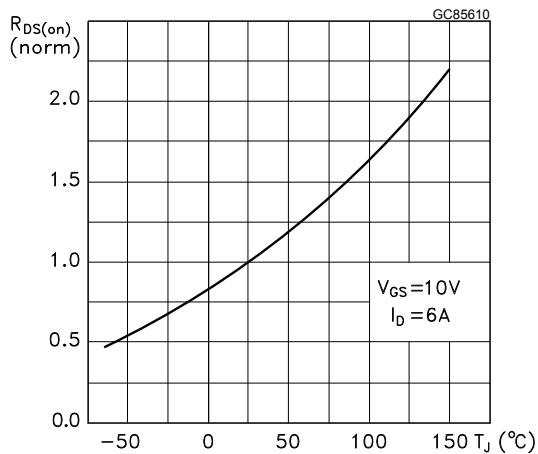
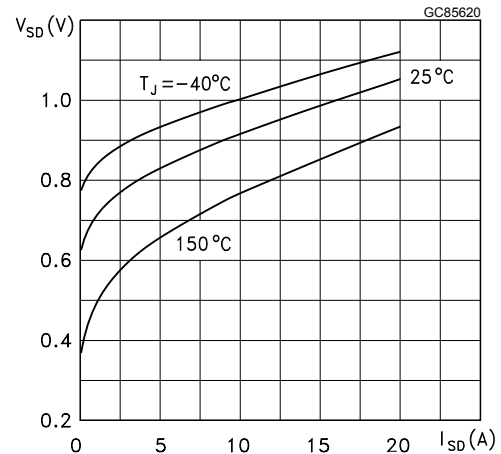
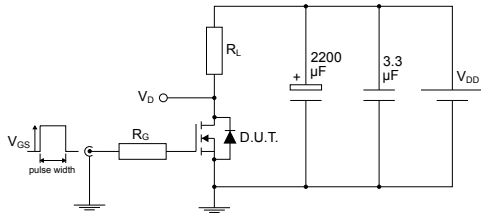
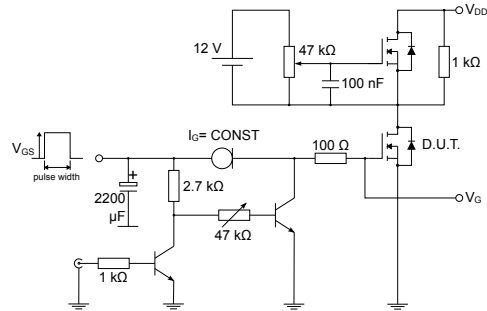


Figure 7. Static drain-source on-resistance

Figure 8. Gate charge vs gate-source voltage

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

Figure 12. Source-drain diode forward characteristics


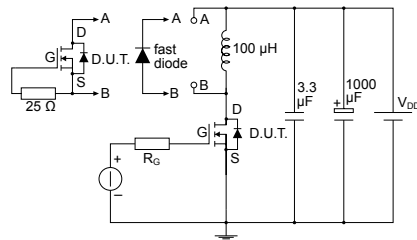
3 Test circuits

Figure 13. Test circuit for resistive load switching times


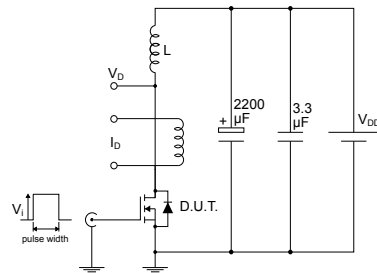
AM01468v1

Figure 14. Test circuit for gate charge behavior


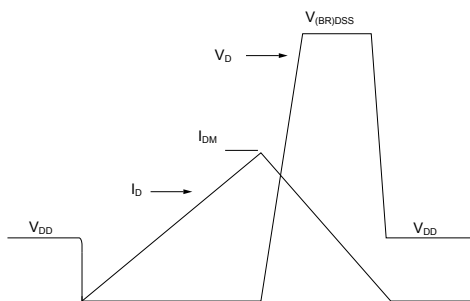
AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


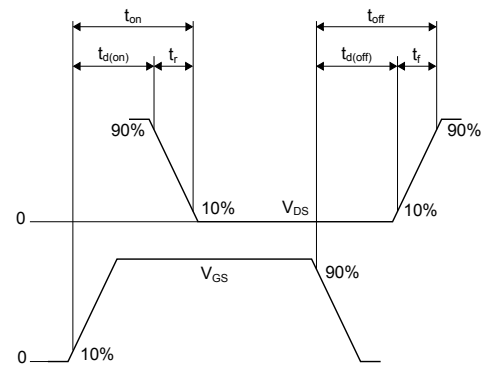
AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


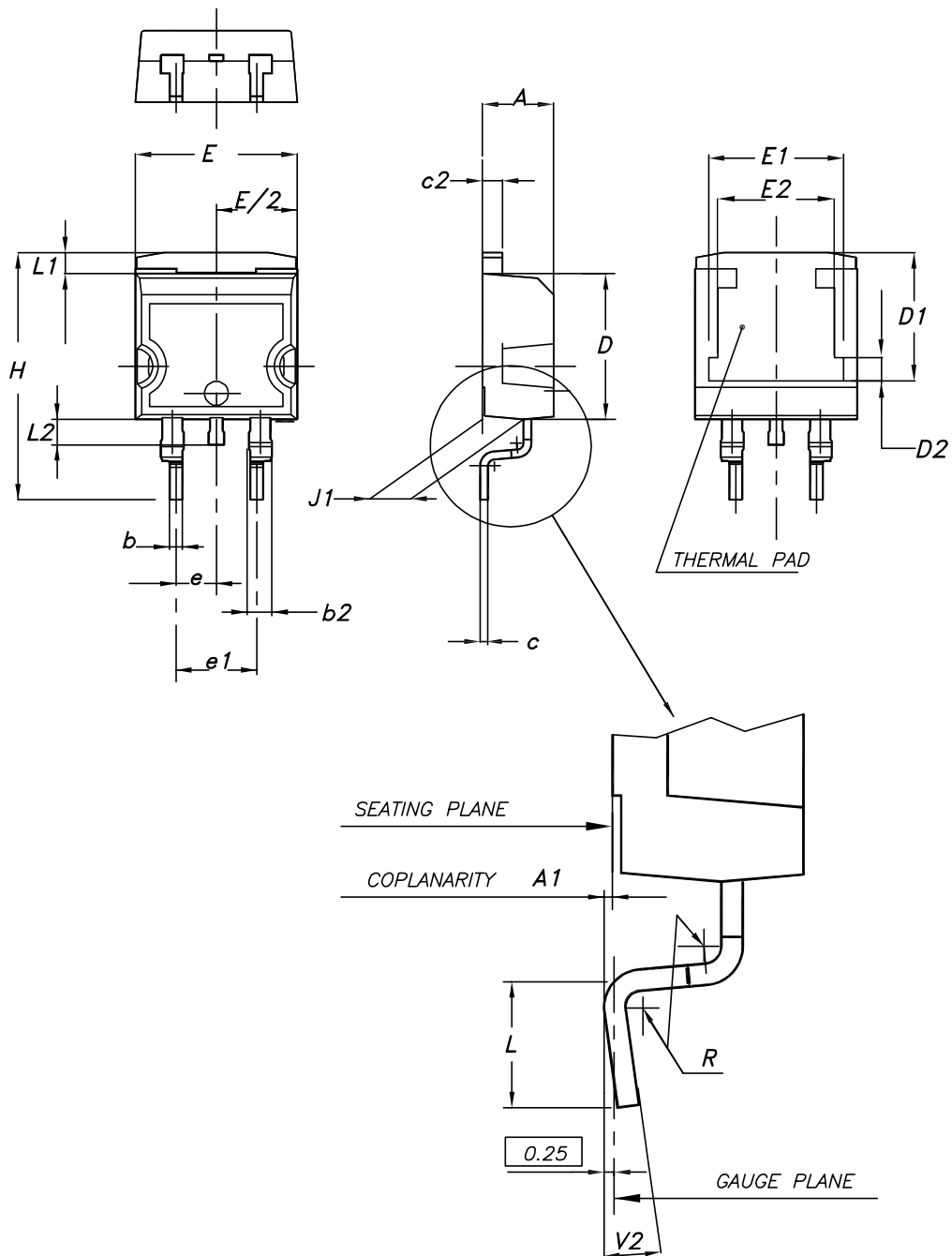
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline

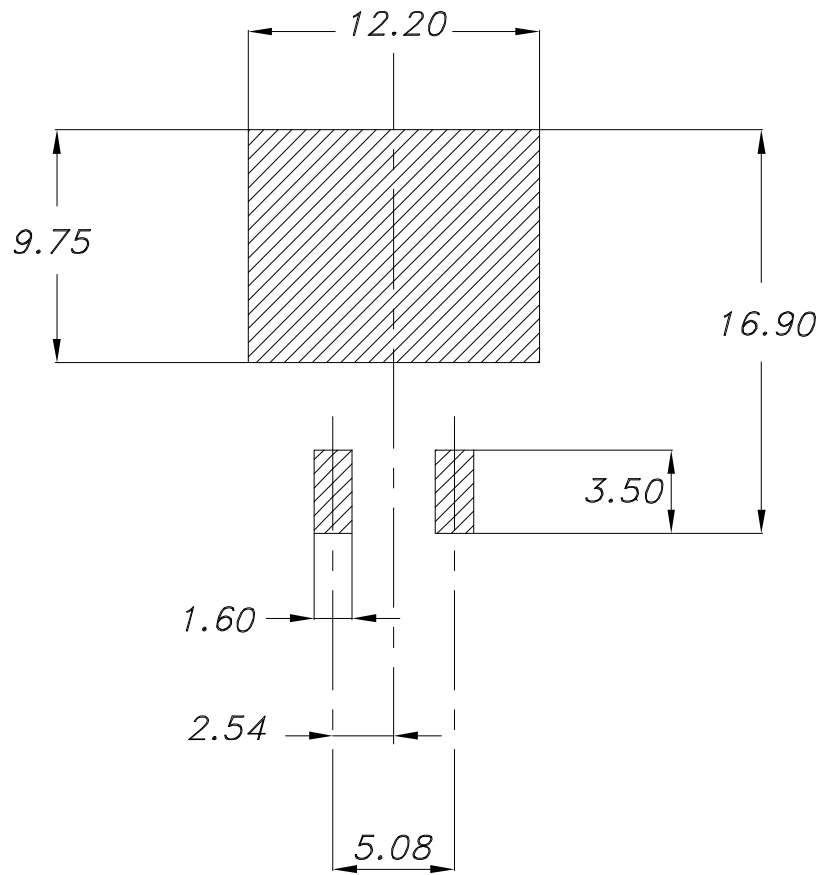


0079457_26

Table 7. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

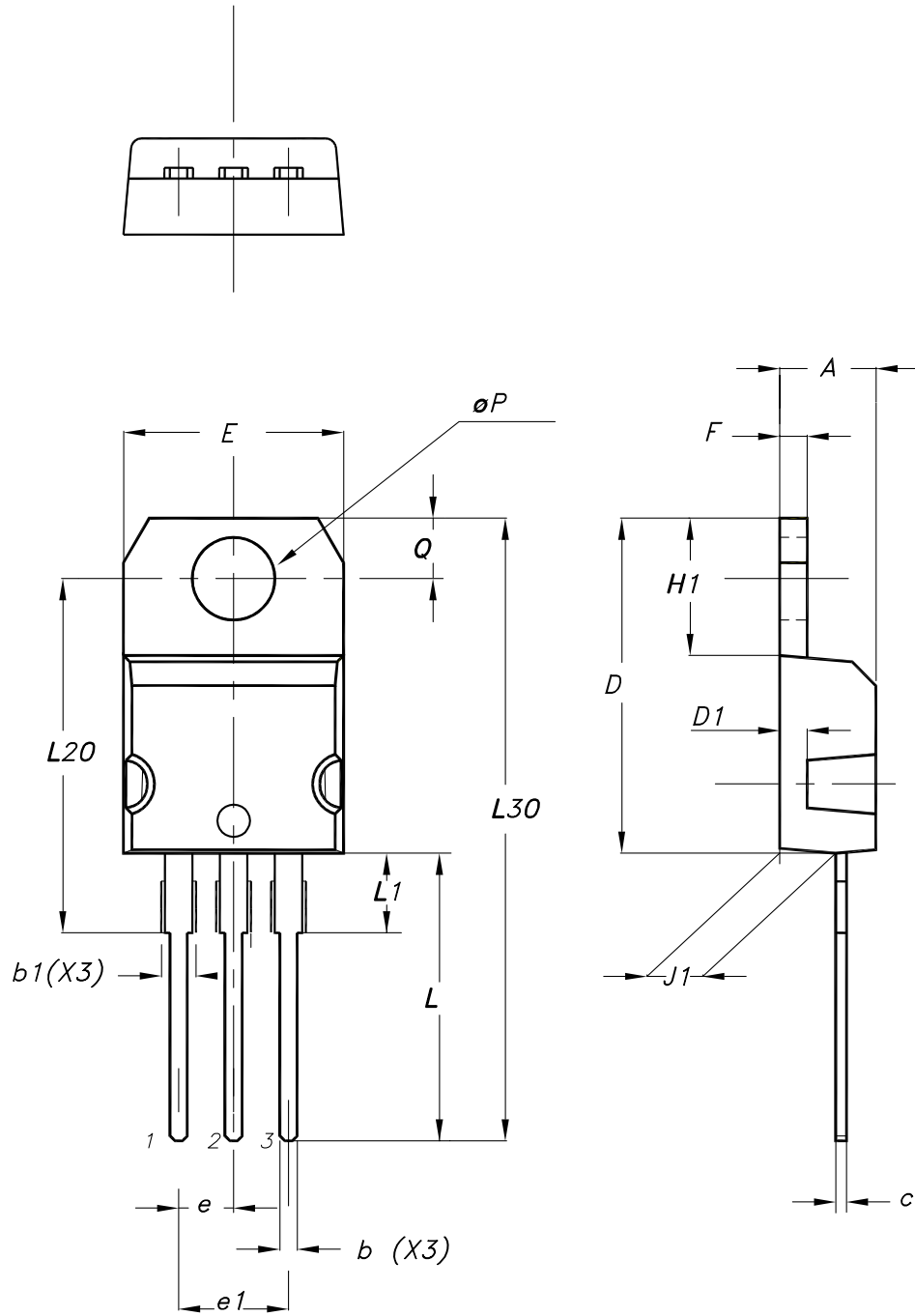
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint_26

4.2 TO-220 type A package information

Figure 21. TO-220 type A package outline



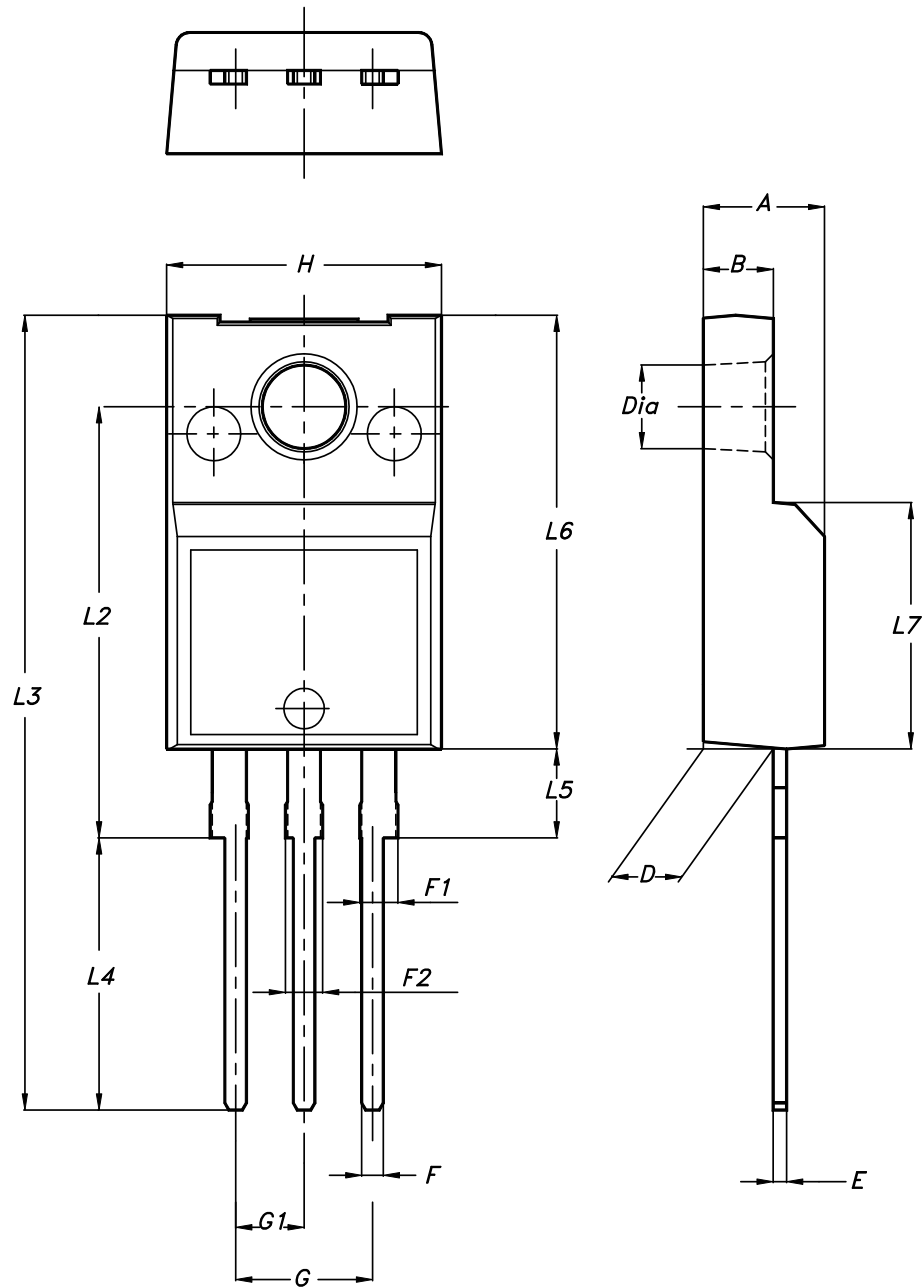
0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 TO-220FP package information

Figure 22. TO-220FP package outline



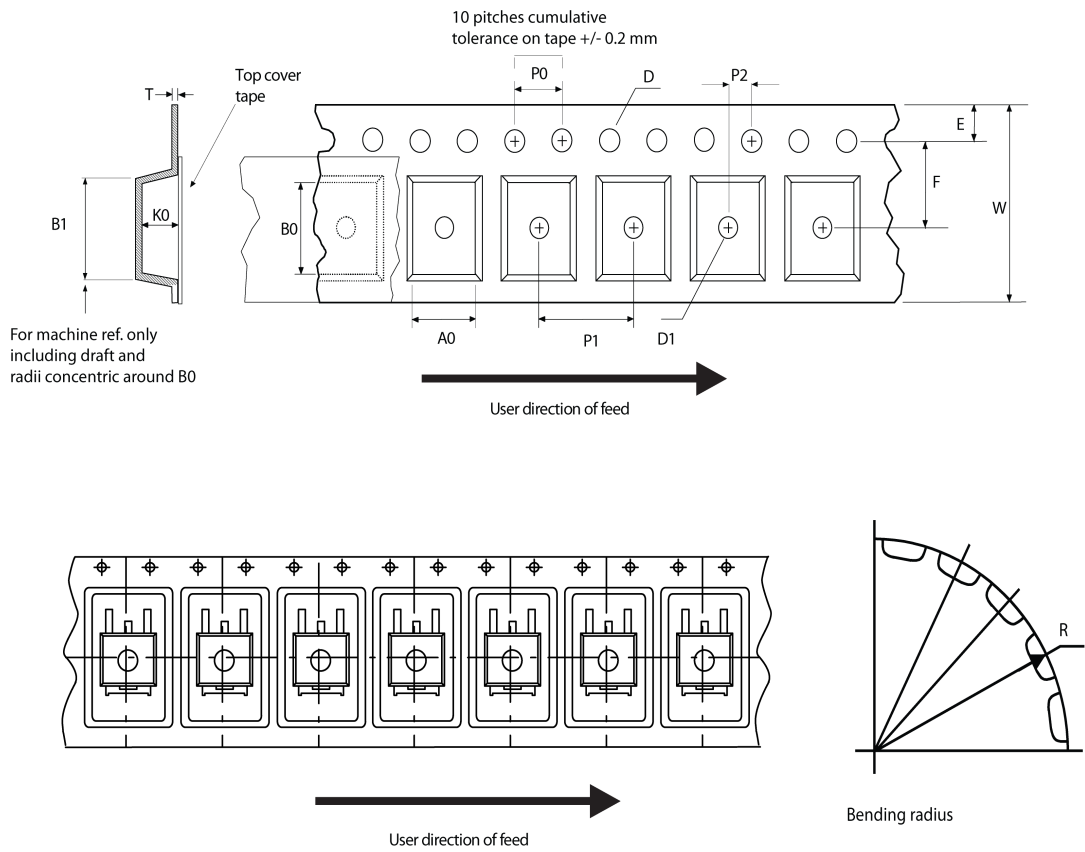
7012510_Rev_13_B

Table 9. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.4 D²PAK packing information

Figure 23. D²PAK tape outline



AM08852v1

Figure 24. D²PAK reel outline


AM06038v1

Table 10. D²PAK tape and reel mechanical data

Tape			Reel			
Dim.	mm		Dim.	mm		
	Min.	Max.		Min.	Max.	
A0	10.5	10.7	A		330	
B0	15.7	15.9	B	1.5		
D	1.5	1.6	C	12.8	13.2	
D1	1.59	1.61	D	20.2		
E	1.65	1.85	G	24.4	26.4	
F	11.4	11.6	N	100		
K0	4.8	5.0	T		30.4	
P0	3.9	4.1	Base quantity Bulk quantity			
P1	11.9	12.1				1000
P2	1.9	2.1				1000
R	50					
T	0.25	0.35				
W	23.7	24.3				

5 Ordering information

Table 11. Order codes

Order codes	Marking	Package	Packing
STB12NM50T4	B12NM50	D ² PAK	Tape and reel
STP12NM50	P12NM50	TO-220	Tube
STP12NM50FP	P12NM50FP	TO-220FP	Tube

Revision history

Table 12. Document revision history

Date	Revision	Changes
14-Mar-2004	8	Preliminary version
15-Feb-2006	9	New voltage value on first page at t_{jmax} .
05-Apr-2006	10	Inserted ecopack indication
27-Jul-2006	11	New template, no content change
22-Oct-2020	12	<p>The part number STB12NM50-1 have been moved to a separate datasheet and the document has been updated accordingly.</p> <p>Updated cover page.</p> <p>Updated Section 1 Electrical ratings and Section 2 Electrical characteristics.</p> <p>Added Section 5 Ordering information.</p> <p>Minor text changes.</p>

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	D ² PAK (TO-263) type A package information	8
4.2	TO-220 type A package information	11
4.3	TO-220FP package information	13
4.4	D ² PAK packing information	15
5	Ordering information	17
	Revision history	18

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved