Keywords: jitter, gaussian, random, RJ, deterministic, cycle to cycle, adjacent cycle, duty cycle distortion, pulse width distortion, inter-symbol, bit error rate, BER, ber

APPLICATION NOTE 1916

An Introduction to Jitter in Communications Systems

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Abstract: This introduction to jitter presents definitions for various jitter types including the random jitter types: Gaussian, cycle-to-cycle, adjacent cycle; and deterministic jitter types: duty cycle distortion, pulse width distortion, pulse skew and data dependent (pattern) jitter. The application note also discusses the relationship between the various jitter components and system Bit Error Rate (BER).

What is Jitter?

The SONET standard states that "Jitter is defined as the short-term variations of a digital signal's significant instants from their ideal positions in time. Significant instants could be (for example) the optimum sampling instants." The Fiber Channel standard simply defines jitter as "The deviation from the ideal timing of an event."

In short, the term "jitter" describes timing errors within a system. In a communications system, the accumulation of jitter will eventually lead to data errors.

The parameter that is of most value to the system user is the frequency of occurrence of these data errors, normally referred to as the Bit Error Rate (BER). We'll discuss BER in more detail later.

First, some definitions. The basic jitter types and definitions are listed in **Table 1** below. Some jitter types have a number of commonly used terms describing the same measurement. Others have terms describing different measurement methods for the same jitter type. Where multiple terms are used to describe the same jitter type, these are listed together.

Table 1. Terms and Definitions Associated with Jitter Measurements

Jitter Term	Definition	Additional Information
Jitter	In addition to the definitions above, jitter is composed of two basic types: random and deterministic.	
Random Jitter (RJ)	Jitter that is not bounded and can be described by a Gaussian probability distribution. Random jitter is characterized by its	The principal source is Gaussian (white) electrical noise within system components. Electrical noise interacts with the

	standard deviation (rms) value.	slew rate of signals to produce timing errors at the switching points.
Random	RJ measurement method. A probability distribution based on the difference in time between an actual clock edge and its ideal (intended) position.	Although two measurements of the same source, random and cycle to cycle jitter are not equivalent. Cycle to cycle jitter has frequency dependant terms and, compared to random jitter measurements, will accentuate high frequency jitter sources while rejecting low frequency sources. The random jitter measurement is independent of frequency.
Cycle to Cycle Adjacent Cycle	RJ measurement method. A probability distribution based on the difference in the period measured between one clock cycle and an adjacent cycle.	
Deterministic Jitter (DJ)	Jitter with a non-Gaussian probability density function. Always bounded in amplitude and with specific causes. DJ is characterized by its bounded, peak-to-peak, value.	Sources are generally related to imperfections in the behavior of a device or transmission media but also may also be due to EMI, crosstalk, grounding problems.
Duty Cycle Distortion Pulse Width Distortion Pulse Skew	DJ component. Deviation in duty cycle value from the ideal (intended) value. In many serial data systems this equates to a deviation in bit time between a 1 bit and a 0 bit. May also defined as the difference in propagation delay between low to high and high to low delay times.	Source is commonly timing differences between rising and falling edges within a system. May also be caused by ground shifts in single ended systems.
Data Dependant Jitter Pattern Jitter Inter-Symbol Interference	DJ component. Timing errors that vary with the data pattern used. Data dependant and Pattern jitter are used to describe the effect of jitter in the time domain. Inter-Symbol Interference is more commonly applied to frequency domain measurements i.e., the spreading of a signal peak as would be seen on a spectrum analyzer.	Primary source is component and system bandwidth limitations. Higher frequency signals have less time to settle than lower frequency ones. This leads to changes in the start conditions for transitions at different frequencies and produces timing errors dependent on the data pattern being applied.
Sinusoidal Jitter Periodic Jitter	DJ component. Jitter that has a sinusoidal (or periodic) form and is related	Source is interference from signals that are related to the data pattern. Ground

	to (correlates to) the data pattern.	bounce and other power supply variations are common causes although the levels of sinusoidal jitter normally encountered are very low.
Uncorrelated bounded Jitter	DJ component. Jitter that is bounded in amplitude and uncorrelated (to the data pattern).	Commonly sinusoidal in nature, source is interference from other signal sources either within the system or external to it. Sources include EMI, capacitive and inductive coupling and power supply switching noise.
Total Jitter (TJ)	The summation (or convolution) of deterministic and random jitter. Total jitter is the peak to peak value obtained.	TJ = DJ + n × RJ where n = number of standard deviations corresponding to the required BER. This summation is usually applied due to it's simplicity although this method over-estimates the actual BER since the maximum RJ errors will not always coincide with maximum DJ error. A probabilistic (convolved) summation of the two jitter types would produce a more accurate solution though the application of this would require knowledge of the DJ modulation waveform.
Mapping Jitter	System level jitter component of DJ type. Jitter due to mapping of data from one transmission standard to another when bit stuffing has occurred during the mapping process.	Gaps are left in the recovered signal after de-mapping. Phase locked loops (PLLs) are used to smooth the resulting gaps but a certain amount of jitter remains.
Pointer Jitter	System level jitter component of DJ type. Jitter resulting from the application of a SONET signal containing defined sequences of pointer activity to a demultiplexer.	
Wander Jitter	System level jitter component of DJ type. Low	Principal source is system temperature variations.

	frequency timing errors less than 10Hz in frequency (SONET).	
Jitter Transfer Jitter Gain	Ratio of jitter on output signal to jitter applied on input signal.	Used to quantify the jitter accumulation performance of data retiming devices: regenerators, PLLs.
Jitter Tolerance	Amount of input jitter a receiver must tolerate without violating system BER specifications.	Can be split into Random Jitter Tolerance and Deterministic Jitter Tolerance.
Unit Interval (UI)	Time period equivalent to 1 bit time in a serial data stream.	Reciprocal of baud rate. Jitter specifications are often quoted in multiples of UI.

How Does Jitter Lead to Data Errors?

Information is extracted from serial data streams by sampling the data signal at specific instants. Ideally these sampling instants would always occur at the centre of a data bit time, equidistant between two adjacent edge transition points. The presence of jitter changes the edge positions with respect to the sampling point. An error will then occur when a data edge falls on the wrong side of a sampling instant.

As has been stated in Table 1, the total jitter can be expressed as the sum of deterministic jitter and a number of standard deviations of random jitter at any particular error probability value. Random jitter is defined above as jitter which can be described by a Gaussian probability distribution. Gaussian distributions are symmetrical about a mean value. One standard deviation (1σ) is defined as the window which contains 68.26% of a population to one side of the mean. **Table 2** lists multiples of σ with the proportion of total population applicable to each.

Table 2. Proportion of Total Population vs. Standard Deviation in a Gaussian Distribution

Limit	Proportion of Population Within Limits
±1σ	68.2689%
±2σ	95.45%
±3σ	99.73%
±4σ	99.99367%
±5σ	99.9999427%
±6σ	100-1.973 × 10^{-7}%
±7σ	100-2.5596 × 10^{-10}%
±8σ	100-1.24419 × 10^{-13}%
±9σ	100-2.25718 × 10^{-17}%
±10σ	100-1.53398 x 10^{-21}%

The result of the summation of deterministic and random jitter is another probability distribution, an example of which is shown in **Figure 1**. The distribution plots probability against timing error magnitude and is characterized by a having a centre portion, which represents the deterministic jitter content, and outer portions which are the tails of the (random jitter) Gaussian distribution. The shape of distribution

shown is referred to as a bimodal response.

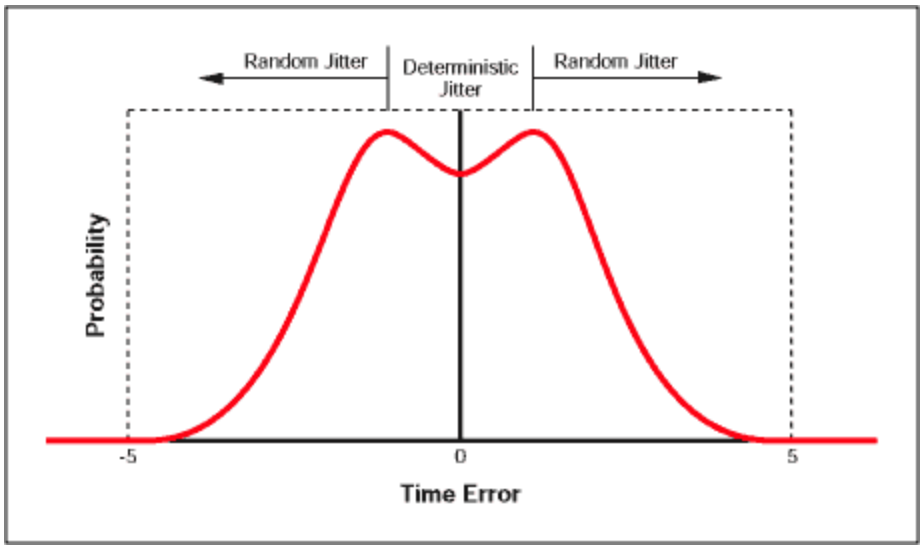

Figure 1. Probability histogram showing deterministic and random components.

Adding the jitter probability distribution of Figure 1 to a data stream effectively modulates the data edge positions with respect to the sampling instant. This is illustrated in **Figure 2**, which shows an ideal eye diagram with probability histograms superimposed on the data transition points. The probability of a data error associated with the sampling instant is the sum of the probabilities that either the first data transition will arrive too late or the second data transition will arrive too early. This probability is denoted by the shaded portion under the curves at the sampling point in Figure 2.

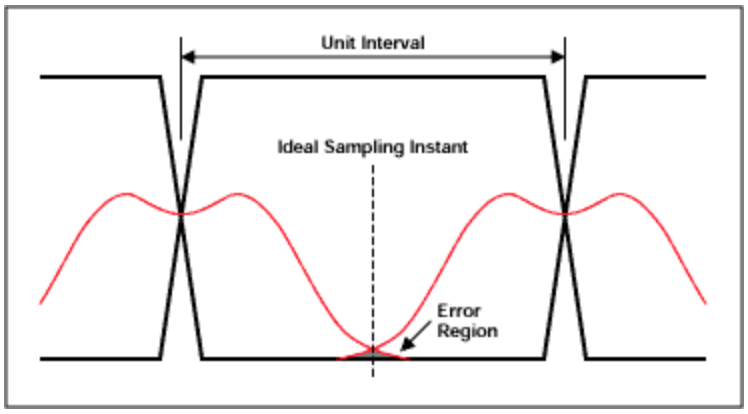

Figure 2. Ideal eye diagram with data transition time probability histograms.

To find the probability of a data error occurring, the sum of the probabilities of either data edge being in error must be multiplied by the probability of a transition actually occurring. The latter is represented by the average transition density and assumed to be equal to 50% for a typical data stream.

By way of an example, consider a data stream with 0.3UIp-p total deterministic jitter (which includes all non-Gaussian timing error sources) and 0.05UI rms random jitter. The maximum allowable jitter is 1UIp-p; this is the amount of jitter an ideal receiver would tolerate before an error occurs (see note below). Using the expression of equation 1

$$DJ(pk) + n \times RJ(rms) = TJ(pk)$$

and substituting TJ = 0.5UI(pk), DJ = 0.15UI(pk) and RJ = 0.05UI(rms), we obtain n = 7. This is the number of standard deviations (σ) of random jitter that will produce a data error. For a Gaussian distribution, 1.28×10^{-10}% of samples lie outside a 7σ limit to one side of the mean. The total error rate (BER) is then given by equation 2.

$$BER = (1.28 \times 10^{-10}\% + 1.28 \times 10^{-10}\%) \times 50\% = 1.28 \times 10^{-10}\%$$

The result of equation 2 corresponds to a BER of 1.28×10^{-12}.

The bit error rates corresponding to random jitter limits from ±1σ to ±10σ are tabulated below in Table 3.

Table 3. BER as a Function of Number of Standard Deviations

Limit	BER
±1σ	0.16
±2σ	2.28×10^{-2}
±3σ	1.35×10^{-3}
±4σ	0.32×10^{-4}
±5σ	2.87×10^{-7}
±6σ	0.98×10^{-9}
±7σ	1.28×10^{-12}
±8σ	0.62×10^{-15}
±9σ	1.13×10^{-19}
±10σ	0.77×10^{-23}

Note: The maximum jitter allowable at a particular BER value is normally provided by the system specifications or by the communications standard which the system is required to be compatible with. The maximum allowable jitter is normally specified at a level lower than 1UI.

Related Parts		
MAX9310	1:5 Clock Driver with Selectable LVPECL Inputs and LVDS Outputs	
MAX9311	1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	Free Samples
MAX9315	1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver	Free Samples
MAX9316	1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver	
MAX9317	Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs	
MAX9320	1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	Free Samples

MAX9322	LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver	
MAX9360	LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators	
MAX9374	Differential LVPECL-to-LVDS Translators	Free Samples
MAX9380	Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer	
MAX9384	ECL/PECL Dual Differential 2:1 Multiplexer	
MAX9386	Differential 5:1 or 4:1 ECL/PECL Multiplexers with Single/Dual Output Buffers	Free Samples
MAX9389	Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers	Free Samples
MAX9400	Quad Differential LVECL/LVPECL Buffer/Receivers	

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