Features

- Single-voltage Operation
  - 5V Read
  - 5V Reprogramming
- Fast Read Access Time – 55 ns
- Internal Program Control and Timer
- Sector Architecture
  - One 16K Bytes Boot Block with Programming Lockout
  - Two 8K Bytes Parameter Blocks
  - Eight Main Memory Blocks (One 32K Bytes, Seven 64K Bytes)
- Fast Erase Cycle Time – 6 Seconds
- Byte-by-Byte Programming – 20 µs/Byte Typical
- Hardware Data Protection
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Low Power Dissipation
  - 20 mA Active Current
  - 70 µA CMOS Standby Current
- Typical 10,000 Write Cycles
- Green (Pb/Halide-free) Packaging Option

4-megabit (512K x 8) 5-volt Only Flash Memory

AT49F040A

1. Description

The AT49F040A is a 5-volt only in-system reprogrammable Flash memory. Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 110 mW over the commercial temperature range.

When the device is deselected, the CMOS standby current is less than 70 µA. To allow for simple in-system reprogrammability, the AT49F040A does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ inputs to avoid bus contention. Reprogramming the AT49F040A is performed by erasing a block of data and then programming on a byte-by-byte basis. The byte programming time is a fast 20 µs. The end of a program cycle can be optionally detected by the $\overline{\text{DATA}}$ polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The device is erased by executing the erase command sequence; the device internally controls the erase operations. There are two 8K byte parameter block sections, eight main memory blocks, and one boot block.

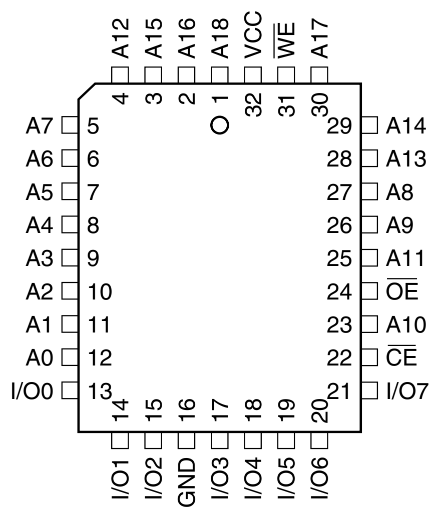
The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. The 16K-byte boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

3359C–FLASH–3/05

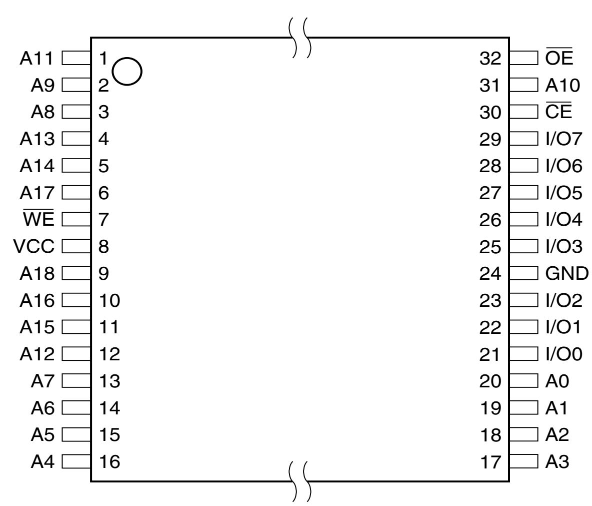
2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

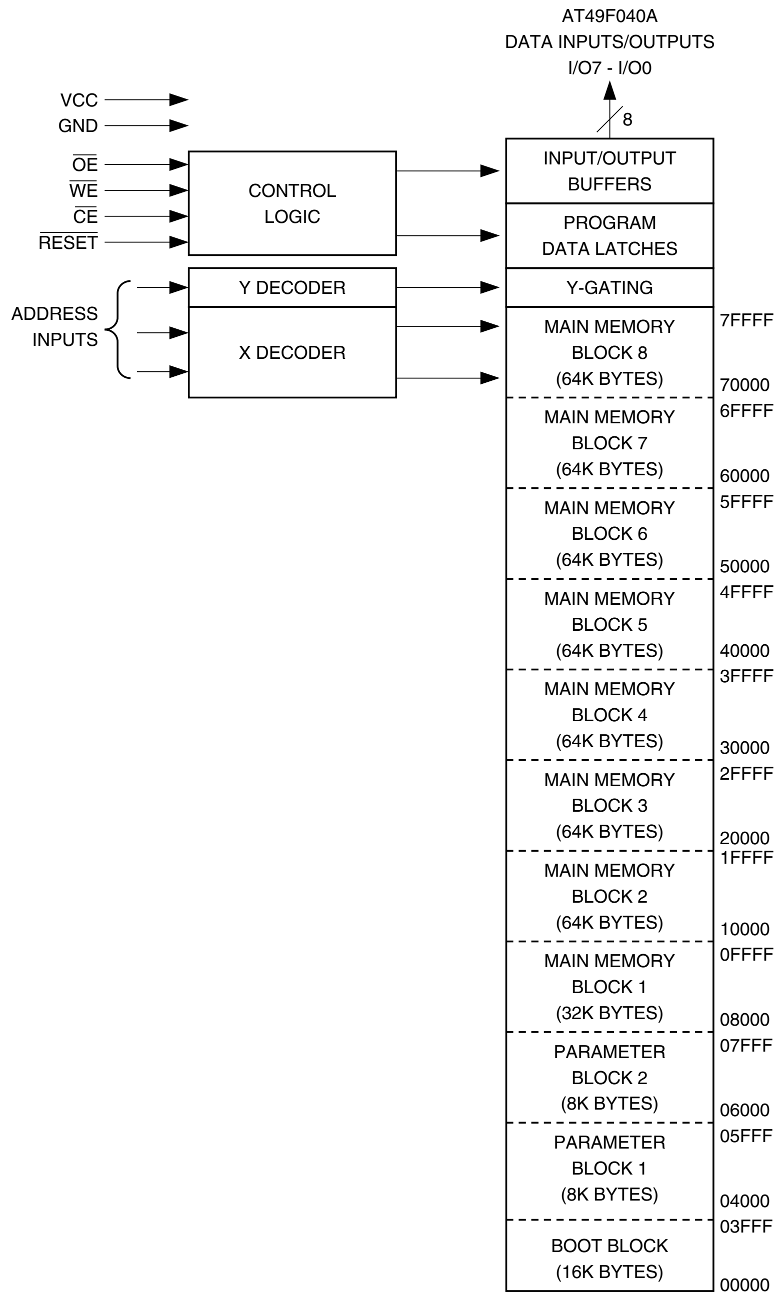
2.1 32-lead PLCC Top View



2.2 32-lead TSOP (Type 1) Top View (8 x 20 mm)



3. Block Diagram



4. Device Operation

4.1 Read

The AT49F040A is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Command Sequences

When the device is first powered on, it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition Table" on page 6. The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (except for the sixth cycle of the Sector Erase command), whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

4.3 Erasure

Before a byte can be reprogrammed, the main memory block or parameter block which contains the byte must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

4.3.1 Chip Erase

If the boot block lockout has been enabled, the Chip Erase function will erase Parameter Block 1, Parameter Block 2, Main Memory Block 1 - 8 but not the boot block. If the Boot Block Lockout has not been enabled, the Chip Erase function will erase the entire chip. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

4.3.2 Sector Erase

As an alternative to a full chip erase, the device is organized into sectors that can be individually erased. There are two 8K-byte parameter block sections and eight main memory blocks. The 8K-byte parameter block sections and the eight main memory blocks can be independently erased and reprogrammed. The Sector Erase command is a six bus cycle operation. The sector address is latched on the rising $\overline{WE}$ edge of the sixth cycle and the 30H data input command is also latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

5. Byte Programming

Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the "Command Definition Table" on page 6). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

6. Boot Block Programming Lockout

The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 16K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000 to 03FFF.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the "Command Definition Table" on page 6.

6.0.1 Boot Block Lockout Detection

A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

6.1 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see "Operating Modes" on page 7 (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

6.2 $\overline{\text{DATA}}$ Polling

The AT49F040A features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

6.3 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling the AT49F040A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

6.4 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT49F040A in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

7. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[5]	30
Byte Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Boot Block Lockout[3]	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	40
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit[4]	3	555	AA	AAA	55	555	F0						
Product ID Exit[4]	1	XXXX	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O7 - I/O0 (Hex). The address format in each bus cycle is as follows: A11 - A0 (Hex); A11 - A18 (don't care).
2. Since A11 is don't care, AAA can be replaced with 2AA.
3. The 16K byte boot sector has the address range 00000H to 03FFFH.
4. Either one of the Product ID Exit commands can be used.
5. SA = sector addresses:
   SA = 00000 to 03FFF for BOOT BLOCK
   SA = 04000 to 05FFF for PARAMETER BLOCK 1
   SA = 06000 to 07FFF for PARAMETER BLOCK 2
   SA = 08000 to FFFF for MAIN MEMORY ARRAY BLOCK 1
   SA = 10000 to 1FFFF for MAIN MEMORY ARRAY BLOCK 2
   SA = 20000 to 2FFFF for MAIN MEMORY ARRAY BLOCK 3
   SA = 30000 to 3FFFF for MAIN MEMORY ARRAY BLOCK 4
   SA = 40000 to 4FFFF for MAIN MEMORY ARRAY BLOCK 5
   SA = 50000 to 5FFFF for MAIN MEMORY ARRAY BLOCK 6
   SA = 60000 to 6FFFF for MAIN MEMORY ARRAY BLOCK 7
   SA = 70000 to 7FFFF for MAIN MEMORY ARRAY BLOCK 8

8. Absolute Maximum Ratings*

Temperature Under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground ....-0.6V to +6.25V

All Output Voltages
with Respect to Ground ....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$
with Respect to Ground ....-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9. DC and AC Operating Range

		AT49F040A-55	AT49F040A-70
Operating Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

10. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program/Erase[(2)]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[(1)]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Reset	X	X	X	X	High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H,[(3)] A0 = V_{IL}	Manufacturer Code[(4)]
				A1 - A18 = V_{IL}, A9 = V_H,[(3)] A0 = V_{IH}	Device Code[(4)]
Software[(5)]				A0 = V_{IL}, A1 - A18 =V_{IL}	Manufacturer Code[(4)]
				A0 = V_{IH}, A1 - A18 =V_{IL}	Device Code[(4)]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 13H.
5. See details under Software Product Identification Entry/Exit.

11. DC Characteristics

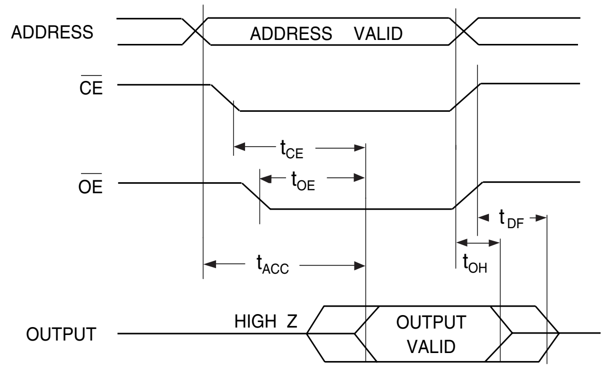
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		70	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}[(1)]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		20	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

12. AC Read Characteristics

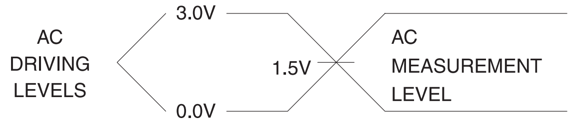
Symbol	Parameter	AT49F040A-55		AT49F040A-70		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		55		70	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		55		70	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	30	0	35	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

13. AC Read Waveforms [1][2][3][4]



Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

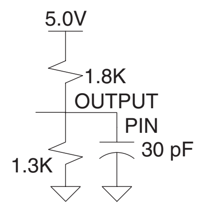
14. Input Test Waveform and Measurement Level



t_R, t_F < 5 ns

15. Output Load Test

55 ns



16. Pin Capacitance

f = 1 MHz, T = 25°C[(1)]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

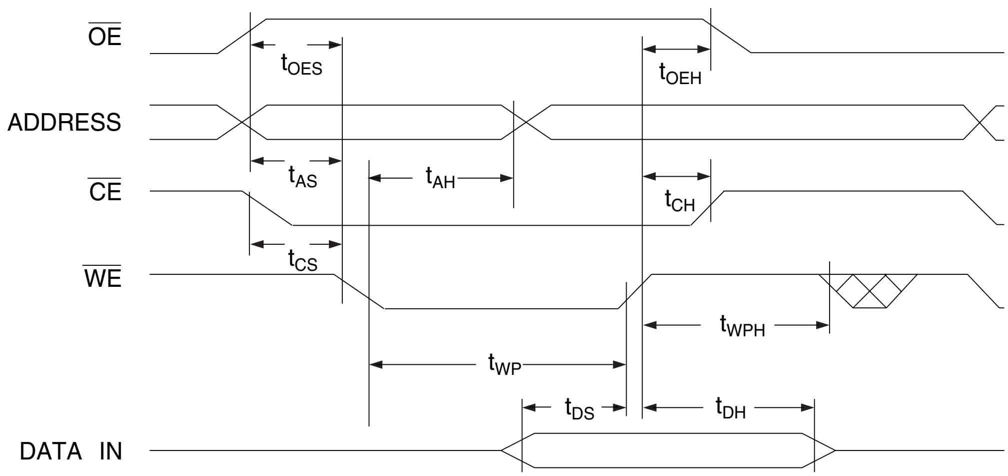
Note: 1. This parameter is characterized and is not 100% tested.

17. AC Byte Load Characteristics

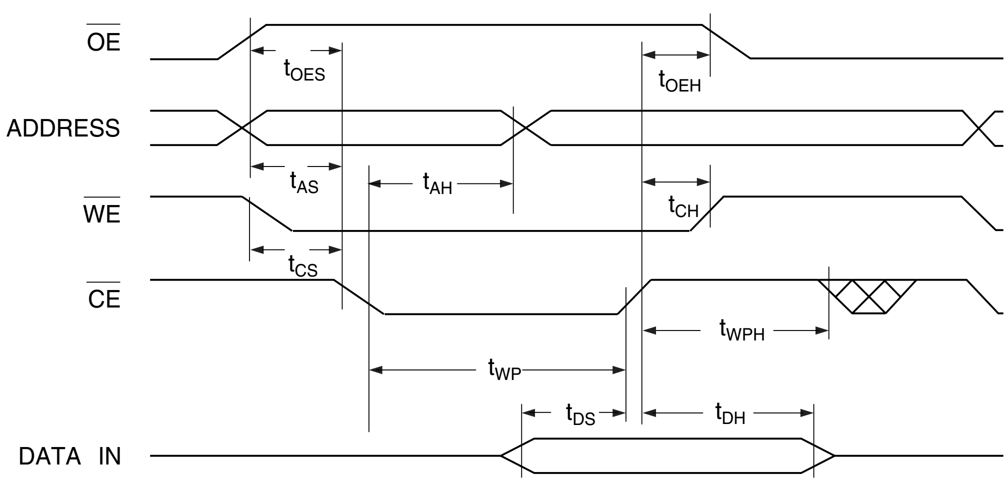
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	25		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	20		ns
t_{DS}	Data Set-up Time	20		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	20		ns

18. AC Byte Load Waveforms

18.1 $\overline{WE}$ Controlled



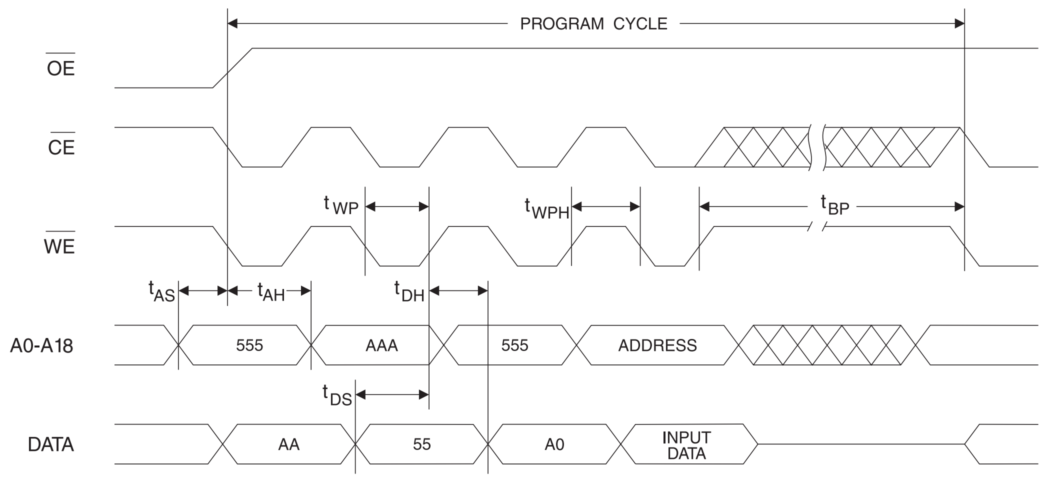
18.2 $\overline{CE}$ Controlled



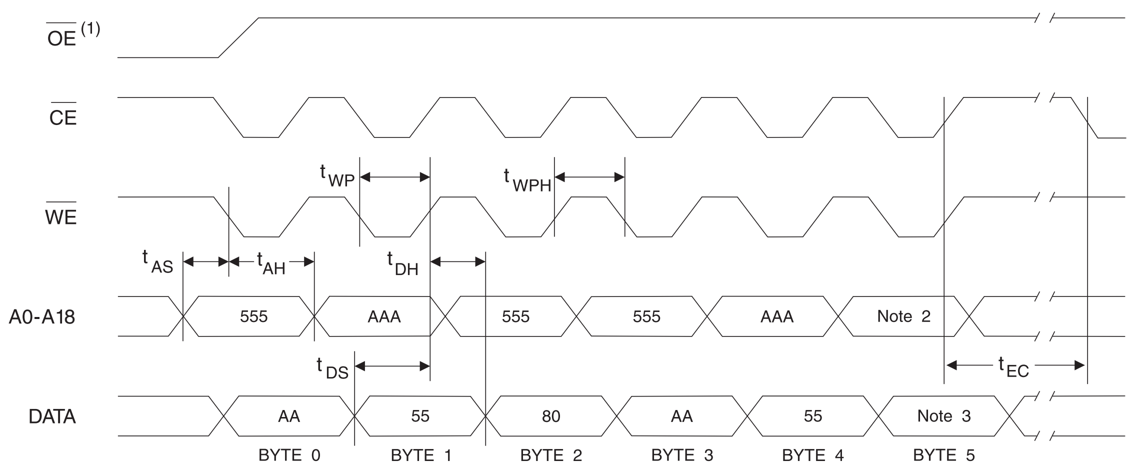
19. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		20	40	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	25			ns
t_{DS}	Data Set-up Time	20			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	20			ns
t_{WPH}	Write Pulse Width High	20			ns
t_{EC}	Chip Erase Cycle Time			12	seconds

20. Program Cycle Waveforms



21. Sector or Chip Erase Cycle Waveforms



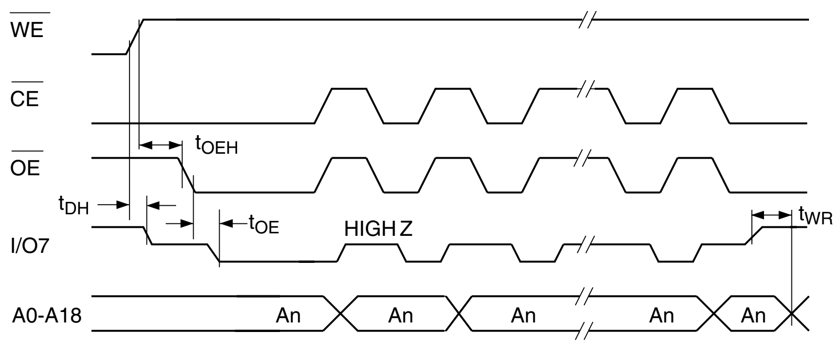
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 4 under "Command Definition Table" on page 6.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

22. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" .

23. $\overline{\text{Data}}$ Polling Waveforms

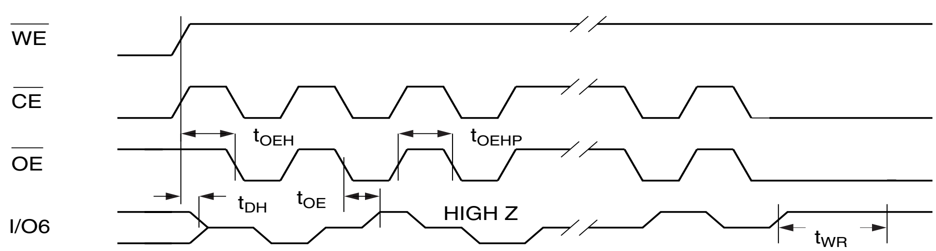


24. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

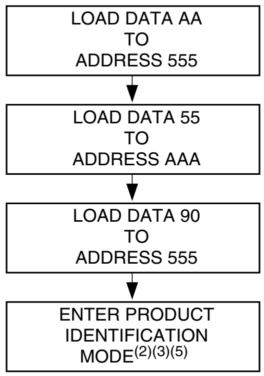
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" .

25. Toggle Bit Waveforms[1][2][3]

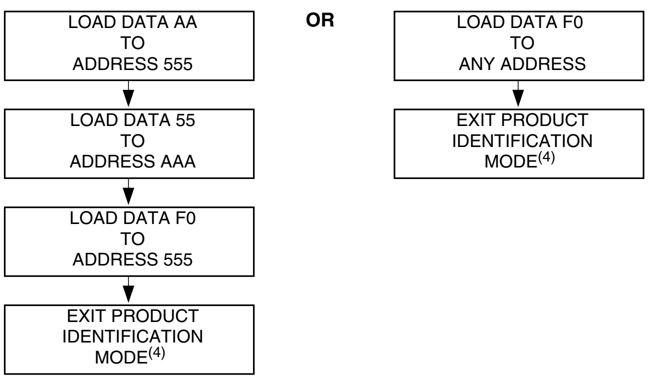


Notes: 1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

26. Software Product Identification Entry[1]

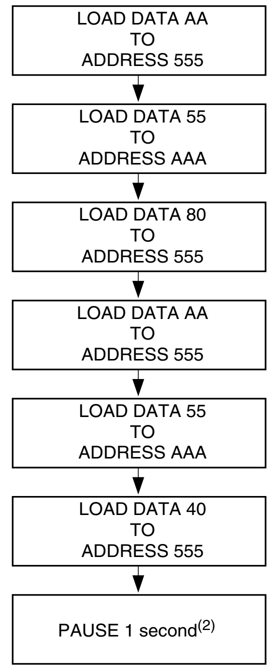


27. Software Product Identification Exit[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A11 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
   Additional Device Code is read for address 0003H
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 13H
   Additional Device Code: 0FH

28. Boot Block Lockout Feature Enable Algorithm[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A11 - A0 (Hex).
2. Boot block lockout feature enabled.

29. Ordering Information

29.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	25	0.1	AT49F040A-55JI AT49F040A-55TI	32J 32T	Industrial (-40° to 85°C)
70	25	0.1	AT49F040A-70JI AT49F040A-70TI	32J 32T	Industrial (-40° to 85°C)

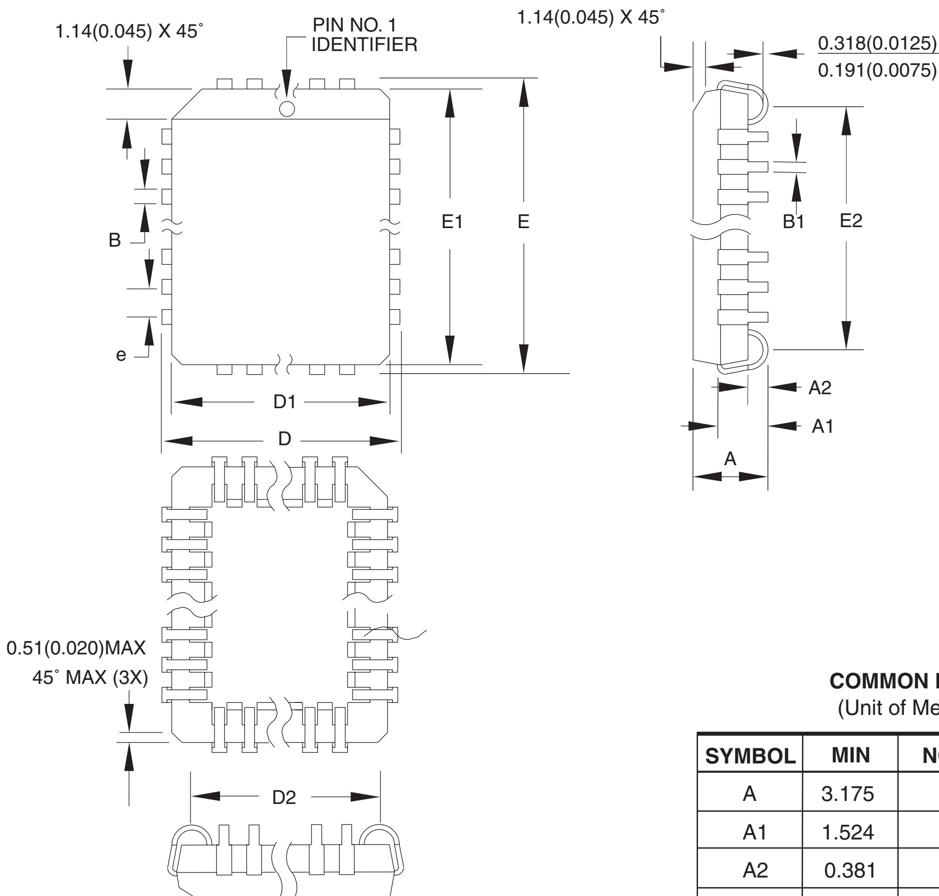
29.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	25	0.1	AT49F040A-55JU AT49F040A-55TU	32J 32T	Industrial (-40° to 85°C)
70	25	0.1	AT49F040A-70JU AT49F040A-70TU	32J 32T	Industrial (-40° to 85°C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier Package (PLCC)
32T	32-lead, Plastic Thin Small Outline Package (TSOP) (8 x 20 mm)

30. Packaging Information

30.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

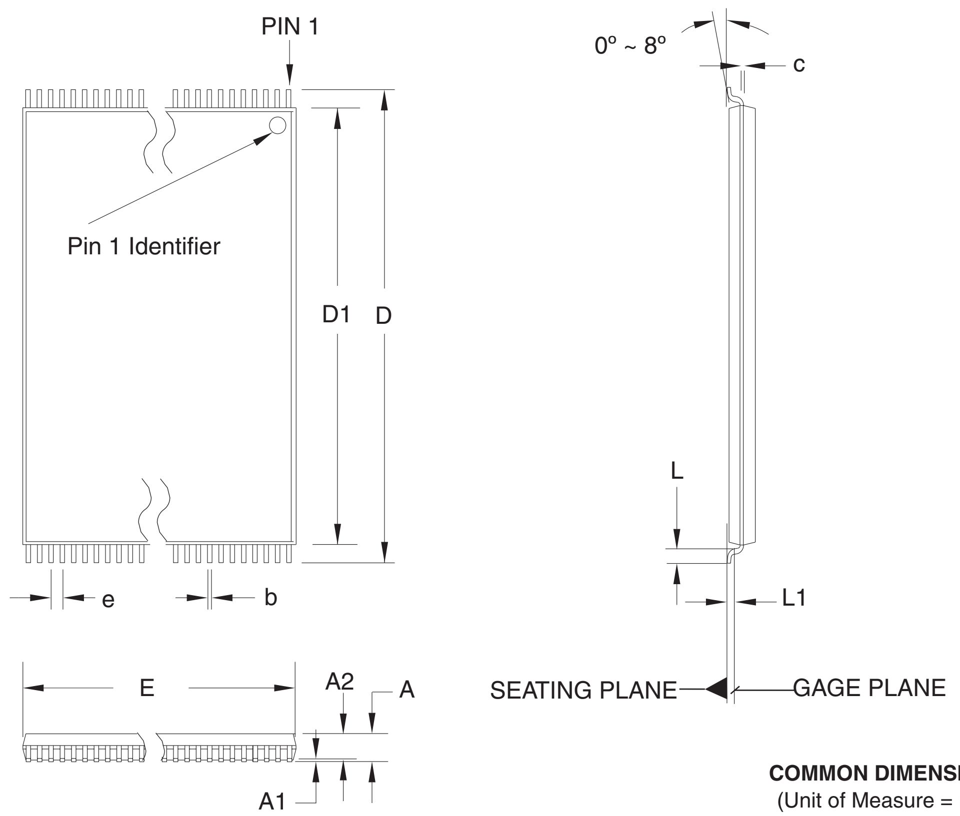
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

30.2 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

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