Si5380 Reference Manual

Overview

This Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5380 devices in end applications. The official device specifications can be found in the Si5380 datasheet.

The Si5380 is a high performance, integer-based (M/N) clock generator for applications which demand the highest level of phase noise and jitter performance. Based on Silicon Laboratories' 4th generation DSPLL technology, the Si5380 combines frequency synthesis and jitter attenuation in a highly integrated digital solution that eliminates the need for external VCXO and loop filter components. A low cost, fixed-frequency crystal provides frequency stability for free-run and holdover modes. This all-digital solution provides superior performance that is highly immune to external board disturbances such as power supply noise and other noise sources that normally couple through external analog components. The Si5380 guarantees high performance independent of board layout. The device configuration is in-circuit programmable via an SPI or I^2C serial interface and is easily stored in non-volatile memory (NVM) for applications which require pre-configured clocks at start-up or after reset. The Si5380 provides output-to-output and input-to-output delay adjustment features for applications which require precise clock edge alignment.

RELATED DOCUMENTS

- Si5380 Data Sheet
- Si5380 Device Errata
- Si5380-EVB User Guide
- Si5380-EVB Schematics, BOM & Layout
- IBIS models
- To download evaluation board design and support files, go to: http://www.silabs.com/Si538x-4x-EVB

Work Flow Expectations with ClockBuilder ™ Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder™ Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

1. Functional Description

1.1 DSPLL

The DSPLL provides the synthesis for generating the output clock frequencies which are synchronous to the selected input clock frequency or freerun from the XTAL. It consists of a phase detector, a programmable digital loop filter, a high-performance ultra-low-phase-noise analog 14.7456 GHz VCO, and a user configurable feedback divider. An internal oscillator (OSC) provides the DSPLL with a stable low-noise clock source for frequency synthesis and for maintaining frequency accuracy in the Freerun or Holdover modes. The oscillator simply requires an external, low cost 54 MHz fundamental mode crystal to operate. No other external components are required for oscillation. A key feature of DSPLL is providing immunity to external noise coupling from power supplies and other uncontrolled noise sources that normally exist on printed circuit boards.

The frequency configuration of the DSPLL is programmable through the SPI or I^2C serial interface and can also be stored in non-volatile memory (NVM) or RAM. The combination of integer input dividers (P0-P3), Integer frequency multiplication (M), Integer output division (N), and integer output division (R0A-R9A) allows the generation of a wide range of frequencies on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro software.

1.2 Si5380 LTE Frequency Configuration

The device's frequency configuration is fully programmable through the serial interface and can also be stored in non-volatile memory. The flexible combination of integer dividers and a high frequency VCO allows the device to generate multiple output clock frequencies for applications that require ultra-low phase-noise and spurious performance. At the core of the device are the N dividers which determine the number of unique frequencies that can be generated from the device. The table below shows a list of possible output frequencies for LTE applications. The Si5380's DSPLL core can generate up to five unique frequencies. These frequencies are distributed to the output dividers using a configurable crosspoint mux. The R dividers allow further division for up to 10 unique integer related frequencies on the Si5380. The ClockBuilder Pro software utility provides a simple means of automatically calculating the optimum divider values (P, M, N and R) for the frequencies listed below.

Table 1.1. Example List of Possible LTE Clock Frequencies

Fin (MHz)[1]	LTE Device Clock Fout (MHz)[2]
15.36	15.36
19.20	19.20
30.72	30.72
38.40	38.40
61.44	61.44
76.80	76.80
122.88	122.88
153.60	153.60
184.32	184.32
245.76	245.76
307.20	307.20
368.64	368.64
491.52	491.52
614.40	614.40
737.28	737.28
-	983.04
-	1228.80
-	1474.56

Fin (MHz)[1]	LTE Device Clock Fout (MHz)[2]
Notes: 1. The Si5380 locks to any one of the frequencies listed in the Fin column and generates LTE device clock frequencies. 2. R output dividers allow other frequencies to be generated. These are useful for applications like JESD204B SYSREF clocks.	

1.3 Si5380 Configuration for JESD204B subclass 1 Clock Generation

The Si5380 can be used as a high performance, fully integrated JEDEC JESD204B jitter cleaner while eliminating the need for discrete VCXO and loop filter components. The Si5380 supports JESD204B subclass 0 and subclass 1 clocking by providing both device clocks (DCLK) and system reference clocks (SYSREF). The 12 clock outputs can be independently configured as device clocks or SYSREF clocks to drive JESD204B ADCs, DACs, FPGAs, or other logic devices. The Si5380 will clock up to six JESD204B subclass 1 targets, using six DCLK/SYSREF pairs. If SYSREF clocking is implemented in external logic, then the Si5380 can clock up to 12 JESD204B targets. Not limited to JESD204B applications, each of the 12 outputs is individually configurable as a high performance output for traditional clocking applications.

For applications which require adjustable static delay between the DCLK and SYSREF signals, the Si5380 supports up to four DCLK/SYSREF pairs, each with independently adjustable delay. An example of an adjustable delay JESD204B frequency configuration is shown in the following figure. In this case, the N0 divider determines the device clock frequencies while the N1-N4 dividers generate the divided SYSREF used as the lower frequency frame clock. Each output N divider also includes a configurable delay (Δt) for controlling deterministic latency. This example shows a configuration where all the device clocks are controlled by a single delay (Δt0) while the SYSREF clocks each have their own independent delay (Δt1 – Δt4), though other combinations are also possible. The bidirectional delay is programmable over ±8.6 ns in 68 ps steps. See 4.7 Output Delay Control (Δt0 – Δt4) for more information on delay control. The SYSREF clock is always periodic and can be controlled (on/off) without glitches by enabling or disabling its output through register writes.

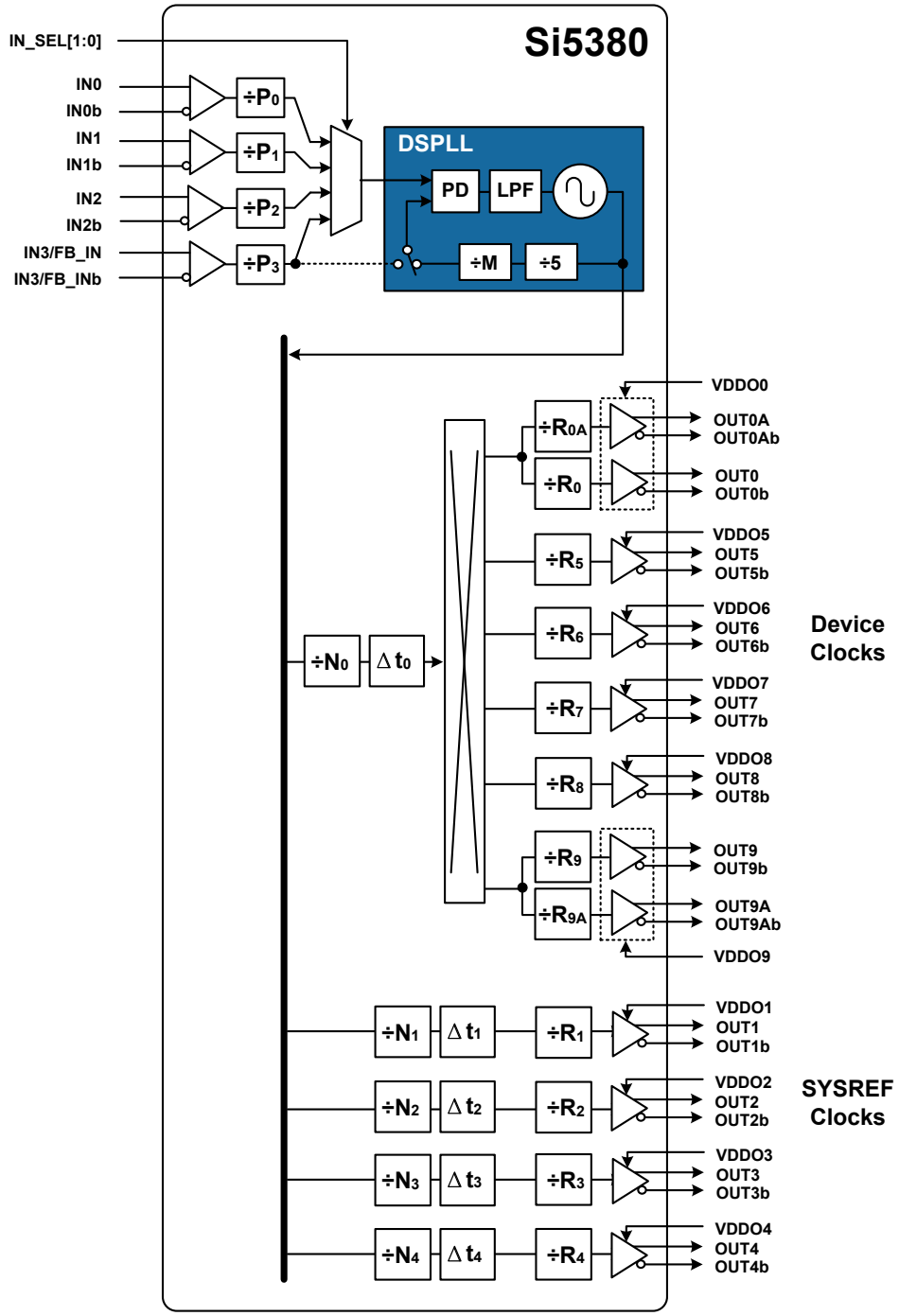

Figure 1.1. Example N Divider Configuration for Generating JESD204B Subclass 1 Clocks

1.4 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and wander filtering. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 100 Hz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. The DSPLL loop bandwidth register values are determined using ClockBuilder Pro. Note that after manually changing bandwidth parameters, the BW_UPDATE bit must be set high to latch the new values into operation. Note that this update bit will latch both loop and Fastlock bandwidths

Table 1.2. DSPLL Loop Bandwidth Registers

Register Name	Hex Address [Bit Field]	Function
BW_PLL	0x0508[7:0]-0x050D[7:0]	Determines the loop BW for the DSPLL. Parameters are generated by ClockBuilder Pro.
BW_UPDATE	0x0514[0]	Writing a 1 to this register bit will latch both the Loop and Fastlock BW parameter registers.

1.4.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher Fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Bandwidth settings in the range from 100 Hz up to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The Fastlock feature can be enabled or disabled independently by register control. If enabled, when LOL is asserted Fastlock will be automatically enabled. When LOL is no longer asserted, Fastlock will be automatically disabled. Note that after changing the bandwidth parameters, the BW_UPDATE bit must be set to 1 to latch the new values into operation. Note that each of these update bits will latch both loop and Fastlock bandwidths.

Table 1.3. DSPLL Fastlock Bandwidth Registers

Register Name	Hex Address [Bit Field]	Function
FAST_BW_PLL	0x050E[7:0]-0x0513[7:0]	Determines the Fastlock BW for the DSPLL. Parameters are generated by ClockBuilder Pro.
FASTLOCK_AUTO_EN	0x052B[0]	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
FASTLOCK_MAN	0x052B[1]	Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

The loss of lock (LOL) feature is a fault monitoring mechanism. Details of the LOL feature can be found in 3.3.4 DSPLL LOL (Loss-of-Lock) Detection and the LOLb Output Indicator Pin.

1.5 Dividers Overview

There are four divider classes within the Si5380. See for a block diagram showing all of these dividers. All divider values for the Si5380 are Integer-only.

- P0-P3: Input clock wide range dividers (0x0208-0x022F)
  - 48-bit numerator, 32-bit denominator
  - Min. value is 1, Max. value is 2 ^{24}
  - Practical range limited by phase detector and VCO range
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
- M: DSPLL feedback divider (0x0515-0x051F)
  - 56-bit numerator, 32-bit denominator
  - Min. value is 1, Max. value is 2^{24}
  - Practical range limited by phase detector and VCO range
  - The M divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Soft Reset will also update M divider values.
- N: Output divider (0x0523-0x0529)
  - 44-bit numerator, 32-bit denominator
  - Min. value is 1, Max. value is 2^{24}
  - Each N divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Soft Reset will also update N divider values.
- R: Final output divider (0x0247-0x026A)
  - 24-bit field
  - Min. value is 2, Max. value is 2^{25}-2
  - Only even integer divide values: 2,4,6, etc.
  - R Divisor=2 x (Field +1). For example, Field=3 gives an R divisor of 8.

2. Modes of Operation

After initialization, the DSPLL will operate in one of the following modes: Free-run, lock-acquisition, locked, or Holdover. These modes are described further in the sections below.

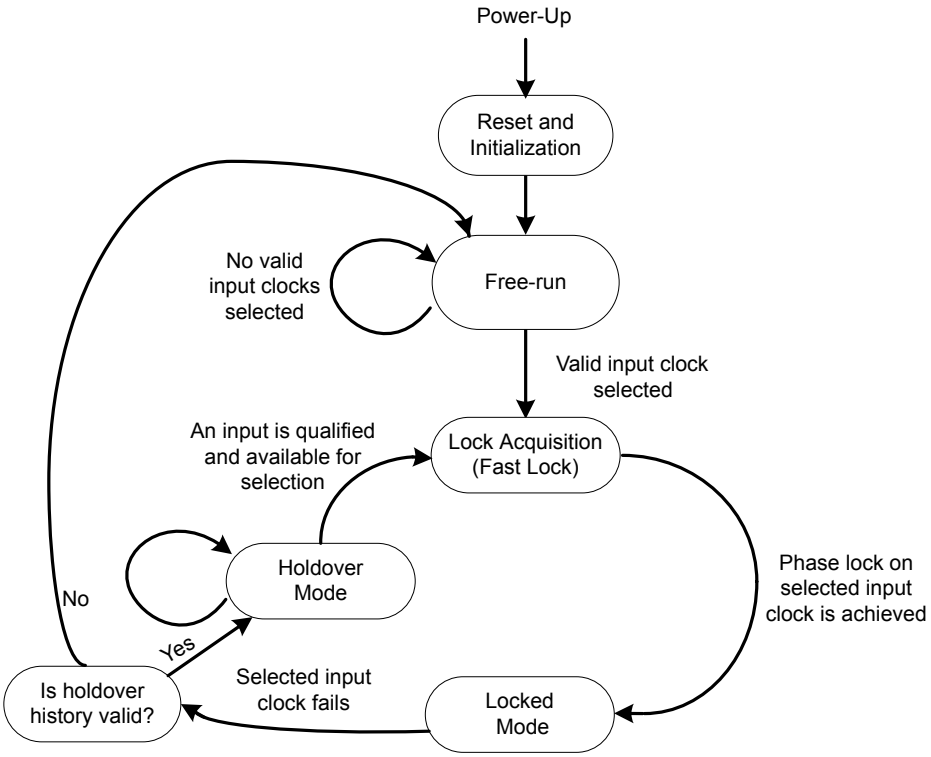

Figure 2.1. Modes of Operation

2.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the SPI or I^2C serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

There are two types of resets available. A Hard Reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface, will be restored to their initial state. A Hard Reset is initiated using the RSTb pin or by asserting the Hard Reset bit. A Soft Reset bypasses the NVM download and is used to initiate register configuration changes. The table below lists the reset and control registers.

Table 2.1. Reset Registers

Register Name	Hex Address [Bit Field]	Function
HARD_RST	0x001E[1]	Writing a 1 to this register bit performs the same function as power cycling the device. All registers will be restored to their NVM values.
SOFT_RST	0x001C[0]	Writing a 1 to this register bit performs a Soft Reset of the device. Initiates register configuration changes without reloading NVM.

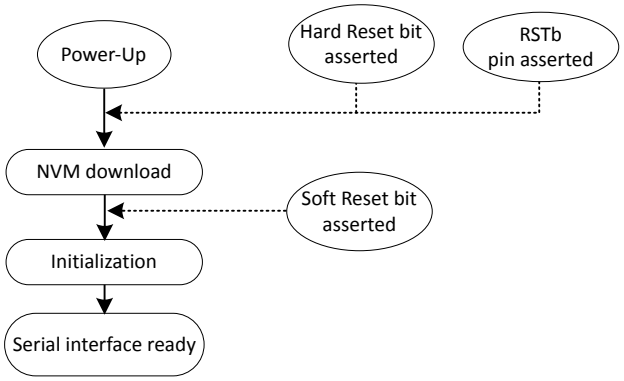

Figure 2.2. Initialization from Hard Reset and Soft Reset

The Si5380 is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins.

2.1.1 Making Register Changes During Device Operation

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). The following are the affected registers:

Control	Register(s)
P0_NUM / P0_DEN	0x0208 – 0x0211
P1_NUM / P1_DEN	0x0212 – 0x021B
P2_NUM / P2_DEN	0x021C – 0x0225
P3_NUM / P3_DEN	0x0226 – 0x022F

PLL lockup can easily be avoided by using the following the preamble and postamble write sequence when one of these registers is modified during device operation. ClockBuilder Pro software adds these writes to the output file by default when Exporting Register Files.

1. To start, write the preamble by updating the following control bits using Read/Modify/Write sequences:

Register	Value
0x0B24	0xD8
0x0B25	0x00

2. Wait 300 ms for the device state to stabilize.
3. Then modify all desired control registers.
4. Write 0x01 to Register 0x001C (SOFT_RST) to perform a Soft Reset once modifications are complete.
5. Write the postamble by updating the following control bits using Read/Modify/Write sequences:

Register	Value
0x0B24	0xDB
0x0B25	0x02

2.2 NVM Programming

The NVM is two-time writable for a base part (no set frequency plan) and one-time writable for a part with a factory pre-programmed frequency plan. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Note: In-circuit programming is supported over the temperature range of 0 to 80 °C.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed. Verify device operation before writing registers to NVM.
2. You may write to the user scratch space (registers 0x026B to 0x0272) to identify the contents of the NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Wait until DEVICE_READY=0x0F.
5. Set NVM_READ_BANK 0x00E4[0]=1.
6. Wait until DEVICE_READY=0x0F.

Alternatively, steps 5 and 6 can be replaced with a Hard Reset, either by RSTb pin, HARD_RST register bit, or power cycling th device to generate a POR. This process will load the new NVM contents back into the device registers.

Table 2.2. NVM Programming Registers

Register Name	Hex Address [Bit Field]	Function
ACTIVE_NVM_BANK	0x00E2[5:0]	Identifies the active NVM bank.
NVM_WRITE	0x00E3[7:0]	Initiates an NVM write when written with value 0xC7.
NVM_READ_BANK	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	Indicates that the device is ready to accept commands when value = 0x0F.

2.3 Free Run Mode

Once power is applied to and initialization is complete the DSPLL will automatically enter Freerun mode, generating the output frequencies determined by the NVM. The frequency accuracy of the generated output clocks in Freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XAXB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in Freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in Freerun or Holdover modes. Because there is little or no jitter attenuation from the XAXB pins to the clock outputs, a low-jitter XAXB source will be needed for low-jitter clock outputs.

2.4 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the Fastlock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

2.5 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock. At this point any XTAL frequency drift will typically not affect the output frequency. A loss of lock pin (LOLb) and status bit indicate when lock is achieved. See 3.3.4 DSPLL LOL (Loss-of-Lock) Detection and the LOLb Output Indicator Pin for more details on the operation of the loss of lock circuit.

2.6 Holdover Mode

The DSPLL will automatically enter Holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. It uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

When entering Holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XAXB pins. If the clock input becomes valid, the DSPLL will automatically exit the Holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is Glitchless and its rate is controlled by the DSPLL bandwidth or the Fastlock bandwidth, if Fastlock is enabled. These options are register programmable.

As shown in Figure 2.1 Modes of Operation on page 7 the Holdover and Freerun modes are closely related. The device will only enter Holdover if a valid clock has been selected long enough for the holdover history to become valid, i.e. HOLD_HIST_VALID = 1. If the clock fails before the combined HOLD_HIST_LEN + HOLD_HIST_DELAY time has been met, HOLD_HIST_VALID = 0 and the device will enter Freerun mode instead. Reducing the HOLD_HIST_LEN and HOLD_HIST_DELAY times will allow Holdover in less time, limited by the source clock failure and wander characteristics. Note that the Holdover timer is reset when the input clock is lost and is restarted from the beginning when either the failed input clock signal returns or another input clock is selected.

Table 2.3. Holdover Mode Control Registers

Register Name	Hex Address [Bit Field]	Function
Holdover Status		
HOLD	0x000E[5]	DSPLL Holdover status indicator. 0: Normal Operation 1: In Holdover/Freerun Mode: HOLD_HIST_VALID = 0 =>Freerun Mode HOLD_HIST_VALID = 1 =>Holdover Mode
HOLD_FLG	0x0013[5]	Holdover indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
HOLD_INTR_MSK	0x0019[5]	Masks Holdover/Freerun from generating INTRb interrupt. 0: Allow Holdover/Freerun interrupt (default) 1: Mask (ignore) Holdover/Freerun for interrupt
HOLD_HIST_VALID	0x053F[1]	Holdover historical frequency data valid. 0: Invalid/incomplete Holdover history, Freerun mode available 1: Valid Holdover history, Holdover mode available
Holdover Control and Settings		
HOLD_RAMP_BYP	0x052C[3]	Must be set to 1 for Normal Operation.

Register Name	Hex Address [Bit Field]	Function
Holdover Status		
HOLD_EXIT_BW_SEL	0x052C[4]	Selects the exit rate from Holdover bandwidth. 0: Exit of Holdover using the Fastlock bandwidth (default) 1: Exit of Holdover using the DSPLL loop bandwidth
HOLD_HIST_LEN	0x052E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $(2^{HOLD\_HIST\_LEN} - 1) \times 8 / 3 \times 10^{-7}$
HOLD_HIST_DELAY	0x052F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY} \times 2 / 3 \times 10^{-7}$
FORCE_HOLD	0x0535[0]	Force the device into Holdover mode. Used to hold the device output clocks while re-training an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID = 0 =>Freerun Mode HOLD_HIST_VALID = 1 =>Holdover Mode

3. Clock Inputs (IN0, IN1, IN2, IN3)

3.1 Input Source Selection

The inputs accept both standard format inputs and low-duty-cycle Pulsed CMOS clocks. Input selection from CLK_SWITCH_MODE can be manual (pin or register controlled) or automatic with user definable priorities. Register 0x052A is used to select manual pin or register control, and to configure the input as shown in the table below.

Table 3.1. Input Selection Control Registers

Register Name	Hex Address [Bit Field]	Function
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 00: Manual (default), 01: Automatic Non-revertive, 02: Automatic Revertive, 03: Reserved
IN_SEL_REGCTRL	0x052A[0]	Manual Input Select control source. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection
IN_SEL	0x052A[2:1]	Manual Input Select selection register. 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3

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3.1.1 Manual Input Selection

In manual mode, CLK_SWITCH_MODE=0x00.

Input switching can be done manually using the IN_SEL[1:0] device pins from the package or through register 0x052A IN_SEL[2:1]. Bit 0 of register 0x052A determines if the input selection is pin selectable or register selectable. The default is pin selectable. The following table describes the input selection on the pins. Note that when Zero Delay Mode is enabled, the FB_IN pins will become the feedback input and IN3 therefore is not available as a clock input. If there is not a valid clock signal on the selected input, the device will automatically enter Freerun or Holdover mode. See 5. Zero Delay Mode for further information.

Table 3.2. Manual Input Selection using IN_SEL[1:0] Pins

IN_SEL[1:0] PINS	DSPLL Input Source
00	IN0
01	IN1
10	IN2
11	IN3[1]

Note:
1. IN3 not available as a DSPLL source in ZDM.

3.1.2 Automatic Input Switching

In automatic mode CLK_SWITCH_MODE = 0x01 (Non-revertive) or 0x02 (Revertive).

Automatic input switching is available in addition to the manual selection described previously in 3.1.1 Manual Input Selection . In automatic mode, the switching criteria is based on input clock qualification, input priority and the revertive option. The IN_SEL[1:0] pins and IN_SEL[2:1] register bits are not used in automatic input switching. Also, only input clocks that are valid (i.e., with no active fault indicators) can be selected by the automatic clock switching. If there are no valid input clocks available, the DSPLL will enter Holdover or Freerun mode. With Revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With Non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid, an automatic switchover to the highest priority valid input will be initiated. Note that automatic input switching is not available in Zero Delay Mode. See section 5. Zero Delay Mode for further information.

Table 3.3. Automatic Input Switching Registers

Register Name	Hex Address [Bit Field]	Function
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. Selections are the following: 00: Manual (default), 01: Automatic Non-revertive, 02: Automatic Revertive, 03: Reserved
IN_LOS_MSK	0x0537[3:0]	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from the automatic clock switching logic
IN_OOF_MSK	0x0537[7:4]	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from the automatic clock switching logic
IN0_PRIORITY	0x0538[2:0]	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4, or 0 for never selected 5-7: Reserved
IN1_PRIORITY	0x0538[6:4]	
IN2_PRIORITY	0x0539[2:0]	
IN3_PRIORITY	0x0539[6:4]	

3.2 Types of Inputs

Each of the four different inputs IN0-IN3/FB_IN can be configured as standard LVDS, LVPECL, HCL, CML, and single-ended LVCMOS formats, or as a low duty cycle pulsed CMOS format. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals, having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in the figure below. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance over Pulsed CMOS.

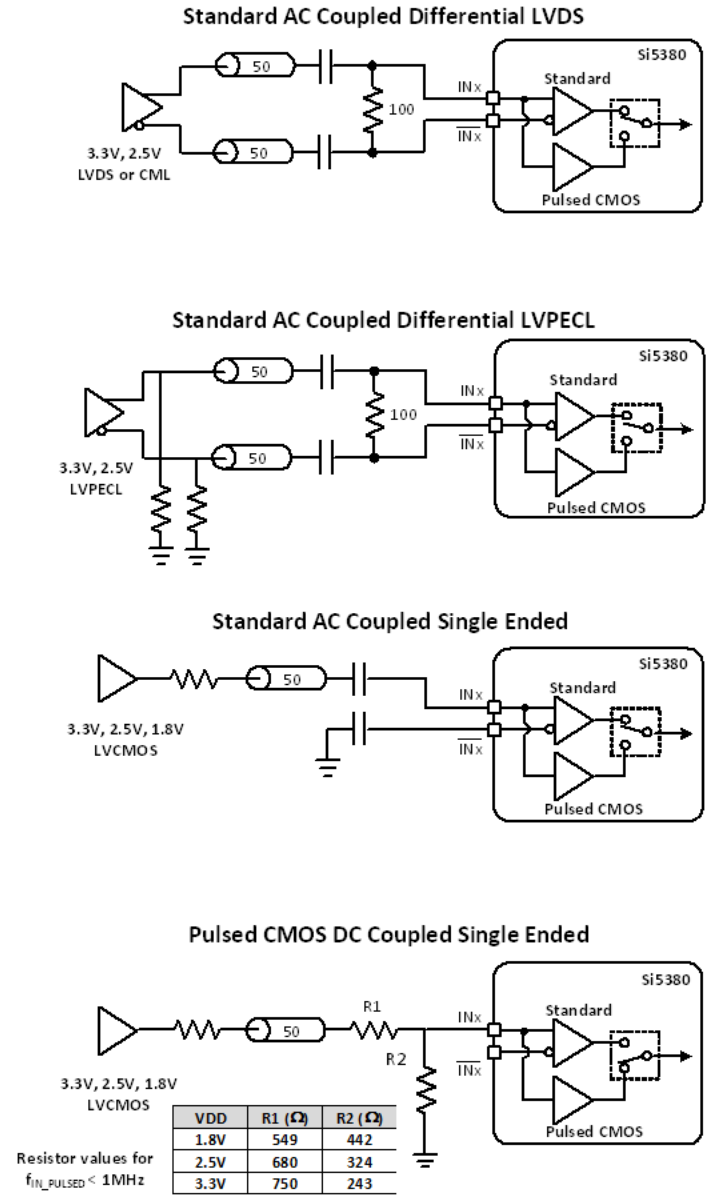


Figure 3.1. Input Termination for Standard and Pulsed CMOS Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for IN3 through IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected as shown in the figure above, including the “Standard AC Coupled Single Ended” case. In Pulsed CMOS mode, it is not necessary to connect the inverting INb input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4] for IN3 through IN0.

Table 3.4. Input Clock Configuration Registers

Register Name	Hex Address [Bit Field]	Function
IN_EN	0x0949[3:0]	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer
IN_PULSED_CMOS_EN	0x0949[7:4]	Select Pulsed CMOS input buffer for IN3 - IN0. See for more information. 0: Standard Input Format 1: Pulsed CMOS Input Format

3.2.1 Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A Hitless switch can only occur when the two input frequencies are frequency locked, which means that they have to have 0 ppm frequency error. In practice, this means that either one of the clocks must be frequency-locked to the other or that both must be frequency-locked to the same source. When Hitless switching is enabled (register 0x0536[2] = 1), the DSPLL absorbs the phase difference between the current input clock and the new input clock. When disabled (register 0x0536[2] = 0), the phase difference between the two inputs will propagate to the output at a rate determined by the DSPLL Loop Bandwidth. The Hitless switching feature supports clock frequencies down to the minimum input frequency of 10 MHz. Note that Hitless switching is not available in Zero Delay Mode.

Table 3.5. Input Hitless Switching Register

Register Name	Hex Address [Bit Field]	Function
HSW_EN	0x0536[2]	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching

3.2.2 Glitchless Input Switching

The DSPLL glitchlessly switches between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency at a rate determined by either DSPLL loop bandwidth or, if enabled, the Fastlock bandwidth. Depending on the LOL configuration settings, the loss of lock (LOL) indicator may assert while the DSPLL is pulling-in to the new clock frequency. However, there will never be abnormally shortened “runt” pulses generated at the output during this transition.

3.2.3 Unused Inputs

Unused inputs can be disabled and left unconnected when not in use. Register 0x0949[3:0] defaults the input clocks to being enabled. Clearing the unused input bits will disable them.

3.3 Fault Monitoring

The four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF). Note that the reference at the XAXB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss of Lock (LOL) indicator asserted when the DSPLL loses synchronization within the feedback loop. The figure below shows the fault monitors for each input path going into the DSPLL, which includes the crystal input as well as IN0-3.

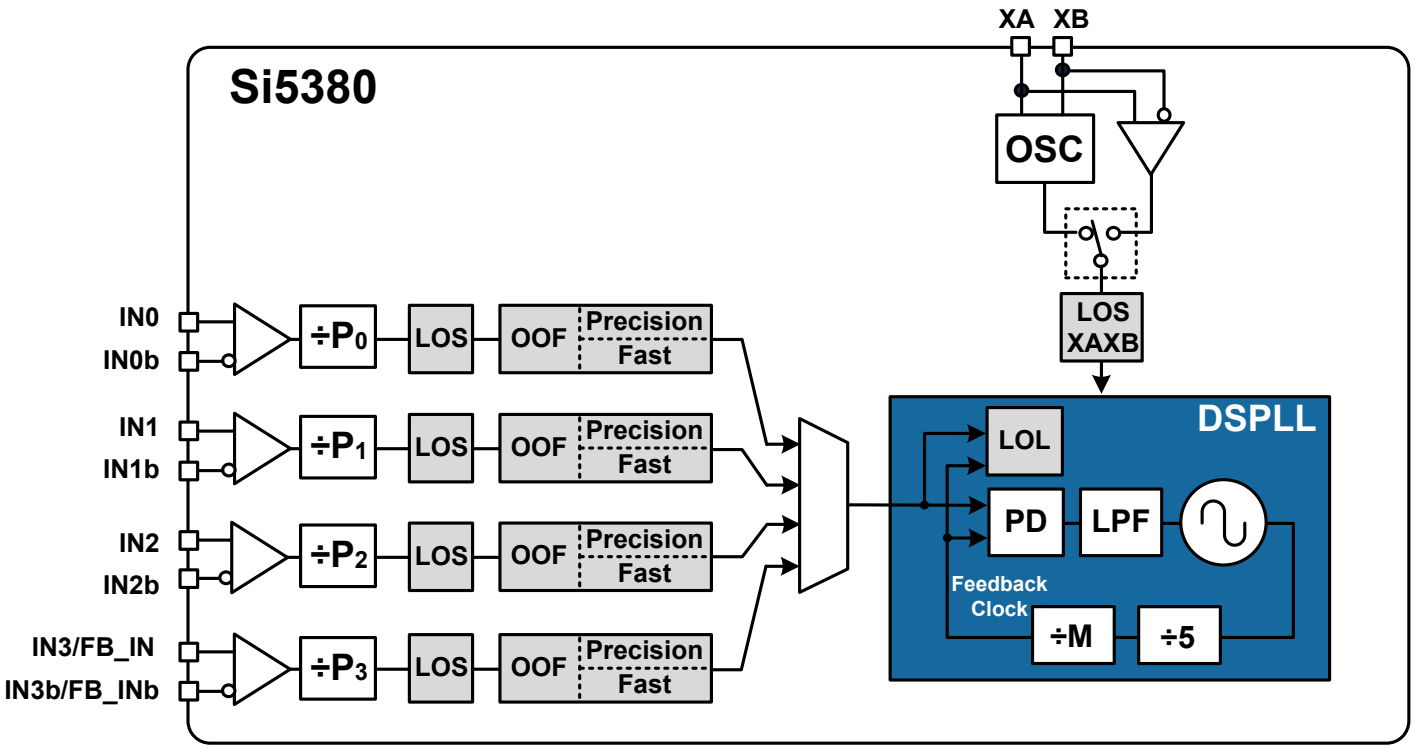


Figure 3.2. Si5380 Fault Monitors

3.3.1 Input LOS (Loss-of-Signal) Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity that allows missing edges or intermittent errors to be ignored. LOS sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading its status register bit. The live LOS register always displays the current LOS state. Also, there is a sticky flag register which stays asserted until cleared by the user.

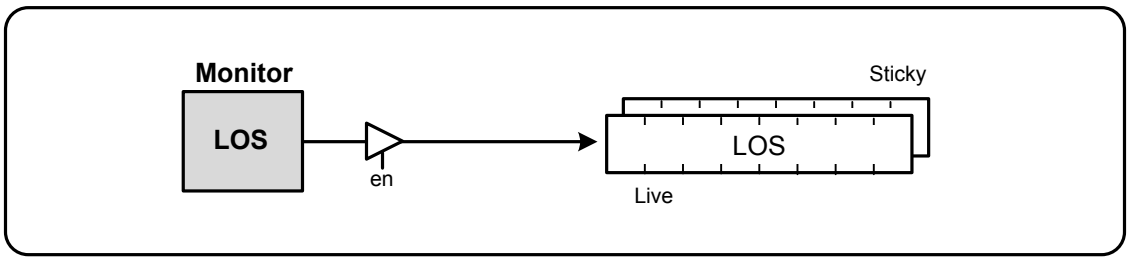


Figure 3.3. LOS Status Indicator

3.3.2 Reference Input LOSXAXB (Loss-of-Signal) Detection

A LOS monitor is also available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when LOSXAXB is detected. This feature can be disabled such that the device will continue to produce output clocks even when LOSXAXB is detected. Single-ended inputs must be connected to the XA input pin with the XB pin terminated properly for LOSXAXB to function correctly. The table below lists the loss of signal status indicators and fault monitoring control registers.

Table 3.6. LOS Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
LOS Status and Controls		
LOS	0x000D[3:0]	LOS status indicators for IN3 - IN0. 0: Input signal detected or input buffer disabled or LOS disabled 1: Insufficient Input signal detected (LOS)
LOS_FLG	0x0012[3:0]	LOS indicator sticky flag bits for IN3 - IN0. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOS_INTR_MSK	0x0018[3:0]	Masks LOS from generating INTRb interrupt for IN3 - IN0. 0: Allow LOS interrupt (default) 1: Mask (ignore) LOS for interrupt
LOS_EN	0x002C[3:0]	LOS enable bits for IN3 - IN0. Allows disabling LOS monitors on unused inputs. 0: Disable input LOS 1: Enable input LOS
LOS_VAL_TIME	0x002D[7:0]	LOS clear validation time for IN3 - IN0. This sets the time that an input must have a valid clock before the LOS condition is cleared. 0: 2 ms, 1: 100 ms, 2: 200 ms, and 3: 1 s
LOS_TRIG_THR	0x002E[7:0]-0x0035[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN3 - IN0. These values are determined by ClockBuilder Pro.
LOS_CLR_THR	0x0036[7:0]-0x003D[7:0]	
LOSXAXB Status and Controls		
LOSXAXB	0x000C[1]	LOS indicator for XAXB input signal 0: XAXB input signal detected 1: Insufficient XAXB input signal detected
LOSXAXB_FLG	0x0011[1]	LOSXAXB status indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

Register Name	Hex Address [Bit Field]	Function
LOS Status and Controls		
LOSXAXB_INTR_MSK	0x0017[1]	Masks LOSXAXB from generating INTRb interrupt. 0: Allow LOSXAXB interrupt (default) 1: Mask (ignore) LOSXAXB for interrupt

3.3.3 Input OOF (Out-of-Frequency) Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its 0 ppm reference. This OOF reference can be selected as either:

- XAXB signal
- IN0, IN1, IN2, IN3

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky flag register bit stays asserted until cleared. Note that IN3 is only available as an OOF reference when the device is not in ZDM.

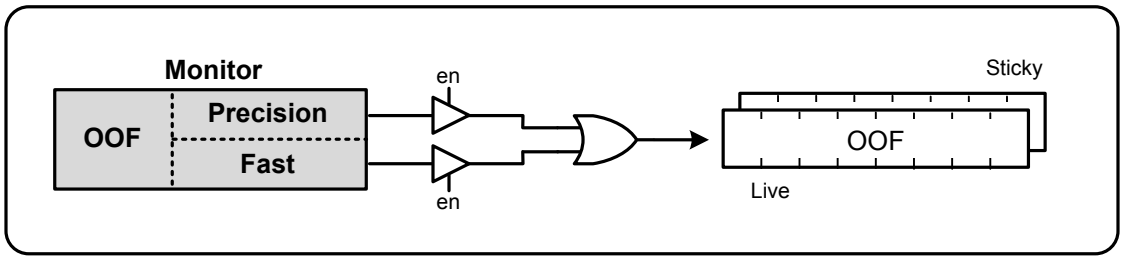


Figure 3.4. OOF Status Indicator

The Precision OOF monitor circuit measures the frequency of all input clocks to within up to ±2 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of from ±2 ppm to ±510 ppm in 2 ppm steps. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XAXB pins is available. These options are all register configurable.

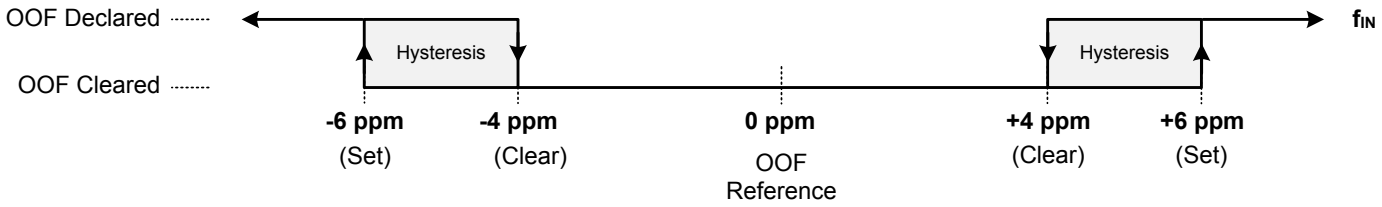


Figure 3.5. Example of Precision OOF Status Monitor Set and Clear Thresholds

The table below lists the OOF monitoring and control registers. Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. However, this may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF responds more quickly, and has larger thresholds.

Table 3.7. OOF Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
OOF Status and Controls		
OOF	0x000D[7:4]	OOF status indicators for IN3 - IN0. 0: Input signal detected or input buffer disabled or OOF disabled 1: Insufficient Input signal detected (OOF)

Register Name	Hex Address [Bit Field]	Function
OOF_FLG	0x0012[7:4]	OOF indicator sticky flag bits for IN3 - IN0. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
OOF_INTR_MSK	0x0018[7:4]	Masks OOF from generating INTRb interrupt for IN3 - IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt
Precision OOF Controls		
OOF_EN	0x003F[3:0]	Enable Precision OOF for IN3 - IN0. 0: Disable Precision OOF 1: Enable Precision OOF
OOF_REF_SEL	0x0040[2:0]	Selects clock used for OOF as the 0 ppm reference. Selections are: XAXB, IN0, IN1, IN2, IN3. Default is XAXB. Note that IN3 may not be used when the device is in ZDM.
OOF_SET_THR	0x0046[7:0]-0x0049[7:0]	OOF Set threshold for IN3 - IN0. Range is from ±2 ppm to ±510 ppm in 2 ppm steps.
OOF_CLR_THR	0x004A[7:0]-0x004D[7:0]	OOF Clear threshold for each input. Range is from ±2 ppm to ±510 ppm in 2 ppm steps.
Fast OOF Controls		
FAST_OOF_EN	0x003F[7:4]	Enable Fast OOF for IN3 - IN0. 0: Disable Precision OOF 1: Enable Precision OOF
FAST_OOF_SET_THR	0x0051[7:0]-0x0054[7:0]	Fast OOF Set threshold for IN3 - IN0. Range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps.
FAST_OOF_CLR_THR	0x0055[7:0]-0x0058[7:0]	OOF Clear threshold for each input. Range is from ±1,000 ppm to ±16,000 ppm in 1,000 ppm steps.

3.3.4 DSPLL LOL (Loss-of-Lock) Detection and the LOLb Output Indicator Pin

The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky flag register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

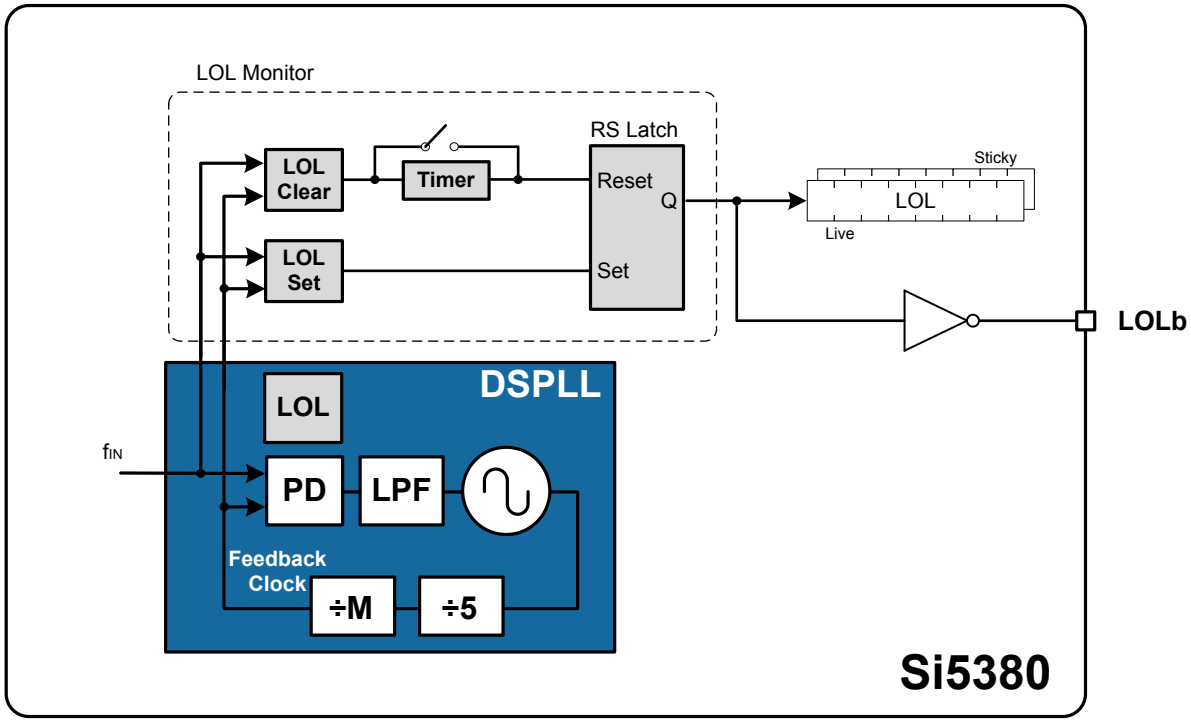


Figure 3.6. LOL Status Indicator

The LOL frequency monitor has an adjustable sensitivity which is register-configurable from ±1 ppm to ±10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 10 ppm frequency difference is shown in the figure below.

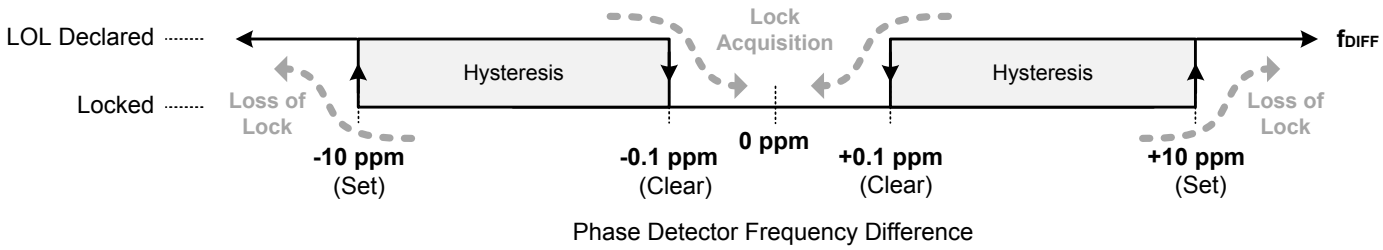


Figure 3.7. Example of LOL Set and Clear Thresholds

The settings in the following table are generated by ClockBuilder Pro.

Table 3.8. LOL Status Monitor and Control Registers

Register Name	Hex Address [Bit Field]	Function
LOL	0x000E[1]	LOL status indicator for the DSPLL. 0: DSPLL Locked to input clock 1: DSPLL Not locked to an input clock
LOL_FLG	0x0013[1]	LOL indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOL_INTR_MSK	0x0019[1]	Masks LOL from generating INTRb interrupt. 0: Allow LOL interrupt (default) 1: Mask (ignore) LOL for interrupt
LOL_SLW_SET_THR	0x009E[7:4]	Configures the loss of lock set thresholds. Selectable as 1,3,10,30,100,300,1000,3000,10000. Values are in ppm.
LOL_SLW_CLR_THR	0x00A0[7:4]	Configures the loss of lock set thresholds. Selectable as 0.1,0.3,1,3,10,30,100,300,1000,3000,10000. Values are in ppm.
LOL_CLR_DELAY	0x00A8[7:0]-0x00AB[2:0]	35-bit delay value for LOL Clear delay. The value is generated by ClockBuilder Pro.
LOL_TIMER_EN	0x00A2[1]	Enable for the LOL Clear Timer. 0: Disable LOL clear timer 1: Enable LOL clear timer

3.3.5 Device Status Monitoring

In addition to the input-driven LOS, LOSXAXB, OOF, LOL, and HOLD fault monitors discussed previously, there are several additional status monitors which may be useful in determining the device operating state. While some of these indicators may seem redundant, they are either taken from different locations in the device or are active in different operating modes. These indicators can provide further insight into the operating state of the device.

Table 3.9. Device Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
SYSINCAL	0x000C[0]	Device in Calibration status indicator. 0: Normal Operation 1: Device in Calibration
LOSREF	0x000C[2]	LOS status indicator for XAXB reference signal. 0: XAXB input signal detected 1: Insufficient XAXB input signal detected
XAXB_ERR	0x000C[3]	XAXB input locking status indicator. 0: XAXB Input Locked 1: XAXB Input Not locked
SMBUS_TMOUT	0x000C[5]	SMB Bus Timeout Indicator. 0: SMB Bus Timeout has Not occurred 1: SMB Bus Timeout Has occurred
CAL	0x000F[5]	DSPLL in Calibration status indicator. 0: Normal Operation 1: DSPLL in Calibration
SYSINCAL_FLG	0x0011[0]	SYSINCAL indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOSREF_FLG	0x0011[2]	LOSREF indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
XAXB_ERR_FLG	0x0011[3]	XAXB_ERR indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
SMBUS_TMOUT_FLG	0x0011[5]	SMBUS_TMOUT indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

Register Name	Hex Address [Bit Field]	Function
CAL_FLG	0x0014[5]	CAL indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

3.3.6 INTRb Interrupt Configuration

The INTRb interrupt output pin is a convenient way to monitor a change in state of one or more status indicator flags, though direct polling may also be used to monitor device status. Each of the status indicator flags is maskable to avoid unwanted assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the unmasked status flag register bit(s) that caused the interrupt. Note that the status flag register bits cannot be cleared if the corresponding status indicator is still showing a fault.

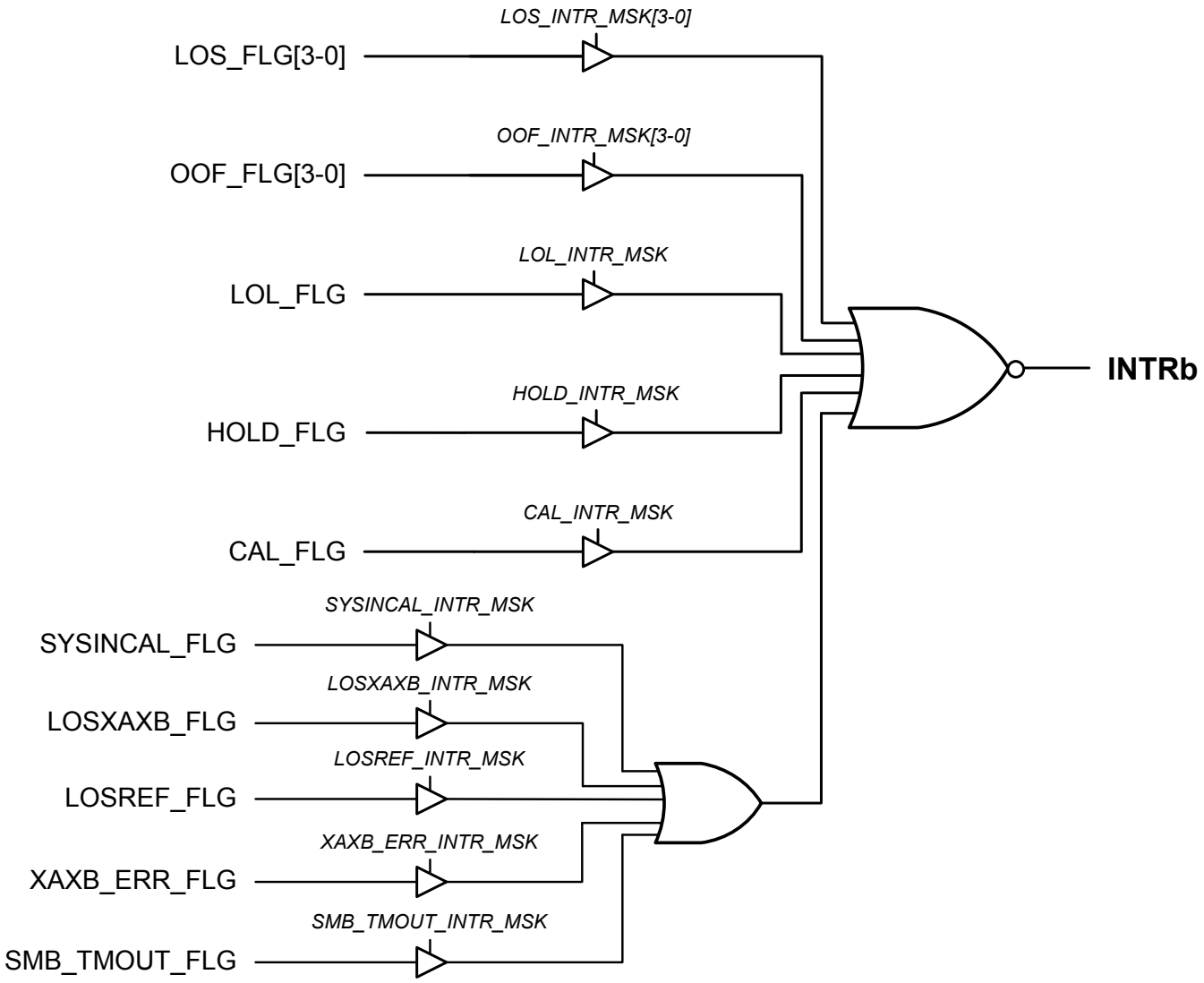


Figure 3.8. Interrupt Pin Source Masking Options

Table 3.10. INTRb Pin Interrupt Mask Registers

Register Name	Hex Address [Bit Field]	Function
LOS_INTR_MSK	0x0018[3:0]	Masks LOS from generating INTRb interrupt for IN3 - IN0. 0: Allow LOS interrupt (default) 1: Mask (ignore) LOS for interrupt

Register Name	Hex Address [Bit Field]	Function
OOF_INTR_MSK	0x0018[7:4]	Masks OOF from generating INTRb interrupt for IN3 - IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt
LOL_INTR_MSK	0x0019[1]	Masks LOL from generating INTRb interrupt. 0: Allow LOL interrupt (default) 1: Mask (ignore) LOL for interrupt
HOLD_INTR_MSK	0x0019[5]	Masks Holdover/Freerun from generating INTRb interrupt. 0: Allow Holdover/Freerun interrupt (default) 1: Mask (ignore) Holdover/Freerun for interrupt
CAL_INTR_MSK	0x001A[5]	Masks CAL from generating INTRb interrupt. 0: Allow CAL interrupt (default) 1: Mask (ignore) CAL for interrupt
SYSINCAL_INTR_MSK	0x0017[0]	Masks SYSINCAL from generating INTRb interrupt. 0: Allow SYSINCAL interrupt (default) 1: Mask (ignore) SYSINCAL for interrupt
LOSXAXB_INTR_MSK	0x0017[1]	Masks LOSXAXB from generating INTRb interrupt. 0: Allow LOSXAXB interrupt (default) 1: Mask (ignore) LOSXAXB for interrupt
LOSREF_INTR_MSK	0x0017[2]	Masks LOSREF from generating INTRb interrupt. 0: Allow LOSREF interrupt (default) 1: Mask (ignore) LOSREF for interrupt
XAXB_ERR_INTR_MSK	0x0017[3]	Masks XAXB_ERR from generating INTRb interrupt. 0: Allow XAXB_ERR interrupt (default) 1: Mask (ignore) XAXB_ERR for interrupt
SMB_TMOUT_INTR_MSK	0x0017[5]	Masks SMB_TMOUT from generating INTRb interrupt. 0: Allow SMB_TMOUT interrupt (default) 1: Mask (ignore) SMB_TMOUT for interrupt

4. Output Clocks

Each output driver has configurable output amplitude and common mode voltage, covering a wide variety of differential signal output formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3, 2.5, or 1.8V) providing up to 20 single-ended outputs or any combination of differential and single-ended outputs. Unused outputs may be left unconnected.

4.1 Output Crosspoint Switch

A crosspoint switch allows any of the output drivers to connect with any of the Output N dividers as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up. Any N divider can source multiple, or even all, output drivers.

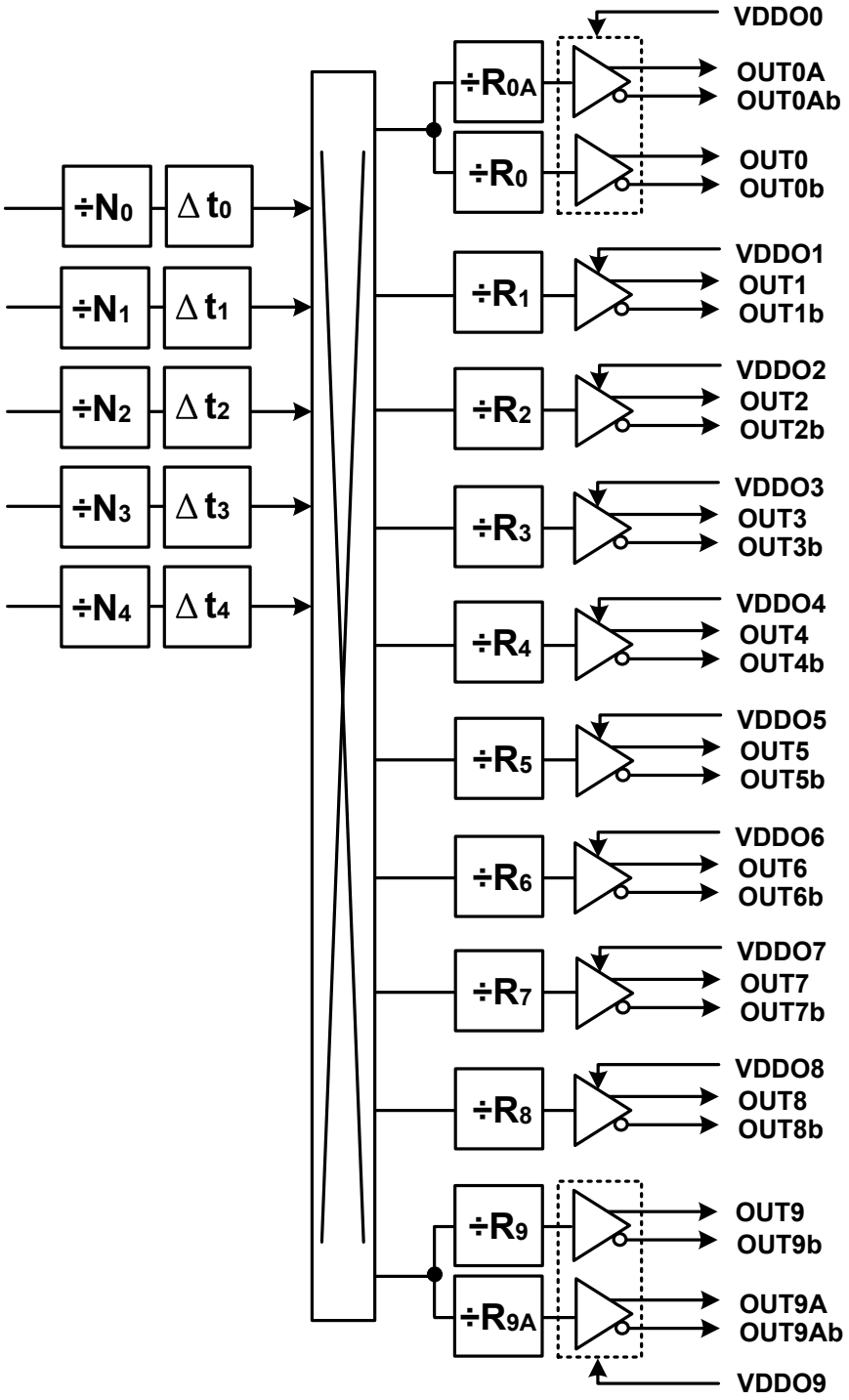


Figure 4.1. N Divider to Output Driver Crosspoint

The following table is used to set up the routing from the N divider frequency selection to the output.

Table 4.1. Output Crosspoint Configuration Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_MUX_SEL	0x0106[2:0]	Connects the output drivers to one of the N divider sources. Selections are: 0: N0 1: N1 2: N2 3: N3 4: N4 5-7: Reserved
OUT0_MUX_SEL	0x010B[2:0]	
OUT1_MUX_SEL	0x0110[2:0]	
OUT2_MUX_SEL	0x0115[2:0]	
OUT3_MUX_SEL	0x011A[2:0]	
OUT4_MUX_SEL	0x011F[2:0]	
OUT5_MUX_SEL	0x0124[2:0]	
OUT6_MUX_SEL	0x0129[2:0]	
OUT7_MUX_SEL	0x012E[2:0]	
OUT8_MUX_SEL	0x0133[2:0]	
OUT9_MUX_SEL	0x0138[2:0]	
OUT9A_MUX_SEL	0x013D[2:0]	

4.1.1 Output R Divider Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable output phase alignment. Resetting the device using the RSTb pin or asserting the Hard Reset bit 0x001E[1] will give the same result. Also, the output R dividers can be reset by driving the SYNCb input pin low or by setting the SYNC register bit (0x001E[2]) high.

Soft Reset does not affect the output synchronization, though it will load any updated Nx_DELAY values to adjust the relative delays between outputs. See 4.7 Output Delay Control (Δt0 – Δt4) for more information.

4.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are located close to one another, the laws of physics dictate that there will be some amount of crosstalk. The Integer-divider nature of the Si5380 greatly reduces the chances for crosstalk, as all clock output frequencies are divided from the same VCO frequency. However, the phase noise of the Si5380 is so low that crosstalk may still be detected in certain cases. Crosstalk occurs at both the device level, as well as the PCB level. It is difficult (and possibly irrelevant) to allocate the crosstalk contributions between these two sources since it can only be measured, while the Si5380 is mounted on a PCB.

In addition to following the PCB layout guidelines given in 9. Crystal and Device Circuit Layout Recommendations, crosstalk can be minimized by modifying the placements of the different output clock frequencies. For example, consider the following lineups of output clocks in the table below. The “Clock Placement Wizard ...” button on the “Define Output Frequencies” page of ClockBuilder Pro provides an easy way to change the frequency placements by either Manual or Automatic means.

Table 4.2. Comparison of Output Clock Frequency Placement Choices

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0A	122.88	122.88
0	122.88	122.88
1	7.68	61.44
2	7.68	7.68
3	7.68	92.16
4	7.68	7.68
5	491.52	491.52
6	92.16	7.68
7	76.8	76.8
8	61.44	7.68
9	256.76	256.76
9A	256.76	256.76

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. A 76.8 MHz clock should not be next to a 92.16 MHz clock as crosstalk will be observed at 15.36 MHz from each frequency. If the jitter integration bandwidth or spur range goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Frequency values that are integer multiples of one another should be grouped together. Noting that because 61.44 x 2 = 122.88 and 7.68 = 61.44 / 8 = 92.16 / 12 = 491.52 / 64 = 76.8 / 10 = 245.76 / 32, it is okay to place each of these frequency values next to one another.
3. Unused outputs can also be placed to separate clock outputs that might otherwise show crosstalk.
4. If some outputs have tighter spur requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk.
5. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided whenever possible. When CMOS is unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see AN862 “Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems.”

4.3 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL, HCSL. For CML applications, see Appendix 1. Custom Differential Amplitude Controls. The standard formats can be either Normal or Low-Power. Low-Power format uses less power for the same amplitude but has the drawback of slower rise/fall times. The source impedance in the Low-Power format is higher than 100 Ω. See Appendix 1. Custom Differential Amplitude Controls for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs. Note also that CMOS output can create much more crosstalk than differential outputs so extra care must be taken in their pin replacement so that other clocks that need best spur performance are not on nearby pins. See “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for additional information.

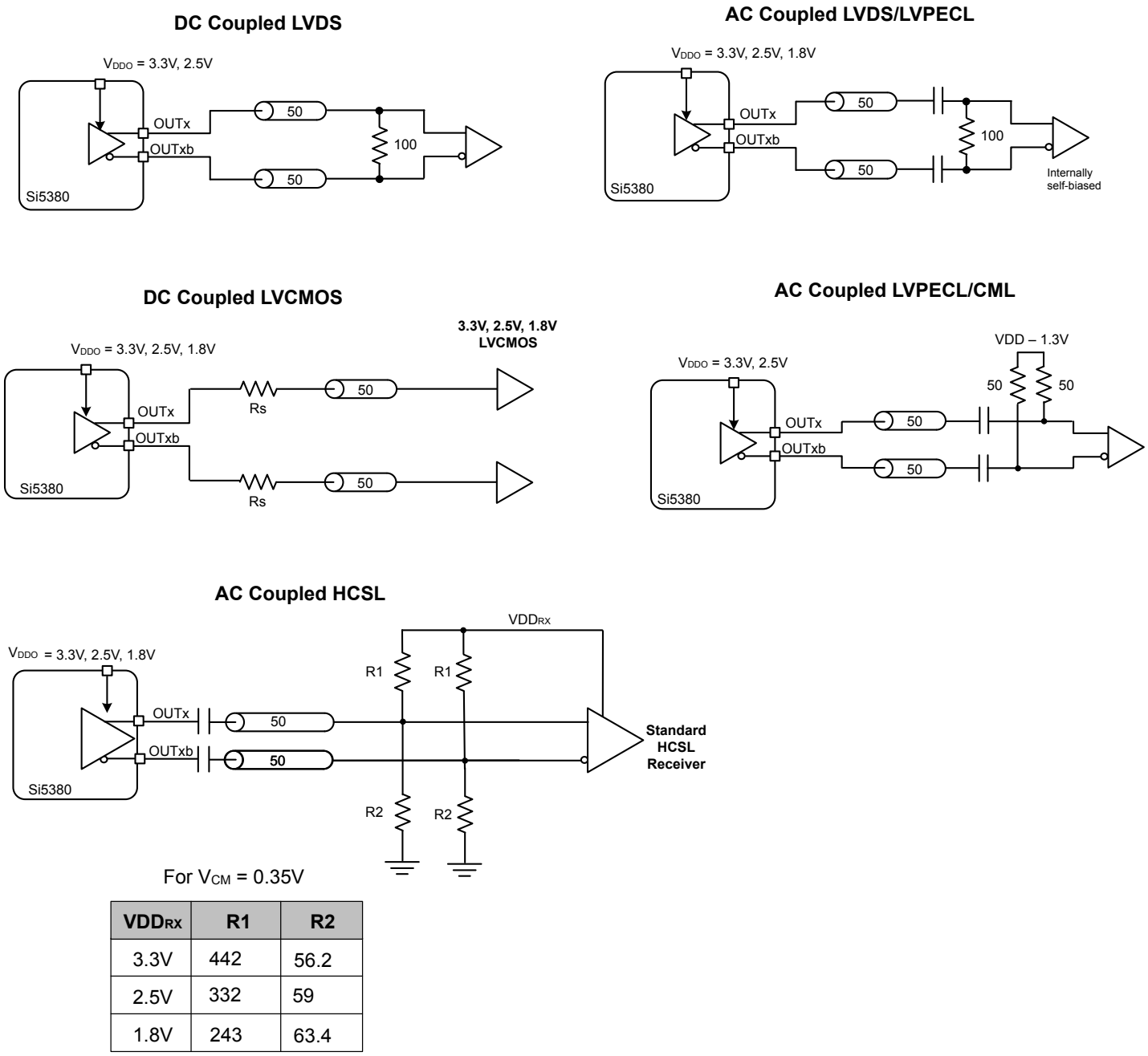
Table 4.3. Output Signal Format Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_FORMAT	0x0104[2:0]	Selects the output signal format as differential or LVCMOS mode. 0: Reserved 1: Normal Differential 2: Low-Power Differential 3: Reserved 4: LVCMOS 5-7: Reserved
OUT0_FORMAT	0x0109[2:0]	
OUT1_ FORMAT	0x010E[2:0]	
OUT2_ FORMAT	0x0113[2:0]	
OUT3_ FORMAT	0x0118[2:0]	
OUT4_ FORMAT	0x011D[2:0]	
OUT5_ FORMAT	0x0122[2:0]	
OUT6_ FORMAT	0x0127[2:0]	
OUT7_ FORMAT	0x012C[2:0]	
OUT8_ FORMAT	0x0131[2:0]	
OUT9_ FORMAT	0x0136[2:0]	
OUT9A_FORMAT	0x013B[2:0]	

4.4 Differential Outputs

4.4.1 Differential Output Terminations

The differential output drivers support both ac and dc-coupled terminations as shown in the following figure.



For V_{CM} = 0.35V

VDDRX	R1	R2
3.3V	442	56.2
2.5V	332	59
1.8V	243	63.4

Figure 4.2. Supported Differential Output Terminations

4.4.2 Differential Output Amplitude Controls

The differential amplitude of each output can be controlled with the following registers. See Table 4.6 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 35 for recommended OUTx_AMPL settings for common signal formats. See Appendix 1. Custom Differential Amplitude Controls for register settings for non-standard amplitudes.

Table 4.4. Differential Output Voltage Swing Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_AMPL	0x0105[6:4]	Sets the voltage swing for the differential output drivers for both Normal and Low-Power modes.
OUT0_AMPL	0x010A[6:4]	
OUT1_ AMPL	0x010F[6:4]	
OUT2_ AMPL	0x0114[6:4]	
OUT3_ AMPL	0x0119[6:4]	
OUT4_ AMPL	0x011E[6:4]	
OUT5_ AMPL	0x0123[6:4]	
OUT6_ AMPL	0x0128[6:4]	
OUT7_ AMPL	0x012D[6:4]	
OUT8_ AMPL	0x0132[6:4]	
OUT9_ AMPL	0x0137[6:4]	
OUT9A_ AMPL	0x013C[6:4]	

4.4.3 Differential Output Common Mode Voltage Selection

The common mode voltage (VCM) for differential output Normal and Low-Power modes is selectable depending on the supply voltage provided at the output's VDDO pin. See the table below for recommended OUTx_CM settings for common signal formats. See Appendix 1. Custom Differential Amplitude Controls " for recommended OUTx_CM settings when using custom output amplitude.

Table 4.5. Differential Output Common Mode Voltage Selection Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_CM	0x0105[3:0]	Sets the common mode voltage for the differential output driver.
OUT0_CM	0x010A[3:0]	
OUT1_ CM	0x010F[3:0]	
OUT2_ CM	0x0114[3:0]	
OUT3_ CM	0x0119[3:0]	
OUT4_ CM	0x011E[3:0]	
OUT5_ CM	0x0123[3:0]	
OUT6_ CM	0x0128[3:0]	
OUT7_ CM	0x012D[3:0]	
OUT8_ CM	0x0132[3:0]	
OUT9_ CM	0x0137[3:0]	
OUT9A_ CM	0x013C[3:0]	

4.4.4 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low-Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low (See 4.6.1 Output Driver State When Disabled for details.)

The Normal mode setting includes an internal 100 W resistor between the OUT and OUTb pins. In Low-Power mode, this resistor is removed, resulting in a higher output impedance. The increased impedance creates larger amplitudes for the same power while reducing edge rates, which may increase jitter or phase noise. In either mode, the differential receiver must be properly terminated to the PCB trace impedance for good system signal integrity. Note that ClockBuilder Pro does not provide Low-Power mode settings. Contact Silicon Labs Technical Support for assistance with Low-Power mode use.

Amplitude controls are as described in the previous section and also in more detail in Appendix 1. Custom Differential Amplitude Controls ". Common mode voltage selection is also described in more detail in this appendix.

Table 4.6. Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Standard	VDDO	Mode	OUTx_FORMAT	OUTx_CM	OUTx_AMPL
	(V)		(dec)	(dec)	(dec)
LVPECL	3.3	Normal	1	11	6
LVPECL	2.5	Normal	1	11	6
LVPECL	3.3	Low-Power	2	11	3
LVPECL	2.5	Low-Power	2	11	3
LVDS	3.3	Normal	1	3	3
LVDS	2.5	Normal	1	11	3
Sub-LVDS[1]	1.8	Normal	1	13	3
LVDS	3.3	Low-Power	2	3	1
LVDS	2.5	Low-Power	2	11	1
Sub-LVDS[1]	1.8	Low-Power	2	13	1
HCSL[2]	3.3	Low-Power	2	11	3
HCSL[2]	2.5	Low-Power	2	11	3
HCSL[2]	1.8	Low-Power	2	13	3

Notes:

1. The Sub-LVDS common mode voltage is not compliant with LVDS standards. Therefore, AC coupling the driver to an LVDS receiver is highly recommended in this case.

2. Creates HCSL compatible signals, see HCSL receiver biasing network in Figure 15.

The output differential driver can also produce a wide range of CML compatible output amplitudes. See Appendix 1. Custom Differential Amplitude Controls for additional information.

4.5 LVCMOS Outputs

4.5.1 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in the following figure.

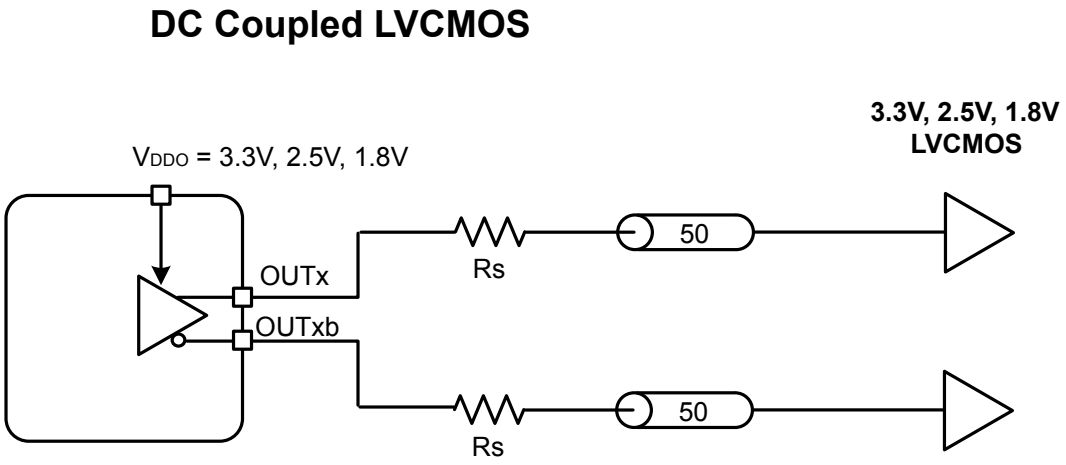


Figure 4.3. LVCMOS Output Terminations

4.5.2 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A series source termination resistor (Rs) is recommended close to the output to match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance – Zs). There are multiple programmable output impedance selections for each VDDO option as shown in the following table. Generally, the lowest impedance for a given supply voltage is preferable, since it will give the fastest edge rates.

Table 4.7. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Driver Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x1	38 W	10 mA
	0x2	30 W	12 mA
	0x3[1]	22 W	17 mA
2.5 V	0x1	43 W	6 mA
	0x2	35 W	8 mA
	0x3[1]	24 W	11 mA
1.8 V	0x3[1]	31 W	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages.

Table 4.8. LVCMOS Drive Strength Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_CMOS_DRV	0x0104[7:6]	LVCMOS output impedance. See the table above for settings.
OUT0_CMOS_DRV	0x0109[7:6]	
OUT1_ CMOS_DRV	0x010E[7:6]	
OUT2_ CMOS_DRV	0x0113[7:6]	
OUT3_ CMOS_DRV	0x0118[7:6]	
OUT4_ CMOS_DRV	0x011D[7:6]	
OUT5_ CMOS_DRV	0x0122[7:6]	
OUT6_ CMOS_DRV	0x0127[7:6]	
OUT7_ CMOS_DRV	0x012C[7:6]	
OUT8_ CMOS_DRV	0x0131[7:6]	
OUT9_ CMOS_DRV	0x0136[7:6]	
OUT9A_ CMOS_DRV	0x013B[7:6]	

4.5.3 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

4.5.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUT and OUTb). By default the clock on the OUTb pin is generated with the same polarity (in phase) with the clock on the OUT pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers. Note that these settings have no effect on the differential-mode output driver.

Table 4.9. LVCMOS Output Polarity Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_INV	0x0106[7:6]	Controls the output polarity of the OUT and OUT pins when in LVCMOS mode. Selections are shown below in the table below.
OUT0_INV	0x010B[7:6]	
OUT1_INV	0x0110[7:6]	
OUT2_INV	0x0115[7:6]	
OUT3_INV	0x011A[7:6]	
OUT4_INV	0x011F[7:6]	
OUT5_INV	0x0124[7:6]	
OUT6_INV	0x0129[7:6]	
OUT7_INV	0x012E[7:6]	
OUT8_INV	0x0133[7:6]	
OUT9_INV	0x0138[7:6]	
OUT9A_INV	0x013D[7:6]	

Table 4.10. LVCMOS Output Polarity of OUT and OUTb Pins

OUTx_INV Register Settings	OUT	OUTb	Comment
0x00	CLK	CLK	Both in phase (default)
0x01	CLK	CLKb	Non-inverted
0x02	CLKb	CLK	Inverted
0x03	CLKb	CLKb	Both out of phase

4.6 Output Enable/Disable

Each output driver may be individually placed in one of three operating states:

- “Enabled” state is the normal state for output clock operation. The output clock is toggling and the differential common mode voltage will be generated, if selected by the output format.
- “Disabled” state gates off clock operation and places the output into a static, user-selectable, logic state. Differential output common mode voltage is maintained, if selected by the output format, allowing a quick transition back to Enabled state operation with minimal common mode disruption.
- “Powerdown” state removes power from the output driver and leaves the output pins high-impedance. In this state, regardless of output format, the output common mode voltage is not generated and the output pin voltages are not well defined. Powerdown is recommended for unused outputs as well as startup or long-term power reduction, where differential common voltage generation restart will not introduce issues in the system. See 10.1 Power Management Features for more information on powerdown.

The OEb pin provides a convenient method of enabling or disabling all of the output drivers at the same time. Holding the OEb pin low enables all of the outputs, while driving it high disables all outputs. In addition to pin control, flexible register controls described in the following sections allow further customization for each application. Note that any one disable control can disable the corresponding output(s) even if all other sources controls are enabled. See the sections below, especially 4.6.5 Output Driver Disable Source Summary , for more information on manual and automatic disable controls.

Table 4.11. Output Enable/Disable Manual Control Registers

Register Name	Hex Address [Bit Field]	Function
OUTALL_DISABLE_LOW	0x0102[0]	Enable/Disable all output drivers. If the OEb pin is held high, then all outputs will be disabled regardless of the state of this or the OUTx_OE register bits. 0: Disable All outputs (default) 1: Enable All outputs
OUT0A_OE	0x0103[1]	Enable/Disable individual outputs. Note that the OEb pin must be held low and OUTALL_DISABLE_LOW = 1 in order to enable an output. 0: Disable Output (default) 1: Enable Output
OUT0_OE	0x0108[1]	
OUT1_OE	0x010D[1]	
OUT2_OE	0x0112[1]	
OUT3_OE	0x0117[1]	
OUT4_OE	0x011C[1]	
OUT5_OE	0x0121[1]	
OUT6_OE	0x0126[1]	
OUT7_OE	0x012B[1]	
OUT8_OE	0x0130[1]	
OUT9_OE	0x0135[1]	
OUT9A_OE	0x013A[1]	

4.6.1 Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable logic low or disable logic high.

Table 4.12. Output Driver Disable State Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_DIS_STATE	0x0104[5:4]	Determines the static state of an output driver when disabled. 0: Disable logic low 1: Disable logic high 2-3: Reserved
OUT0_DIS_STATE	0x0109[5:4]	
OUT1_ DIS_STATE	0x010E[5:4]	
OUT2_ DIS_STATE	0x0113[5:4]	
OUT3_ DIS_STATE	0x0118[5:4]	
OUT4_ DIS_STATE	0x011D[5:4]	
OUT5_ DIS_STATE	0x0122[5:4]	
OUT6_ DIS_STATE	0x0127[5:4]	
OUT7_ DIS_STATE	0x012C[5:4]	
OUT8_ DIS_STATE	0x0131[5:4]	
OUT9_ DIS_STATE	0x0136[5:4]	
OUT9A_ DIS_STATE	0x013B[5:4]	

4.6.2 Synchronous Output Enable/Disable Feature

Each of the output drivers has individually selectable synchronous or asynchronous enable/disable behavior. Output drivers with Synchronous enable/disable will wait until a clock period has completed before changing the enable state. This prevents unwanted shortened “runt” pulses from occurring. Output drivers with Asynchronous enable/disable will change the enable state immediately, without waiting for the entire clock period to complete. This selection affects both manual as well as automatic output enables and disables.

Table 4.13. Synchronous Enable/Disable Control Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_SYNC_EN	0x0104[3]	Synchronous output Enable/Disable selection. 0: Asynchronous Enable/Disable (default) 1: Synchronous Enable/Disable
OUT0_SYNC_EN	0x0109[3]	
OUT1_ SYNC_EN	0x010E[3]	
OUT2_ SYNC_EN	0x0113[3]	
OUT3_ SYNC_EN	0x0118[3]	
OUT4_ SYNC_EN	0x011D[3]	
OUT5_ SYNC_EN	0x0122[3]	
OUT6_ SYNC_EN	0x0127[3]	
OUT7_ SYNC_EN	0x012C[3]	
OUT8_ SYNC_EN	0x0131[3]	
OUT9_ SYNC_EN	0x0136[3]	
OUT9A_SYNC_EN	0x013B[3]	

4.6.3 Automatic Output Disable During LOL

By default, a DSPLL that is out of lock will generate an output clock. There is an option to disable the outputs when the DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into Holdover.

4.6.4 Automatic Output Disable During LOSXAXB

The internal oscillator circuit, in combination with the external crystal, provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an LOSXAXB fault. By default all outputs will be disabled during assertion of the LOSXAXB fault.

Table 4.14. Output Automatic Disable on LOL and LOSXAXB Registers

Register Name	Hex Address [Bit Filed]	Function
OUT_DIS_MSK_LOL	0x0142[1]	Determines if the outputs are disabled during an LOL condition. 0: Disable all outputs on LOL (default) 1: Normal Operation during LOL
OUT_DIS_MSK_LOSXAXB	0x0141[6]	Determines if outputs are disabled during an LOSXAXB condition. 0: Disable all outputs on LOSXAXB (default) 1: All outputs remain enabled during LOSXAXB

4.6.5 Output Driver Disable Source Summary

There are a number of conditions that may cause the outputs to be automatically disabled. The user may mask out unnecessary disable sources to match system requirements. Any one of the unmasked sources may cause the output(s) to be disabled; this is more powerful, but similar in concept, to common “wired-OR” configurations. The table below summarizes the output disable sources with additional information for each source.

Table 4.15. Output Driver Summary of Disable Sources

Output Driver Disable Source	Disable Output(s) when Source...	Outputs Individually Assignable?	User Maskable?	Related Registers [bits]	Comments
OUTALL_DISABLE_LOW	Low	N	N	0x0102[0]	User Controllable
OUT0A_OE	Low	Y	N	0x0103[1]	User Controllable
OUT0_OE				0x0108[1]	
OUT1_OE				0x010D[1]	
OUT2_OE				0x0112[1]	
OUT3_OE				0x0117[1]	
OUT4_OE				0x011C[1]	
OUT5_OE				0x0121[1]	
OUT6_OE				0x0126[1]	
OUT7_OE				0x012B[1]	
OUT8_OE				0x0130[1]	
OUT9_OE				0x0135[1]	
OUT9A_OE				0x013A[1]	
OEb (pin)	High	Y	N	0x0022[1:0], 0x0023[7:0], 0x0024[3:0]	User Controllable
OE (register)	Low				
LOL	High	N	Y	0x000D[1], 0x0142[1]	Maskable
LOSXAXB	High	N	Y	0x000C[1], 0x0141[6]	Maskable
SYSINCAL	High	N	N	0x000C[0]	Automatic, not user controllable or maskable

4.7 Output Delay Control (Δt0 – Δt4)

The Si5380 uses independently adjustable output N dividers (N0 - N4) to generate up to 5 unique top frequencies to its 12 outputs through the output crosspoint switch. By default all output clocks are aligned. Each N divider has an independently adjustable delay path (Δt0 – Δt4) associated with it. Each of these dividers is available for applications that require deterministic output delay configuration. This is useful for PCB trace length mismatch compensation or for applications that require quadrature clock generation. Delay adjustments are bidirectional over ±8.6 ns in 68 ps steps and are programmed through registers. An example of generating two frequencies with unique configurable path delays of Δt2 and Δt3 is shown in the figure below.

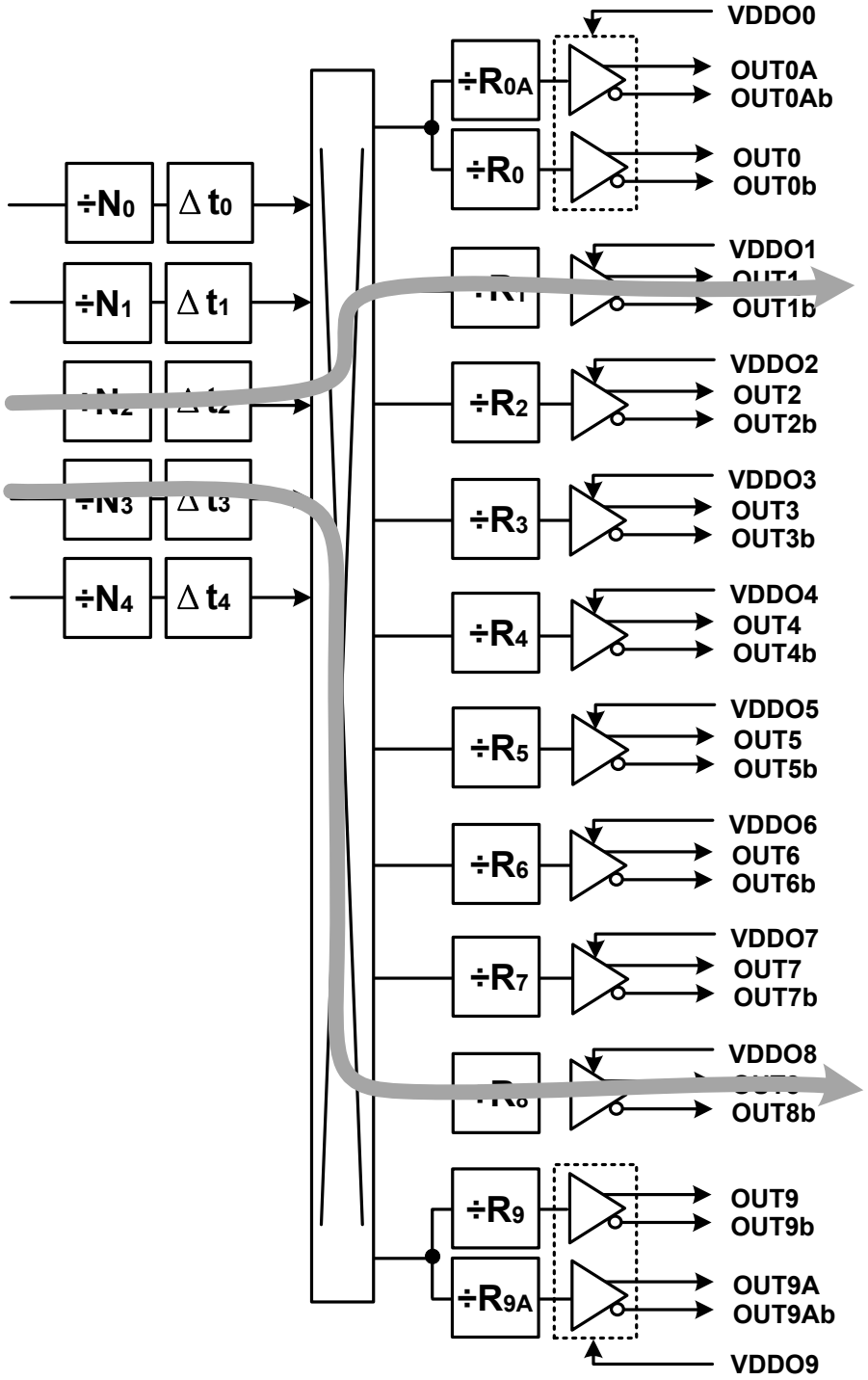


Figure 4.4. Example of Independently-Configurable Path Delays

A Soft Reset of the device, SOFT_RST (0x001C[0] = 1), is required to latch in the new bidirectional delay value(s). All delay values are restored to their default values after POR, RSTb, or Hard Reset. Delay default values can be written to NVM, allowing a custom delay offset configuration at power-up or after a Hard Reset.

Table 4.16. Output Delay Adjustment Registers

Register Name	Hex Address [Bit Field]	Function
N0_DELAY	0x035A[7:0]	8-bit 2s-complement delay values. Nx_Delay values range between -128 and +127, inclusive. t_{DLY} = Nx_DELAY * 67.8 ps f_{vco}=14.7456 GHz, 1/f_{vco}=67.8 ps
N1_DELAY	0x035C[7:0]	
N2_DELAY	0x035E[7:0]	
N3_DELAY	0x0360[7:0]	
N4_DELAY	0x0362[7:0]	

5. Zero Delay Mode

A Zero Delay Mode is available for applications that require consistent minimum fixed delay between the selected input and outputs. The Zero Delay Mode is configured by opening the internal DSPLL feedback loop through software configuration and then closing the loop externally as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9A output and FB_IN input pins are recommended for the external feedback connection in the Si5380 to minimize the overall distance and delay. In this case the pairs of pins are adjacent and polarized in such a way that no vias are required to make this connection. The FB_IN input pins must be terminated and ac-coupled as shown below when Zero Delay Mode is used. A differential external feedback path connection is necessary for best performance.

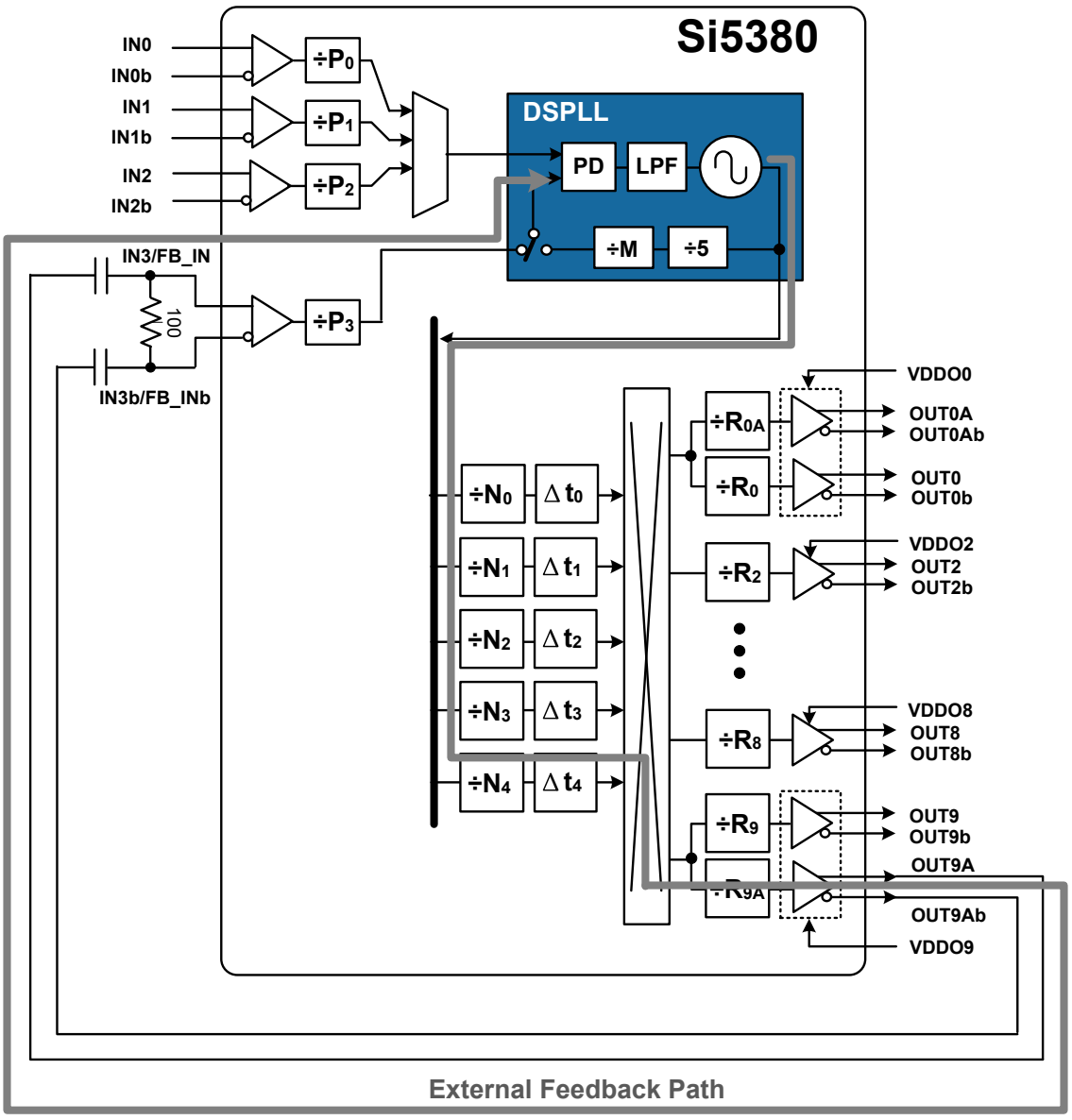


Figure 5.1. Zero Delay Mode (ZDM) Setup

To enable ZDM, set ZDM_EN 0x0487[0] = 1. In ZDM, the DSPLL cannot use either Hitless switching or Automatic switching. The DSPLL input clock selection between IN0, IN1, and IN2 must be made manually. As with manual input clock switching discussed earlier in this manual, the ZDM manual selection can be done by either pins or by register, depending on the state of the IN_SEL_REGCTRL register bit. The table below lists the register controls used for the Zero Delay Mode.

Table 5.1. Zero Delay Mode Registers

Register Name	Hex Address [Bit Field]	Function
ZDM_EN	0x0487[0]	Enable ZDM. 0: Disable Zero Delay Mode (default) 1: Enable Zero Delay Mode
IN_SEL_REGCTRL	0x052A[0]	Manual Input Select control source. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection
IN_SEL	0x052A[2:1]	Manual Input Select selection register. 0: IN0 (default) 1: IN1 2: IN2 3: Reserved

6. Serial Interface

Configuration and operation of the Si5380 is controlled by reading and writing registers using the I²C or SPI interface. The I²C_SEL pin selects I²C or SPI operation. The Si5380 supports communication with a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI interface supports both 4-wire or 3-wire modes by setting the SPI_3WIRE (0x002B[3]) configuration bit. See the figure below for supported modes of operation and settings. All digital I/O pins are 3.3 V-tolerant, even when operating at 1.8 V. Additionally, the pins with internal pull-ups, I2C_SEL and A0/CS are pulled-up to 3.3 V through a high impedance pull-up, regardless of IO_VDD_SEL setting.

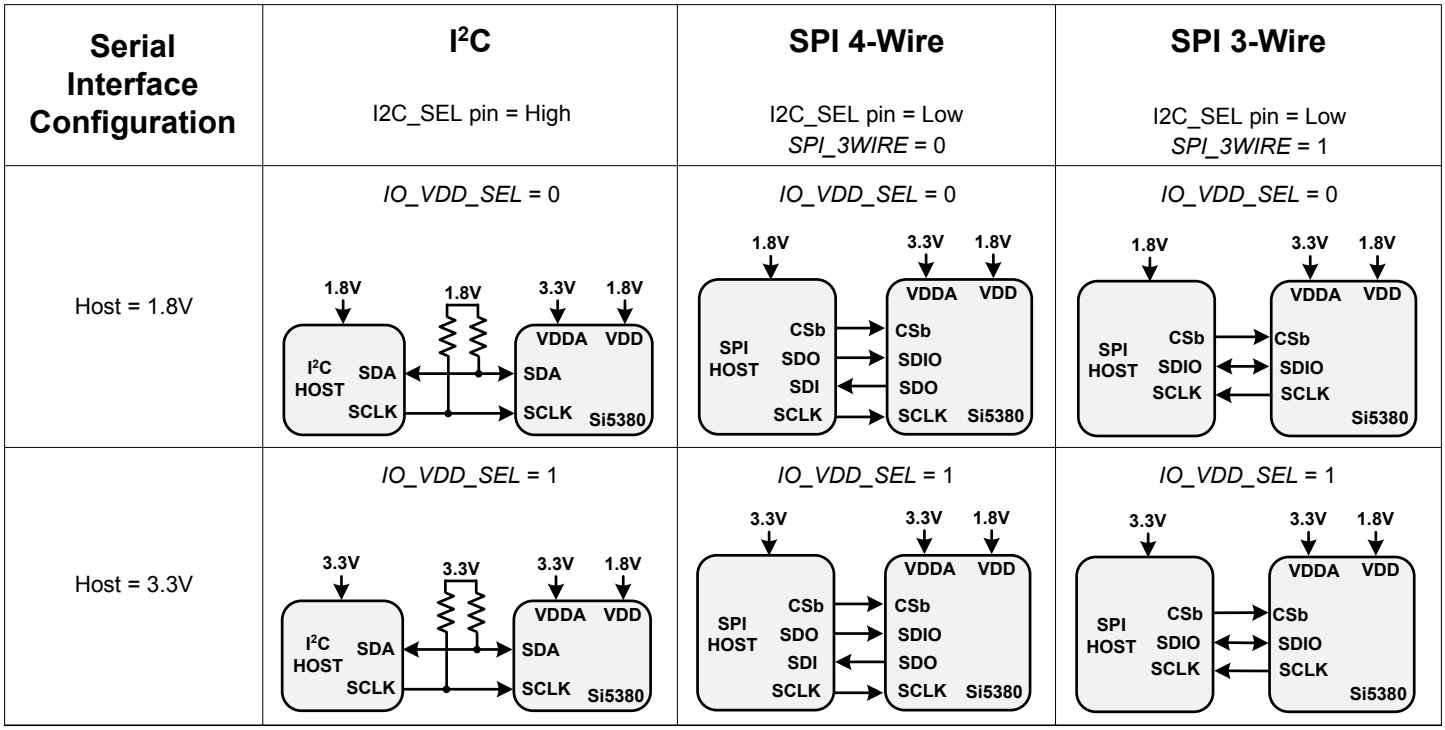


Figure 6.1. I2C/SPI Device Connectivity Configurations

In some cases it is not known prior to the design, what the serial interface type and I/O voltage will be. Setting the device to 1.8 V (IO_VDD_SEL = 0) digital I/O in the NVM allows the host to reliably write the device, regardless of its operating voltage. Once the serial interface type has been chosen using the I²C_SEL pin, the device may be written successfully regardless of the host interface type. This is true for both 3-wire and 4-wire SPI modes as well as I²C. The SPI serial data is written to the same SDA/SDIO input pin in all cases. At this point, the device can be configured to adjust IO_VDD_SEL for optimum 3.3 V operation and to select SPI_3WIRE between 3-/4-wire SPI modes. These mode changes are made immediately and no delays or wait times are needed for subsequent serial interface operations, including read operations.

Note that the registers are organized into multiple pages to allow a larger register set, given the limitations of the I²C/SPI interface standards. First, the correct page must be selected with the initial write. Then the register location within that page can be read/written. See for more information on register paging.

If neither serial interface is used, the SDA/SDIO, A1/SDO, and SCLK pins must be pulled either high or low externally since they are not pulled internally. I²C_SEL and A0/CSb have internal pull-ups and may be left unconnected in this case. Note that the Si5380 is not I²C failsafe upon loss of power. Applications that require failsafe operation should isolate the device from a shared I²C bus.

The following table lists register settings of interest for the I²C/SPI serial interface operation.

Table 6.1. I2C/SPI Configuration Registers

Register Name	Hex Address [Bit Field]	Function
IO_VDD_SEL	0x0943[0]	Select digital I/O operating voltage. 0: 1.8 V digital I/O connections (default) 1: 3.3 V digital I/O connections

Register Name	Hex Address [Bit Field]	Function
SPI_3WIRE	0x002B[3]	Selects operating mode for SPI interface: 0: 4-wire SPI (default) 1: 3-wire SPI
I2C_ADDR	0x000B[6:0]	7-bit I2C Address. See 6.1 I²C Interface for more information.

6.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and operates in either Standard-Mode (100 kbps) or Fast-Mode (400 kbps) while supporting burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure below. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kW) as recommended by the I2C specification. Two address select pins, A1 and A0, are provided, allowing up to four Si5380 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

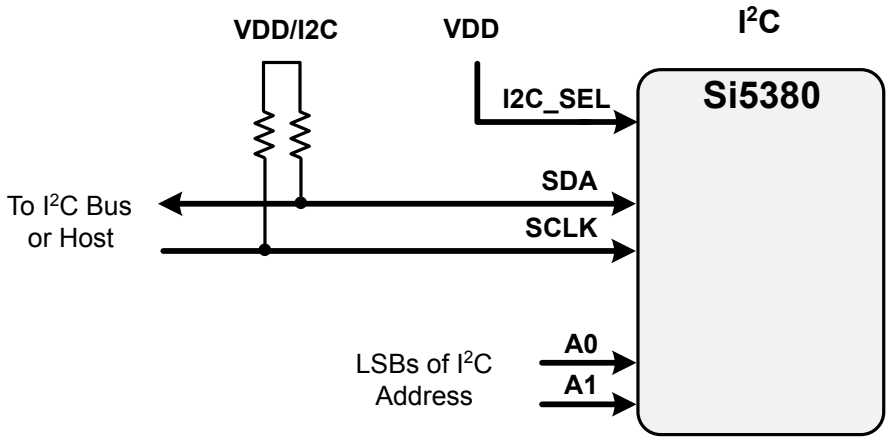


Figure 6.2. I2C Configuration

The 7-bit I²C slave device address of the Si5380 consists of a 5-bit fixed address plus two bit determined by the voltages on the A1 and A0 input pins, as shown in the figure below.

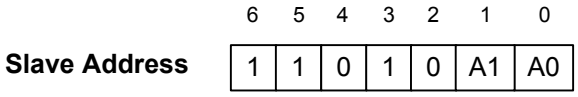


Figure 6.3. 7-bit I2C Slave Address Bit-Configuration

The I²C bus supports SDA timeout for compatibility with SMB Bus interfaces. The error indicator and flag are listed in the registers listed in the table below. See 3.3 Fault Monitoringfor more information.

Table 6.2. SMB Bus Timeout Error Registers

Register Name	Hex Address [Bit Field]	Function
SMB_TMOUT	0x000C[5]	SMB Bus Timeout Indicator. 0: SMB Bus Timeout has Not occurred 1: SMB Bus Timeout Has occurred
SMB_TMOUT_FLG	0x0011[5]	SMB_TMOUT indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in the figure below. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

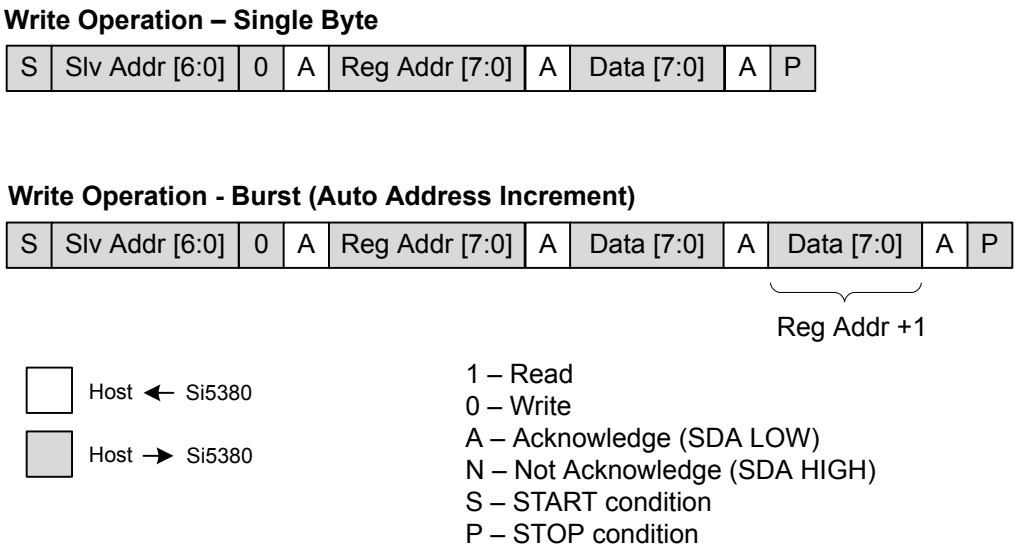


Figure 6.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the following figure.

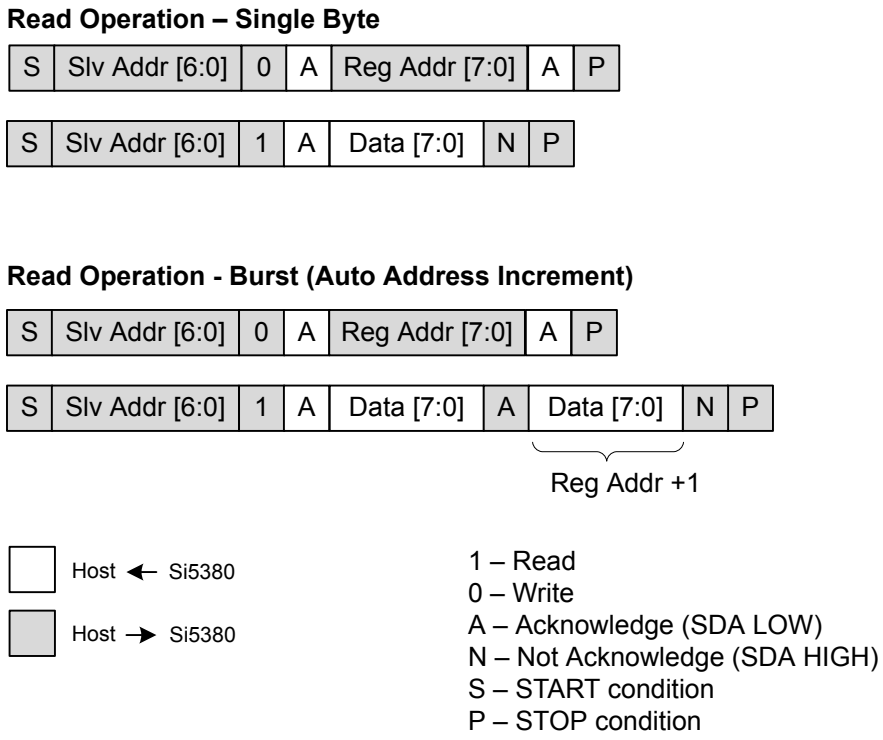


Figure 6.5. I²C Read Operation

6.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit, 0x000B[3]. The 4-wire interface consists of a clock input (SCLK), a chip select input (CSb), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the following figure.

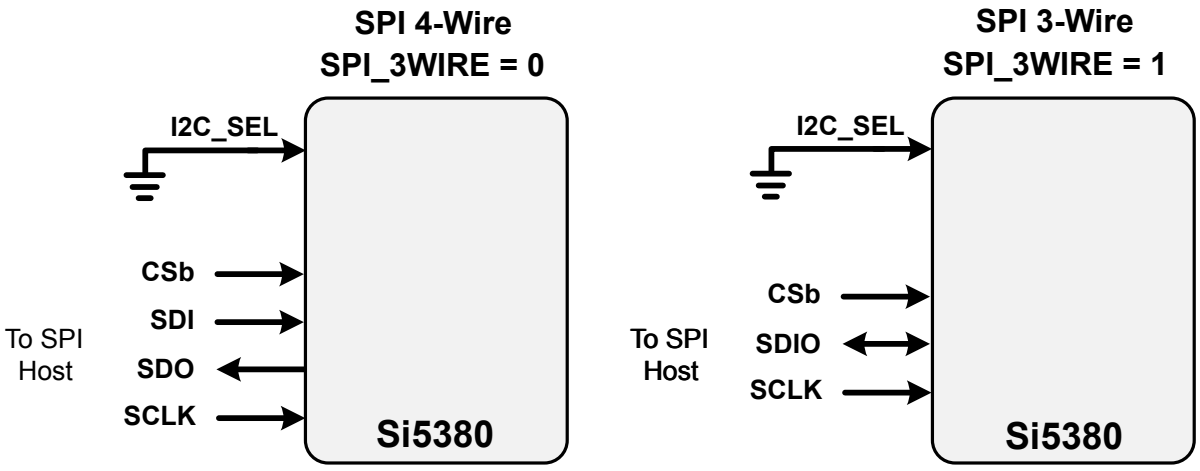


Figure 6.6. SPI Interface Connections

Table 6.3. SPI Command Formats

Instruction	Ist Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	-	-
Write Data	010x xxxx	8-bit Data	-	-
Read Data	100x xxxx	8-bit Data	-	-
Write Data + Address Increment	011x xxxx	8-bit Data	-	-
Read Data + Address Increment	101x xxxx	8-bit Data	-	-
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Note:
1. X = don't care (1 or 0)
2. The Burst Write Command is terminated by de-asserting CSb (CSb = high)
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a “Set Address” command followed by a “Write Data” or “Read Data” command. The 'Write Data + Address Increment' or “Read Data + Address Increment” commands are available for cases where multiple byte operations in sequential address locations is necessary. The “Burst Write Data” instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. The first figure below shows an example of writing three bytes of data using the write commands. This demonstrates that the “Write Burst Data” command is the most efficient method for writing data to sequential address locations. Figure 6.8 Example of Reading Three Data Bytes Using the SPI Read Commands on page 52 provides a similar comparison for reading data with the read commands. Note that there is no burst read, only read increment.

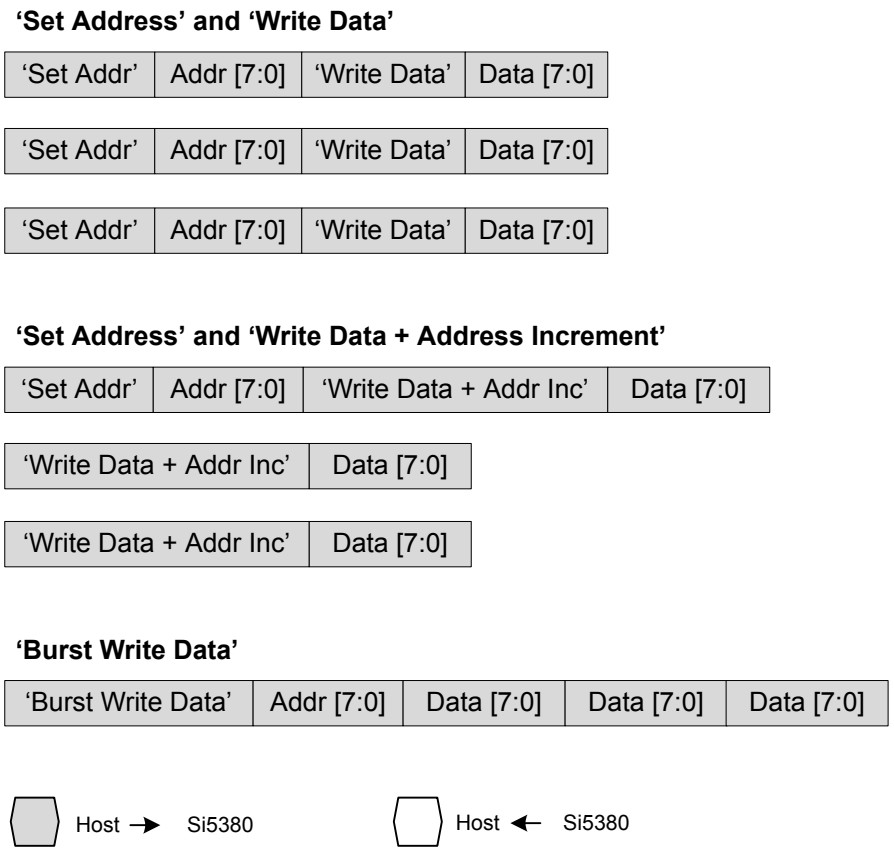


Figure 6.7. Example Writing Three Data Bytes Using the SPI Write Commands

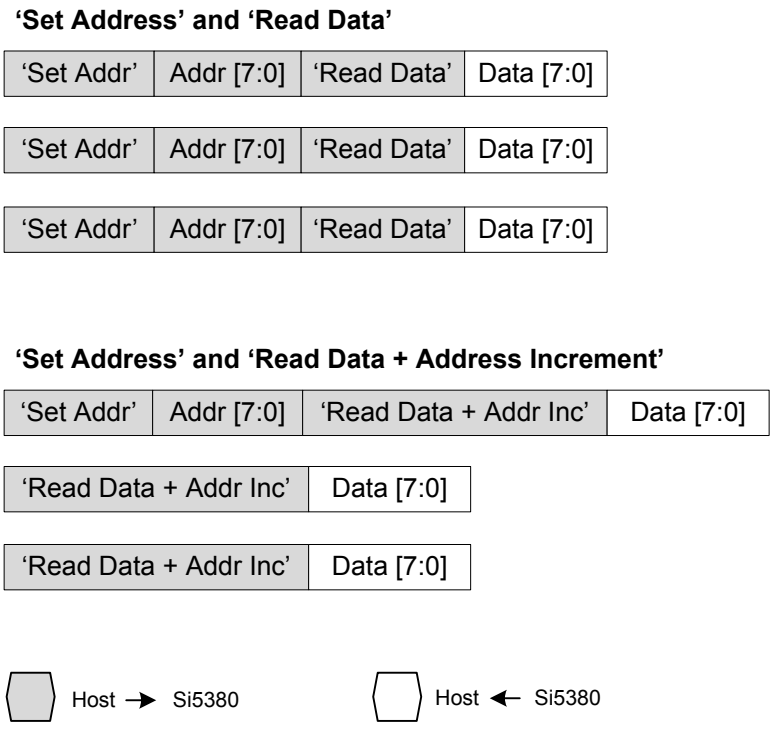


Figure 6.8. Example of Reading Three Data Bytes Using the SPI Read Commands

The timing diagrams for the SPI commands are shown in the following figures.

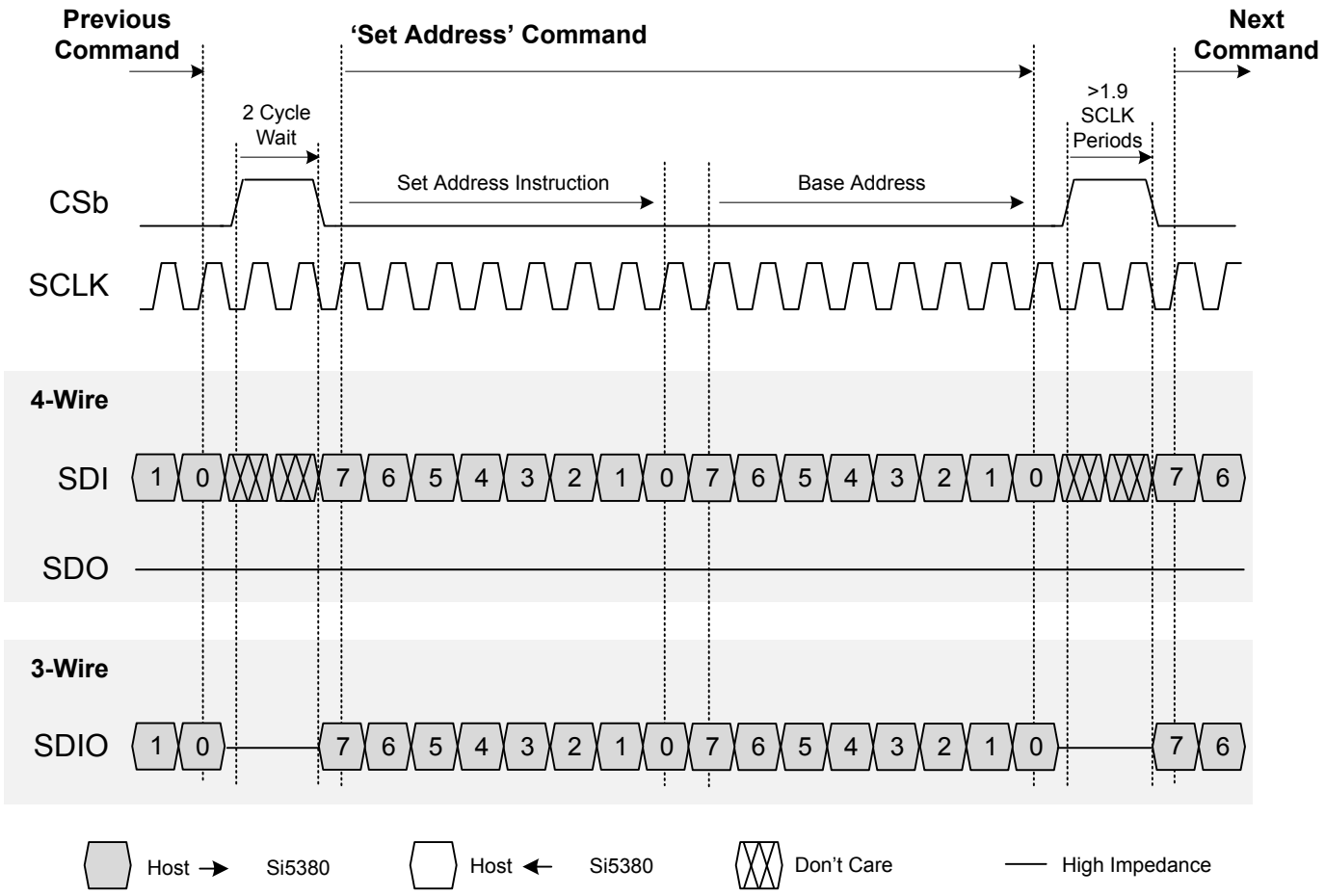


Figure 6.9. SPI "Set Address" Command Timing

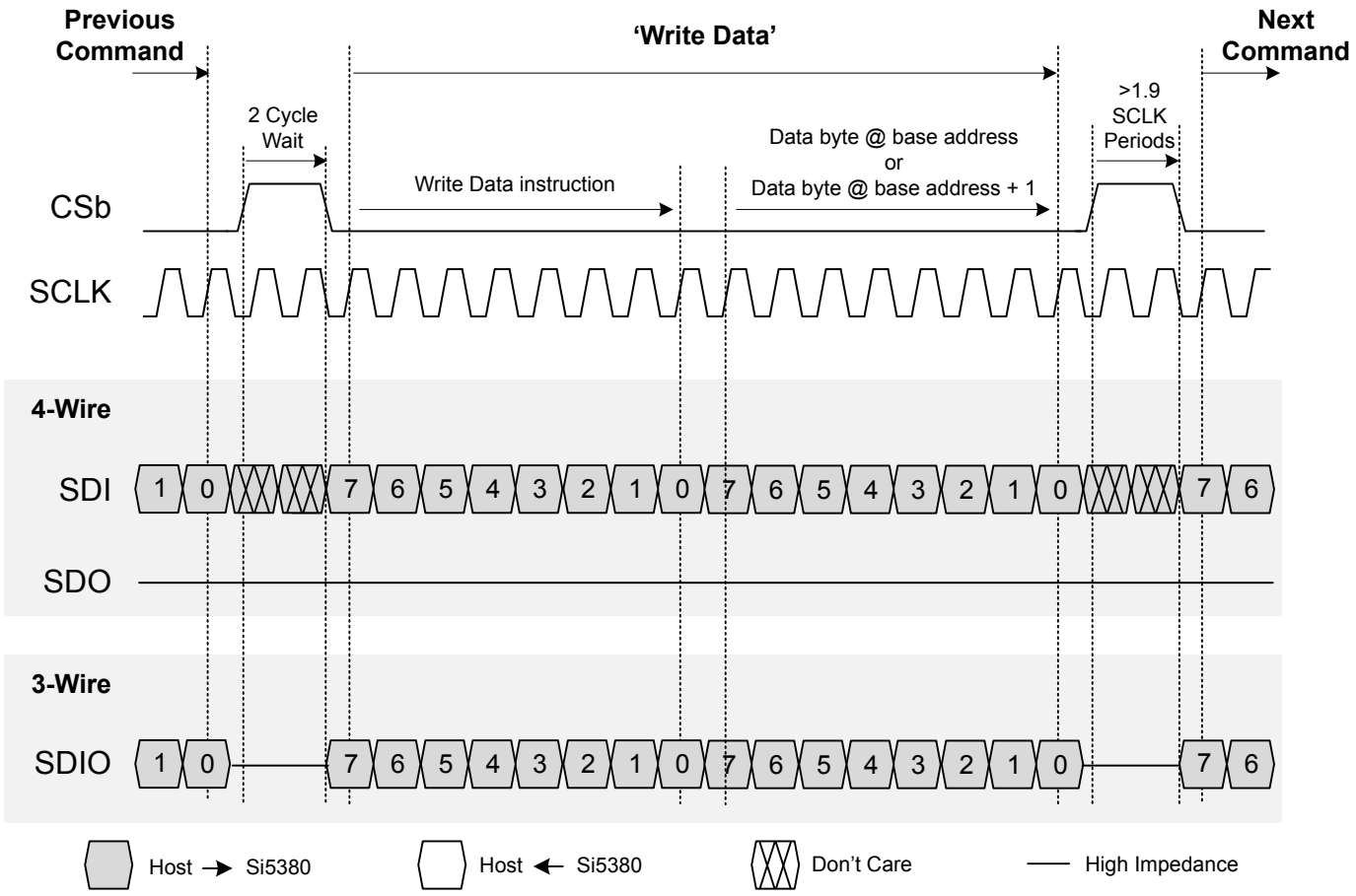


Figure 6.10. SPI "Write Data" and "Write Data + Address Increment" Instruction Timing

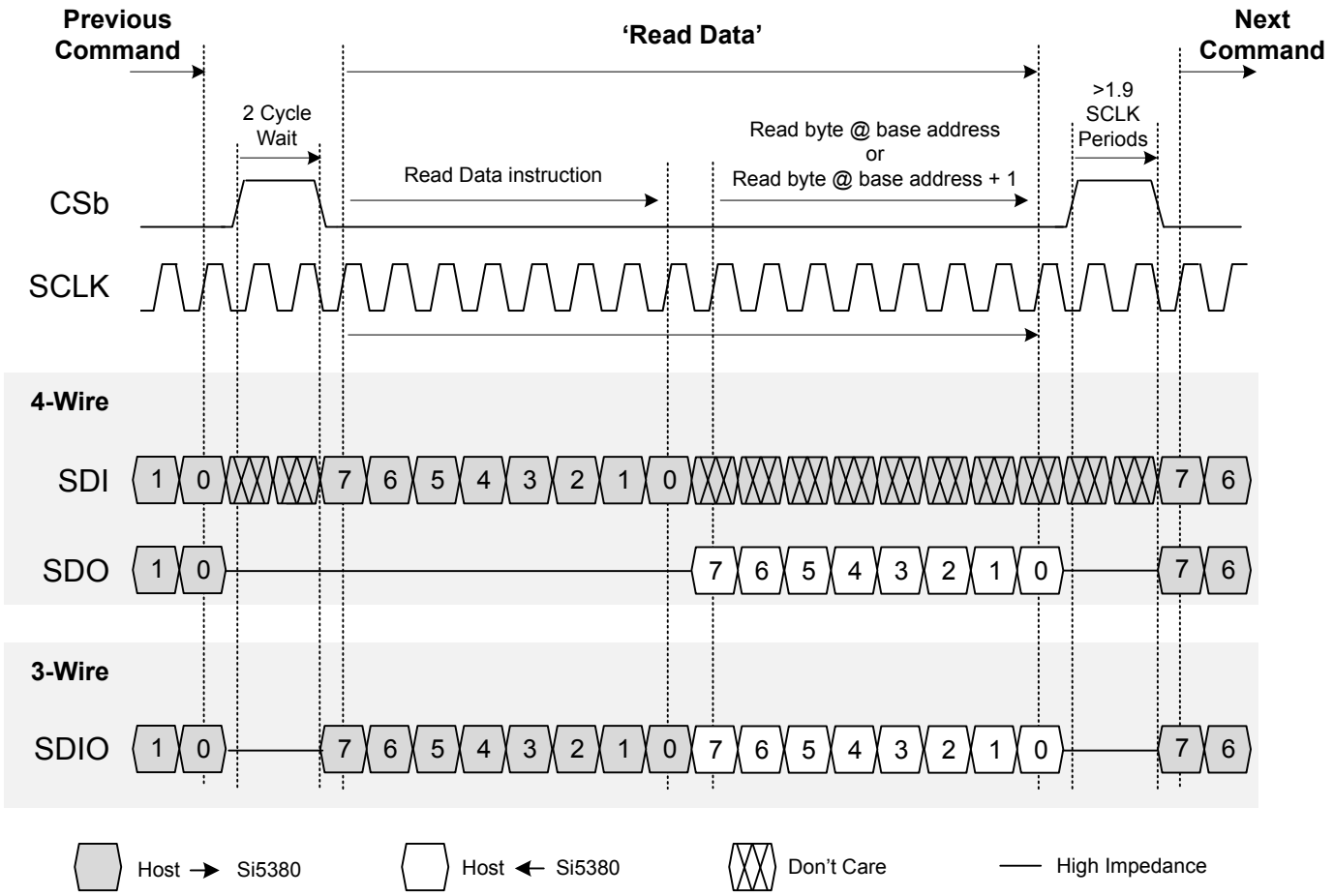


Figure 6.11. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

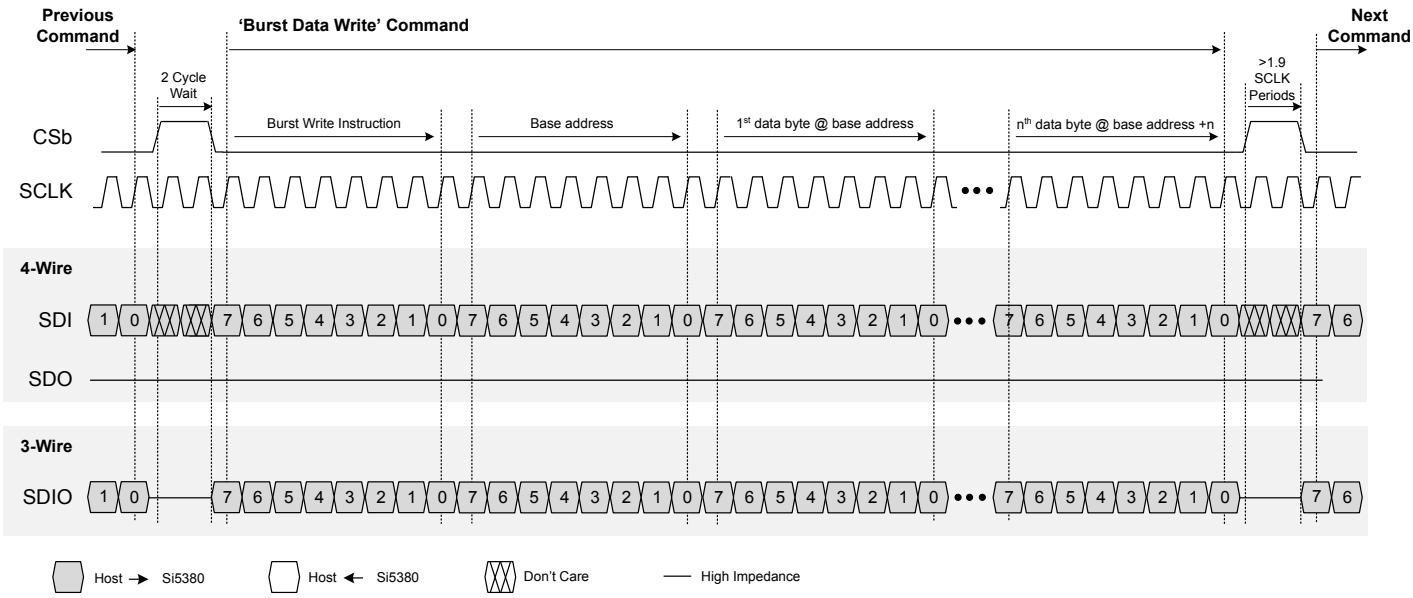


Figure 6.12. SPI "Burst Data Write" Instruction Timing

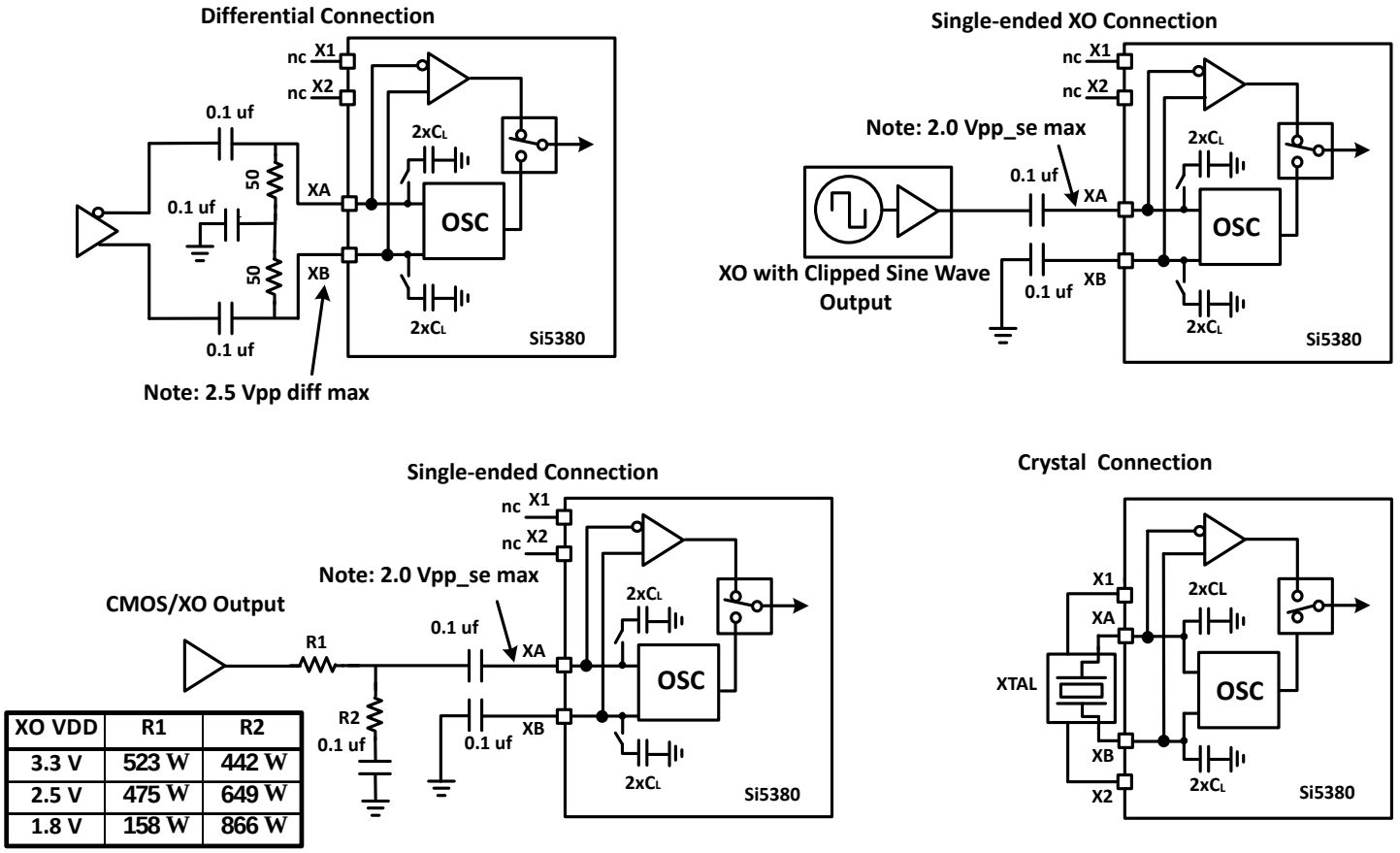
7. Field Programming

To simplify design and software development of systems using the Si5380, a field programmer is available. The ClockBuilder Pro Field Programmer supports both “in-system” programming for devices already mounted on a PCB, as well as “in-socket” programming of Si5380 sample devices. Refer to http://www.silabs.com/CBProgrammer for information about this kit.

8. XAXB External References

8.1 Performance of External References

An external standard non-pullable crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low phase noise reference clock for the DSPLL, as well as providing a stable reference for the Freerun and Holdover modes. Simplified connection diagrams are shown below. The device includes internal 8 pF crystal loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. The recommended crystal suppliers are listed in Table 8.1 Recommended Crystals on page 58 with crystal PCB layout recommendations in 9.1 Si5380 Crystal Layout Guidelines



XO VDD	R1	R2
3.3 V	523 W	442 W
2.5 V	475 W	649 W
1.8 V	158 W	866 W

Figure 8.1. XAXB Crystal Resonator and External Reference Clock Connection Options

In addition to crystal operations, the Si5380 accepts a Clipped Sine wave, CMOS, or Differential reference clock on the XAXB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 50 W or 100 W load. For this reason, place the TCXO as close to the Si5380 as possible to minimize PCB trace length. In addition, connect both the Si5380 and the TCXO directly to the same ground plane. The figure above shows the recommended method of connecting a clipped sine wave TCXO to the Si5380. Because the Si5380 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into XA after ac-coupling. Single-ended inputs must be connected to the XA pin with proper termination on the XB pin. Because the signal is single-ended in this case, the XB input is ac-coupled to ground. The figure above also illustrates the recommended method of connecting a single-ended CMOS rail-to-rail output to the XAXB inputs of the Si5380. The resistor network attenuates the swing to ensure that the maximum input voltage swing at the XA pin remains below the datasheet specification. The signal is ac-coupled before connecting it to the Si5380 XA input. For applications with loop BW values less than 10 Hz that require low wander output clocks, using a TCXO as the XAXB reference source should be considered to avoid the wander of a crystal.

8.2 Recommended Crystals

The table below lists the presently recommended 54 MHz crystals for the Si5380. See the “Crystal Specifications” table in the Si5380 Datasheet for detailed crystal specifications and requirements. Other vendors can also supply crystals that meet the datasheet specifications and those shown in the figure below.

Table 8.1. Recommended Crystals

Supplier	Part Number	Frequency (MHz)	Initial Accuracy (±ppm)	Accuracy over -40 °C to +85 °C (±ppm)	C0 Max (pF)	ESR Max (W)	CL (pF)	Drive Level (µW)	Case Size (mm x mm)
Connor Winfield	CS-044	54	15	25	2	20	8	200	3.2 x 2.5
Hosonic	E3S54.000F08M22SI	54	20	20	2	22	8	200	3.2 x 2.5
Hosonic	E3S54.000F08M22SI	54	20	20	1.5	25	8	200	3.2 x 2.0
Kyocera	CX3225SB54000D0WPJC1	54	10	15	2	23	8	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPJC2	54	10	15	2	23	8	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPTC1	54	30	60	2	23	8	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPSC1	54	15	30	2	23	8	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPSC2	54	15	30	2	23	8	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPSC3	54	50	50	2	15	8	200	3.2 x 2.5
NDK	NX3225SA-54.000M-CS07551	54	15	30	1.8	23	8	200	3.2 x 2.5
Siward	XTL571500-S315-006	54	50	50	2	20	8	200	3.2 x 2.5
Siward	XTL571500-S315-007	54	50	50	2	20	8	200	3.2 x 2.0
Taitien	S0242-X-001-3	54	20	20	2	23	8	200	3.2 x 2.5
TXC	7M54070010	54	10	15	2	22	8	200	3.2 x 2.5
TXC	7M54072001	54	20	30	2	22	8	200	3.2 x 2.5
TXC	7M54072002	54	10	15	2	22	8	200	3.2 x 2.5

Supplier	Part Number	Frequency (MHz)	Initial Accuracy (±ppm)	Accuracy over -40 °C to +85 °C (±ppm)	C0 Max (pF)	ESR Max (W)	CL (pF)	Drive Level (µW)	Case Size (mm x mm)
TXC	7M54072003	54	10	15	2	15	8	200	3.2 x 2.5

In normal operation, a crystal meeting the datasheet specifications, including operating power of at least 200 µW, and meeting the requirements of the figure below is guaranteed to oscillate. In general, lower-ESR crystals produce improved phase noise at low frequency offsets, <1kHz, than do higher-ESR crystals.

Some applications may require crystals that have been tested incrementally over the entire temperature range to ensure that the change in crystal resonant frequency over any 2 °C temperature difference is bounded. This is called “testing for activity dips” and adds cost to the crystal. The Si5380 is designed to work with both normally tested crystals as well as activity-dip-tested crystals.

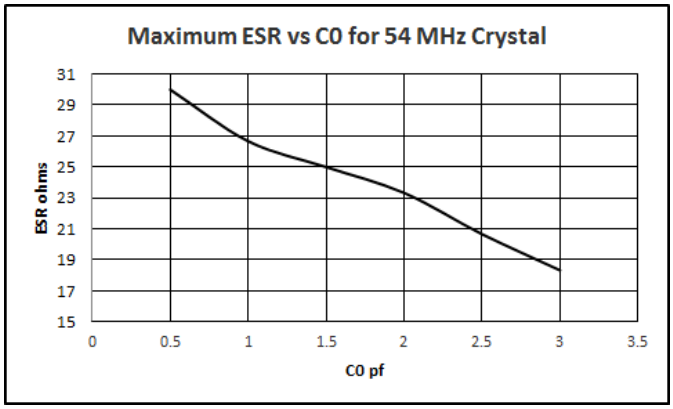


Figure 8.2. Maximum ESR vs. C0 for 54 MHz Crystal

8.3 Recommended External Oscillators

The table below lists recommended TCXO/OCXO suppliers. Other vendors can also supply TCXOs and OCXOs which meet the requirements for the Si5380. In general, using an external crystal with the internal oscillator will yield better phase noise results than using an external XO.

Table 8.2. Recommended Oscillators

Supplier	Part Number	Type	Frequency (MHz)	Case Size (mm x mm)
TXC	8W54072001-54M00	TCXO	54	2.5 x 2.0

When an external oscillator is used as the XAXB reference, it is important to use a low jitter source because there is essentially no jitter attenuation from the XAXB pins to the outputs.

8.4 XAXB Control Register Settings

The following registers can be used to control and make adjustments for the external reference source used.

8.4.1 XAXB_EXTCLK_EN Reference Clock Selection Register

Table 8.3. XAXB External Clock Selection Register

Register Name	Hex Address [Bit Field]	Function
XAXB_EXTCLK_EN	090E[0]	This bit selects between the Crystal or External reference clock on the XAXB pins. 0: Crystal on XAXB, enable internal XO (default) 1: External XAXB signal, internal XO disabled

9. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered for optimum phase noise include the following:

- Number and size of the ground vias for the Epad (see 10.4 Grounding Vias)
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace coupling
- Xtal signal coupling
- Xtal layout (see 9.1 Si5380 Crystal Layout Guidelinesbelow for important crystal layout guidelines)

If the application uses a crystal for the XAXB inputs, a shield should be placed underneath the crystal connected to the X1 and X2 pins (7 and 10) to provide the best possible performance. The shield should not be connected to the ground plane and the planes underneath should overlap under the shield as little as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

Go to http://www.silabs.com/Si538x-4x-EVB to obtain Si5380-EVB schematics, layouts, and component BOM files.

9.1 Si5380 Crystal Layout Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XAXB pins.
2. **DO NOT** connect the crystal's GND pins to the PCB gnd.
3. Connect the crystal's "GND" pins to the devices X1 and X2 pins via a local crystal shield placed around and under the crystal. See the bottom right diagram of Figure 9.1 Si5380 Device and Crystal Layout Recommendations, Top Layer (Layer 1) on page 62for an illustration of how to connect the crystal shield by placing vias connecting the top layer traces to the shield layer underneath. The second layer of the ground shield is shown in Figure 9.2 Input Clocks and Crystal Shield Layer, Below the Top Layer (Layer 2) on page 63.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequent toggling digital signals, such as serial interface lines.
5. In general, do not route GND, power planes/traces, or locate components on the other side of the PCB, below the crystal GND shield. As an exception, if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or on a layer at least 50 mils (0.05") away. The crystal should have all layers underneath the ground shield removed.

9.2 64-Pin QFN Si5380 Layout Recommendations

This section details the recommended guidelines for the crystal layout of the 64-pin Si5380 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: crystal shield
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: power routing layer
- Layer 6: ground input clocks, ground flooded
- Layer 7: output clocks layer
- Layer 8: ground layer

The figure below shows the top layer layout of the Si5380 device mounted on EVB. The crystal/oscillator is outlined with the white box around it. In this case, the top layer is flooded with ground. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. Note that this layout has a resistor in series with each pin of the crystal. In dedicated applications, these resistors would be removed. Notice the 5x5 array of thermal vias in the center of the device. See 10.4 Grounding Vias for more information on thermal/ground via layout.

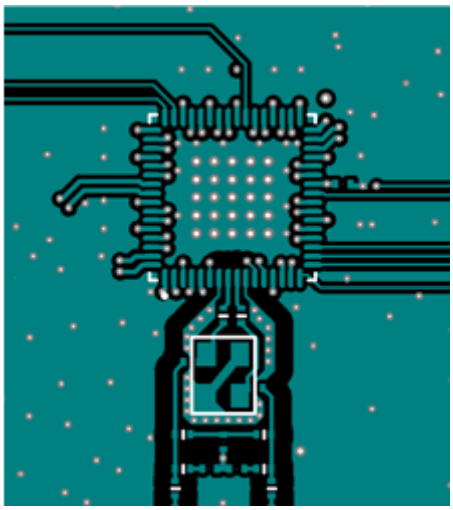


Figure 9.1. Si5380 Device and Crystal Layout Recommendations, Top Layer (Layer 1)

The following figure shows the layer that implements the shield underneath the crystal. The shield is separated from the surrounding ground plane and extends underneath the entire crystal to the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2, they have a ground shield above, below, and on the sides for maximum protection.

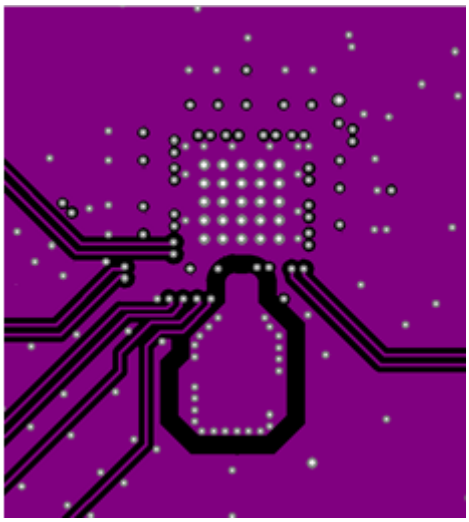


Figure 9.2. Input Clocks and Crystal Shield Layer, Below the Top Layer (Layer 2)

The figure below is the ground plane and shows a void underneath the crystal shield. Figure 9.4 Internal Power Plane (Layer 4) on page 64 is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued to the internal layers of the PCB.

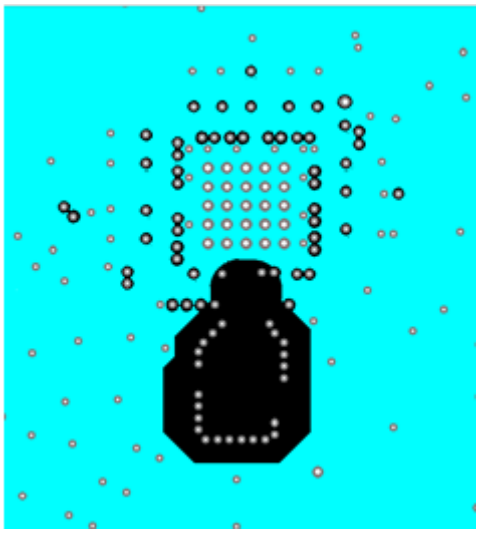


Figure 9.3. Internal Ground Plane (Layer 3)

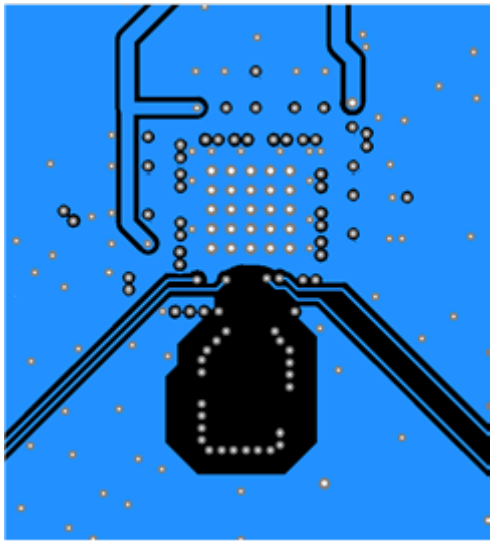


Figure 9.4. Internal Power Plane (Layer 4)

The figure below shows layer 5, which is the power plane routed to the clock output power pins.

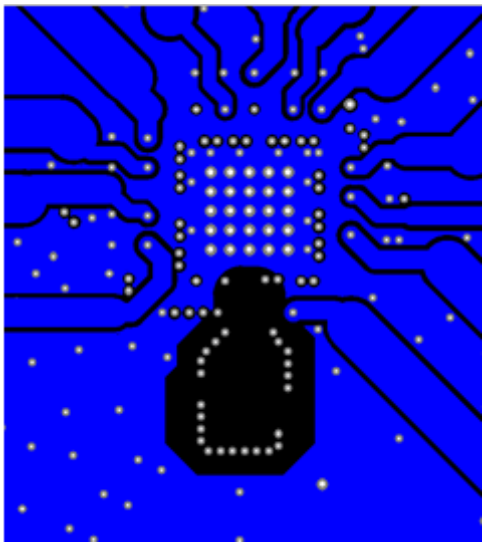


Figure 9.5. Internal Power Plane (Layer 5)

The figure below shows layer 6, another ground plane similar to layer 3.

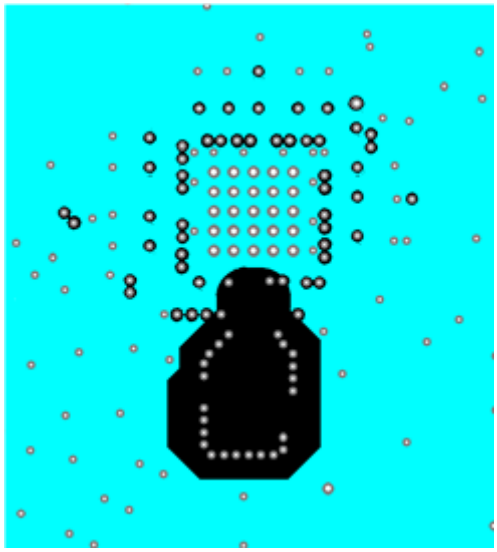


Figure 9.6. Internal Ground Plane (Layer 6)

The figure below shows the output clocks. Similar to the input clocks, the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is ground flooding between the clock output pairs to reduce crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

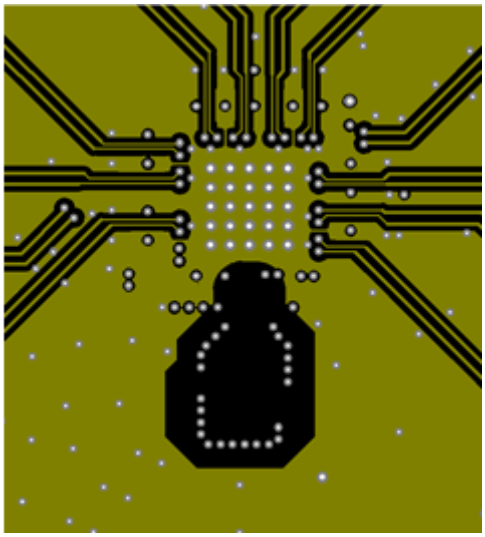


Figure 9.7. Output Clocks (Layer 7)

The bottom layer shown in the figure below displays the location of the decoupling capacitors close to the device.

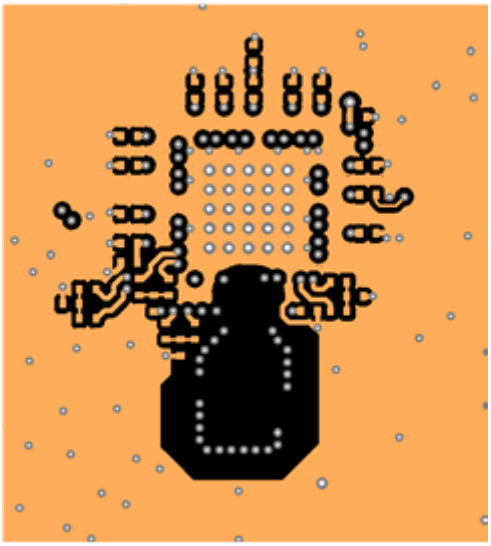


Figure 9.8. Bottom Layer Ground Flooded (Layer 8)

10. Power Management

10.1 Power Management Features

A number of unused functions can be powered down to minimize power consumption. The registers listed in the table below are used for powering down different features of the device.

Table 10.1. Powerdown Registers

Register Name	Hex Address [Bit Field]	Function
PDN	0x001E[0]	Place the device into a low current Power-down state. Note that the serial interface and registers remain active in this state. 0: Normal Operation (default) 1: Powerdown Device
OUT0A_PDN OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN OUT4_PDN OUT5_PDN OUT6_PDN OUT7_PDN OUT8_PDN OUT9_PDN OUT9A_PDN	0x0103[0] 0x0108[0] 0x010D[0] 0x0112[0] 0x0117[0] 0x011C[0] 0x0121[0] 0x0126[0] 0x012B[0] 0x0130[0] 0x0135[0] 0x013A[0]	Powers down unused output drivers. 0: Power-up output driver (default) 1: Powerdown output driver
OUT_PDN_ALL	0x0145[0]	Powers down all output drivers. 0: Normal Operation (default) 1: Powerdown All output drivers
XAXB_XO_EN	0x090E[1]	Powers down the built-in low noise crystal oscillator when using an external reference input. 0: Powerdown Internal Oscillator 1: Internal Oscillator Powered (default) - required when using a crystal with the XAXB oscillator.
IN_EN	0x0949[3:0]	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer

10.2 Power Supply Recommendations

Power supply filtering is generally important for optimal timing performance. The Si5380 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will minimize signal degradation from power supply noise.

It is recommended to use a 0402-size 1 mF ceramic capacitor on each power supply pin for optimal performance. If the supply voltage is extremely noisy, it might require a ferrite bead in series between the voltage supply voltage and the device power supply pin.

10.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5380:

1. VDD=1.8V (Core digital supply)
2. VDDA=3.3V (Analog supply)
3. VDDO=1.8/2.5/3.3V (Output Clock supplies)

There is no general requirement for power supply sequencing on this device unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting Hard Reset 0x001E[1] register bits or driving the RSTb pin. Note that using a Hard Reset will reload the register with the contents of the NVM and any unsaved register changes will be lost.

10.4 Grounding Vias

The "Epad" on the bottom of the device functions as both the sole electrical ground and as the primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

11. Base vs. Factory Preprogrammed Devices

The Si5380 devices can be ordered as "base" or "factory-preprogrammed" (also known as "custom OPN") versions.

11.1 "Base" Devices (a.k.a. "Blank" Devices)

- Example "base" orderable part numbers (OPNs) are of the form "Si5380A-B-GM."
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 48 MHz crystal on the XAXB reference and a 1.8 V compatible I/O voltage setting for the host I^2C/SPI interface.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the on-line lookup utility at www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx to access the default configuration plan and register settings for any base OPN.

11.2 "Factory Preprogrammed" (Custom OPN) Devices

- Factory preprogammed devices use a “custom OPN”, such as Si5380A-Axxxxx-GM, where “xxxxx” is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx
- Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both "base" and "factory preprogrammed" devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see 2.2 NVM Programming).

11.3 Part Numbering Summary

Part numbers are of the form:

Si<Part Num Type><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

For example:

- **Si5380A-B12345-GM:** Applies to a factory preprogrammed OPN (Ordering Part Number) device. These devices are programmed at the factory with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.
- **Si5380A-B-GM:** Applies to a "base" device. Base devices are factory programmed to a specific base part type (e.g., Si5380) but **exclude** any user-defined frequency plan or other operating characteristics which would be selected in ClockBuilder Pro.

12. Register Map

12.1 Page 0 Registers Si5380

Table 12.1. Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Default	Description
0x0000	3:0	R	DIE_REV	0	4-bit die revision number

Table 12.2. Register 0x0001 Page

Reg Address	Bit Field	Type	Name	Default	Description
0x0001	7:0	R/W	PAGE	0	Select one of 256 possible pages.

This is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 12.3. Register 0x0002-0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Default	Description
0x0002	7:0	R	PN_BASE	0x45	Four-digit ,"base" part number, one nibble per digit. Example: Si53280A-A0GM. The base part number (OPN) is 5380, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

See 11.3 Part Numbering Summary for more information on part numbers.

Table 12.4. Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed grade. For example Si5380A-B12345-GM: 1 = A

See 11.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 12.5. Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B; 2 = C, etc. For example: Si5380A-B12345-GM, the device revision is B

See 11.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 12.6. Register 0x0006-0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R	TOOL_VERSION[3:0]	Special
0x0006	7:4	R	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R	TOOL_VERSION[16]	Minor[8]
0x0008	4:1	R	TOOL_VERSION[20:17]	Major
0x0008	7:5	R	TOOL_VERSION[23:21]	Tool

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 12.7. Register 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grade: 0: Industrial (-40 to 85 °C

See 11.3 Part Numbering Summary for more information on part numbers.

Table 12.8. Register 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R	PKG_ID	Package Identifier: 0: 9x9 mm 64 QFN

See 11.3 Part Numbering Summary for more information on part numbers.

Table 12.9. Register 0x000B I2C Address

Reg Address	Bit Field	Type	Name	Description
0x000B	6:0	R	I2C_ADDR	7-bit I2C Address

Note that the 2 least significant bits, [1:0], are determined by the voltages on the A1 and A0 input pins respectively.

Table 12.10. Register 0x000C Device Status

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is currently calibrating.
0x000C	1	R	LOSXAXB	1 if there is currently no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if there is currently no signal detected on the XAXB input signal.
0x000C	3	R	XAXB_ERR	1 if there is currently a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is currently an SMB Bus Timeout error.

See 3.3 Fault Monitoring for more information.

Table 12.11. Register 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Status

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if IN3 - IN0 is currently LOS
0x000D	7:4	R	OOF	1 if IN3 - IN0 is currently OOF

See 3.3 Fault Monitoring for more information.

- IN0: LOS 0x000D[0], OOF 0x000D[4]
- IN1: LOS 0x000D[1], OOF 0x000D[5]
- IN2: LOS 0x000D[2], OOF 0x000D[6]
- IN3/FB_IN: LOS 0x000D[3], OOF 0x000D[7]

Table 12.12. Register 0x000E Holdover (HOLD) and Loss-of-Lock (LOL) Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is currently out of lock
0x000E	5	R	HOLD	1 if the DSPLL is currently in Hold-over or Freerun

See 3.3 Fault Monitoring for more information.

Table 12.13. Register 0x000F DSPLL Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL	1 if the DSPLL internal calibration is currently busy

See 3.3 Fault Monitoring for more information.

Table 12.14. Register 0x0011 Device Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Flag 1 if the device was in SYSINCAL
0x0011	1	R/W	LOSXAXB_FLG	Flag 1 if the XAXB input showed LOSXAXB
0x0011	2	R/W	LOSREF_FLG	Flag 1 if the XAXB input LOSREF
0x0011	3	R/W	XAXB_ERR_FLG	Flag 1 if the XAXB input showed XAXB_ERR
0x0011	5	R/W	SMB_TMOUT_FLG	Flag 1 if SMB_TMOUT was in error

These are sticky flag bits corresponding to the bits in register 0x000C. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000C register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 12.15. Register 0x0012 OOF and LOS Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	Flag 1 if IN3 - IN0 was or is LOS

Reg Address	Bit Field	Type	Name	Description
0x0012	7:4	R/W	OOF_FLG	Flag 1 if IN3 - IN0 was or is OOF

These are sticky flag bits corresponding to the bits in register 0x000D. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000D register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

- IN0: LOS_FLG 0x0012[0], OOF_FLG 0x0012[4]
- IN1: LOS_FLG 0x0012[1], OOF_FLG 0x0012[5]
- IN2: LOS_FLG 0x0012[2], OOF_FLG 0x0012[6]
- IN3/FB_IN: LOS_FLG 0x0012[3], OOF_FLG 0x0012[7]

Table 12.16. Register 0x0013 HOLD and LOL Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	Flag 1 if the DSPLL was or is LOL
0x0013	5	R/W	HOLD_FLG	Flag 1 if the DSPLL was or is in Holdover or Freerun

These are sticky flag bits corresponding to the bits in register 0x000E. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000E register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 12.17. Register 0x0014 DSPLL Calibration Status Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG	Flag 1 if the internal calibration was or is busy

These are sticky flag bits corresponding to the bits in register 0x000F. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000F register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 12.18. Register 0x0017 Device Status Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOSREF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	XAXB_ERR_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0017	5	R/W	SMBUS_IMOUT_FLG_MSK	1 to mask SMBUS_TMOUT_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0011. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 12.19. Register 0x0018 OOF and LOS Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask LOS_FLG from causing an interrupt

Reg Address	Bit Field	Type	Name	Description
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask OOF_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0012. See 3.3.6 INTRb Interrupt Configuration for more information.

- IN0: LOS_INTR_MSK 0x0018[0], OOF_INTR_MSK 0x0018[4]
- IN1: LOS_INTR_MSK 0x0018[1], OOF_INTR_MSK 0x0018[5]
- IN2: LOS_INTR_MSK 0x0018[2], OOF_INTR_MSK 0x0018[6]
- IN3/FB_IN: LOS_INTR_MSK 0x0018[3], OOF_INTR_MSK 0x0018[7]

Table 12.20. Register 0x0019 HOLD and LOL Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask HOLD_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0013. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 12.21. Register 0x001A PLL In Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_INTR_MSK	1 to mask CAL_PLL_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0014. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 12.22. Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Initialize and calibrates the entire device 0 No effect

Soft Reset restarts the device using the existing register values without loading from NVM. Soft Reset also updates registers requiring a separate update strobe, including the DSPLL bandwidth registers as well as the P, M, N, and R dividers.

Table 12.23. Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	Place the device into a low current Powerdown state. Note that the serial interface and registers remain active in this state. 0: Normal Operation (default) 1: Powerdown Device

Reg Address	Bit Field	Type	Name	Description
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Resets all R dividers. Logically equivalent to asserting the SYNCb pin. 0: Normal Operation 1: Reset R Dividers

Table 12.24. Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	Selects between Pin and Register control for output disable. 0: OEb Pin disable (default) 1: OE Register disable
0x0022	1	R/W	OE_REG_DIS	When OE_REG_SEL = 1: 0: Disable selected outputs 1: Enable selected outputs

By default ClockBuilder Pro sets the OEb pin controlling all outputs. OUTALL_DISABLE_LOW (0x0102[0]) must be high (enabled) to allow the OEb pin to enable outputs. Note that the OE_REG_DIS bit (active high) has inverted logic sense from the OEb pin (active low). See 4.6.5 Output Driver Disable Source Summary for more information.

Table 12.25. Register 0x0023-0x0024 OE0 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0023	0	R/W	OE_OUT0A_SEL	Selects whether each output driver is affected by the OEb pin or OE_REG_DIS. 0: Output Ignores OEb and OE_REG_DIS 1: Output Disabled by OEb/ OE_REG_DIS
	1		OE_OUT0_SEL	
	2		OE_OUT1_SEL	
	3		OE_OUT2_SEL	
	4		OE_OUT3_SEL	
	5		OE_OUT4_SEL	
	6		OE_OUT5_SEL	
	7		OE_OUT6_SEL	
0x0024	0	R/W	OE_OUT7_SEL	
	1		OE_OUT8_SEL	
	2		OE_OUT9_SEL	
	3		OE_OUT9A_SEL	

By default ClockBuilder Pro sets the OEb pin controlling all outputs. OUTALL_DISABLE_LOW (0x0102[0]) must be high (enabled) to allow the OEb pin to enable outputs. See 4.6.5 Output Driver Disable Source Summary for more information.

Table 12.26. Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	Selects operating mode for SPI interface: 0: 4-wire SPI 1: 3-wire SPI

This bit is ignored for I2C bus operation, when I2C_SEL is high.

Table 12.27. Register 0x002C LOS Enables

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	Enable LOS detection on IN3 - IN0. 0: Disable LOS Detection 1: Enable LOS Detection

- IN0: LOS_EN[0]
- IN1: LOS_EN[1]
- IN2: LOS_EN[2]
- IN3/FB_IN: LOS_EN[3]

Table 12.28. Register 0x002D LOS Clear Delays

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	IN0 LOS Clear delay. 0: 2 ms 1: 100 ms 2: 200 ms 3: 1000 ms
0x002D	3:2	R/W	LOS1_VAL_TIME	IN1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	IN2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	IN3/FB_IN, same as above

When a valid input clock is not present on the input, LOS will be asserted. When the clock returns, it must remain valid for this period of time before that clock is considered to be qualified again.

Table 12.29. Register 0x002E-0x002F IN0 LOS Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit LOS Trigger Threshold value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for IN0, given a particular frequency plan.

Table 12.30. Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit LOS Clear Threshold value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for IN0, given a particular frequency plan.

All 4 input buffers are identical in terms of control. The single set of descriptions for IN0 above also apply to IN1-IN3.

Table 12.31. Output Registers Following the Same Definitions as IN0

Register Addresses	Description	(Same as) Addresses
0x0030 - 0x0031	IN1 LOS Trigger Threshold	0x002E - 0x002F
0x0038 - 0x0039	IN1 LOS Clear Threshold	0x002E - 0x002F
0x0032 - 0x0033	IN2 LOS Trigger Threshold	0x002E - 0x002F
0x003A - 0x003B	IN2 LOS Clear Threshold	0x002E - 0x002F
0x0034 - 0x0035	IN3/FB_IN LOS Trigger Threshold	0x002E - 0x002F
0x003C - 0x003D	IN3/FB_IN LOS Clear Threshold	0x002E - 0x002F

Table 12.32. Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	Enable Precision OOF for IN3 - IN0 0: Disable Precision OOF 1: Enable Precision OOF
0x003F	7:4	R/W	FAST_OOF_EN	Enable Fast OOF for IN3 - IN0 0: Disable Fast OOF 1: Enable Fast OOF

- IN0: OOF_EN[0], FAST_OOF_EN[4]
- IN1: OOF_EN[1], FAST_OOF_EN[5]
- IN2: OOF_EN[2], FAST_OOF_EN[6]
- IN3/FB_IN: OOF_EN[3], FAST_OOF_EN[7]

Table 12.33. Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	Select reference 0ppm 0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5-7: Reserved

Table 12.34. Register 0x0046-0x0049 Precision OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	Precision OOF Set Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Set Threshold (ppm) = OOFx_SET_THR x 2 ppm OOF will be indicated if this is set to 0.
0x0047	7:0	R/W	OOF1_SET_THR	
0x0048	7:0	R/W	OOF2_SET_THR	
0x0049	7:0	R/W	OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 12.35. Register 0x004A-0x004D Precision OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	Precision OOF Clear Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Clear Threshold (ppm) = OOFx_CLR_THR x ±2 ppm Note that OOF will be indicated if this is set to 0.
0x004B	7:0	R/W	OOF1_CLR_THR	
0x004C	7:0	R/W	OOF2_CLR_THR	
0x004D	7:0	R/W	OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 12.36. Register 0x0051-0x0054 Fast OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	Fast OOF Set Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Set Threshold (ppm) = (FAST_OOFx_SET_THR + 1) x ±1000 ppm Note that OOF will be indicated if this is set to 0.
0x0052	7:0	R/W	FAST_OOF1_SET_THR	
0x0053	7:0	R/W	FAST_OOF2_SET_THR	
0x0054	7:0	R/W	FAST_OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 12.37. Register 0x0055-0x0058 Fast OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	Fast OOF Clear Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Clear Threshold (ppm) = (FAST_OOFx_CLR_THR + 1) * ±1000ppm Note that OOF will be indicated if this is set to 0.
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	
0x0057	7:0	R/W	FAST_OOF2_CLR_THR	
0x0058	7:0	R/W	FAST_OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 12.38. Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLOW_EN_PLL	Enable LOL detection. 0: LOL Disabled 1: LOL Enabled

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 12.39. Register 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SLW_SET_THR	LOL Set Threshold. See the list below for settings.

Table 12.40. Register 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_SLW_CLR_THR	LOL Clear Threshold. See the list below for settings.

LOL_SET_THR and LOL_CLR_THR Threshold settings:

- 0 = 0.1 ppm
- 1 = 0.3 ppm
- 2 = 1 ppm
- 3 = 3 ppm
- 4 = 10 ppm
- 5 = 30 ppm
- 6 = 100 ppm
- 7 = 300 ppm
- 8 = 1000 ppm
- 9 = 3000 ppm
- 10 = 10000 ppm
- 11 - 15 Reserved

Table 12.41. Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	Enable Delay for LOL Clear. 0: Disable Delay for LOL Clear 1: Enable Delay for LOL Clear

Extends the time after a clock returns or stabilizes before LOL de-asserts.

Table 12.42. Register 0x00A8-0x00AC LOL Clear Delay

Reg Address	Bit Field	Type	Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY	35-bit value
0x00A9	15:8			
0x00AA	23:16			
0x00AB	31:24			
0x00AC	34:32			

The LOL Clear Delay value is set by ClockBuilder Pro based on each frequency plan.

Table 12.43. Register 0x00E2 NVM Active Bank

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned hen ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See 2.2 NVM Programming for a detailed description of how to program the NVM.

Table 12.44. Register 0x00E3

Reg Address	Bit Field	Type	Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 2.2 NVM Programming.

Table 12.45. Register 0x00E4

Reg Address	Bit Field	Type	Name	Description
0x00E4	0	S	NVM_READ_BANK	Set to 1 to initiate NVM copy to registers.

Table 12.46. Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Device Ready indicator. 0x0F: Device is Ready 0xF3: Device is Not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-up. When reads from DEVICE_READY return 0x0F the user can safely read or write to all registers. This is generally only needed after POR, after a Hard Reset by pin or register, or after initiating and NVM write. The “Device Ready” register is available on every page in the device at the second to the last serial address, 0xFE. There is a device ready register at 0x00FE, 0x01FE, 0x02FE, … etc.

12.2 Page 1 Registers

Table 12.47. Register 0x0102 Global Output Gating for all Clock Outputs

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	Enable/Disable All output drivers. If the OEb pin is held high, then all outputs will be disabled regardless of this setting. 0: Disable All outputs (default) 1: Enable All outputs

Table 12.48. Register 0x0103 OUT0A Output Enable and R0A Divider Configuration

Reg Address	Bit Field	Type	Name	Description
0x0103	0	R/W	OUT0A_PDN	Powerdown output driver. 0: Normal Operation (default) 1: Powerdown output driver
0x0103	1	R/W	OUT0A_OE	Enable/Disable individual output. 0: Disable output (default) 1: Enable output
0x0103	2	R/W	OUT0A_RDIV_FORCE	Force R0A output divider divide-by-2. 0: R0A_REG sets divide value (default) 1: Divide value forced to divide-by-2

Setting R0A_REG=0 will not set the divide value to divide-by-2 automatically. OUT0A_RDIV_FORCE must be set to a value of 1 to force R0A to divide-by-2. Note that the R0A_REG value will be ignored while OUT0A_RDIV_FORCE=1. Seee R0A-REG registers, 0x0247-0x0249, for more information.

Table 12.49. Register 0x0104 OUT0A Output Format and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0104	2:0	R/W	OUT0A_FORMAT	Select output format. 0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved

Reg Address	Bit Field	Type	Name	Description
0x0104	3	R/W	OUT0A_SYNC_EN	Synchronous Enable/ Disable selection. 0: Asynchronous Enable/ Disable (default) 1: Synchronous Enable/ Disable (Glitchless)
0x0104	5:4	R/W	OUT0A_DIS_STATE	Determines the logic state of the output driver when disabled: 0: Disable logic Low 1: Disable logic High 2-3: Reserved
0x0104	7:6	R/W	OUT0A_CMOS_DRV	LVCMOS output impedance selection. See Table 4.7 LVCMOS Output Impedance and Drive Strength Selections on page 37for valid selections.

Table 12.50. Register 0x0105 Output OUT0A Differential Amplitude and Common Mode

Reg Address	Bit Field	Type	Name	Description
0x0105	3:0	R/W	OUT0A_CM	OUT0A Common Mode Voltage selection. Only applies when OUT0A_FORMAT=1 or 2.
0x0105	6:4	R/W	OUT0A_AMPL	OUT0A Differential Amplitude setting. Only applies when OUT0A_FORMAT=1 or 2.

ClockBuilder Pro is used to select the correct settings for this register. See Table 4.6 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 35 and Appendix 1. Custom Differential Amplitude Controls for details of the settings.

Table 12.51. Register 0x0106 Output OUT0A Source Selection and LVCMOS Inversion

Reg Address	Bit Field	Type	Name	Description
0x0106	2:0	R/W	OUT0A_MUX_SEL	OUT0A output source divider select. 0: N0 is the source for OUT0A 1: N1 is the source for OUT0A 2: N2 is the source for OUT0A 3: N3 is the source for OUT0A 4: N4 is the source for OUT0A 5-7: Reserved
0x0106	7:6	R/W	OUT0A_INV	OUT0A output LVCMOS inversion. Only applies when OUT0A_FORMAT = 4. See Table 25, “LVCMOS Output Polarity Registers,” on page 42 for more information.

Each output can be independently configured to use one of the N0-N4 divider outputs as its source. The frequency for each N-divider is set in registers 0x0302-0x0337 for N0 to N4. Five different frequencies can be set in the N-dividers (N0-N4) and each of the 12 outputs can be configured to any of the five different frequencies.

All 12 output drivers are identical in terms of control. The single set of descriptions above for OUT0A also applies to OUT0-OUT9A:

Table 12.52. Output Registers Following the Same Definitions as OUT0A

Register Address	Description	(Same as) Address
0x0108	OUT0 Powerdown, Output Enable, and R0 Divide-by-2	0x0103
0x0109	OUT0 Signal Format and Configuration	0x0104
0x010A	OUT0 Differential Amplitude and Common Mode	0x0105
0x010B	OUT0 Source Selection and LVCMOS Inversion	0x0106
0x010D	OUT1 Powerdown, Output Enable, and R1 Divide-by-2	0x0103
0x010E	OUT1 Signal Format and Configuration	0x0104
0x010F	OUT1 Differential Amplitude and Common Mode	0x0105
0x0110	OUT1 Source Selection and LVCMOS Inversion	0x0106
0x0112	OUT2 Powerdown, Output Enable, and R2 Divide-by-2	0x0103

Register Address	Description	(Same as) Address
0x0113	OUT2 Signal Format and Configuration	0x0104
0x0114	OUT2 Differential Amplitude and Common Mode	0x0105
0x0115	OUT2 Source Selection and LVCMOS Inversion	0x0106
0x0117	OUT3 Powerdown, Output Enable, and R3 Divide-by-2	0x0103
0x0118	OUT3 Signal Format and Configuration	0x0104
0x0119	OUT3 Differential Amplitude and Common Mode	0x0105
0x011A	OUT3 Source Selection and LVCMOS Inversion	0x0106
0x011C	OUT4 Powerdown, Output Enable, and R4 Divide-by-2	0x0103
0x011D	OUT4 Signal Format and Configuration	0x0104
0x011E	OUT4 Differential Amplitude and Common Mode	0x0105
0x011F	OUT4 Source Selection and LVCMOS Inversion	0x0106
0x0121	OUT5 Powerdown, Output Enable, and R5 Divide-by-2	0x0103
0x0122	OUT5 Signal Format and Configuration	0x0104
0x0123	OUT5 Differential Amplitude and Common Mode	0x0105
0x0124	OUT5 Source Selection and LVCMOS Inversion	0x0106
0x0126	OUT6 Powerdown, Output Enable, and R6 Divide-by-2	0x0103
0x0127	OUT6 Signal Format and Configuration	0x0104
0x0128	OUT6 Differential Amplitude and Common Mode	0x0105
0x0129	OUT6 Source Selection and LVCMOS Inversion	0x0106
0x012B	OUT7 Powerdown, Output Enable, and R7 Divide-by-2	0x0103
0x012C	OUT7 Signal Format and Configuration	0x0104
0x012D	OUT7 Differential Amplitude and Common Mode	0x0105
0x012E	OUT7 Source Selection and LVCMOS Inversion	0x0106

Register Address	Description	(Same as) Address
0x0130	OUT8 Powerdown, Output Enable, and R8 Divide-by-2	0x0103
0x0131	OUT8 Signal Format and Configuration	0x0104
0x0132	OUT8 Differential Amplitude and Common Mode	0x0105
0x0133	OUT8 Source Selection and LVCMOS Inversion	0x0106
0x0135	OUT9 Powerdown, Output Enable, and R9 Divide-by-2	0x0103
0x0136	OUT9 Signal Format and Configuration	0x0104
0x0137	OUT9 Differential Amplitude and Common Mode	0x0105
0x0138	OUT9 Source Selection and LVCMOS Inversion	0x0106
0x013A	OUT9A Powerdown, Output Enable, and R9A Divide-by-2	0x0103
0x013B	OUT9A Signal Format and Configuration	0x0104
0x013C	OUT9A Differential Amplitude and Common Mode	0x0105
0x013D	OUT9A Source Selection and LVCMOS Inversion	0x0106

Table 12.53. Register 0x0141 Output Disable Mask for LOSXAXB

Reg Address	Bit Field	Type	Name	Description
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Mask LOSXAXB from disabling all output drivers. 0: Disable All output drivers on LOSXAXB (default) 1: Ignore LOSXAXB for output driver disable

See 4.6.5 Output Driver Disable Source Summaryfor more information.

Table 12.54. Register 0x0142 Output Disable Mask for LOL

Reg Address	Bit Field	Type	Name	Description
0x0142	1	R/W	OUT_DIS_MASK_LOL	Mask LOL from disabling all output drivers. 0: Disable All output drivers on LOL (default) 1: Ignore LOL for output driver disable

See 4.6.5 Output Driver Disable Source Summaryfor more information.

Table 12.55. Register 0x0145 Output Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	Powerdown all output drivers. 0: Normal Operation (default) 1: Powerdown all output drivers

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Table 12.56. Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8			
0x020A	23:16			
0x020B	31:24			
0x020C	39:32			
0x020D	47:40			

Table 12.57. Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8			
0x0210	23:16			
0x0211	31:24			

The P input divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. The new register values for the P divider will not take effect until the appropriate Px_UPDATE strobe is set as described below.
Note: This ratio of Px_NUM/Px_DEN should be an integer for proper operation of the device.

Table 12.58. Registers that Follow the P0_NUM and P0_DEN Above

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

Table 12.59. Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S	P0_UPDATE	Set these bits for IN3 - IN0 to 1 to latch in new P-divider values.
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

The Px_UPDATE bit must be asserted to update the internal P divider numerator and denominator values. These update bits are provided so that all of the P input dividers can be changed at the same time.

Table 12.60. Register 0x0247-0x0249 R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x0247	7:0	R/W	R0_REG	24-bit integer final R0A divider selection. R Divisor = (R0_REG+1) x 2 However, note that setting R0A_REG = 0 will not set the output to divide-by-2. See notes below.
0x0248	15:8			
0x0249	23:16			

The final output R dividers are even dividers beginning with divide-by-2. While all other values follow the formula in the bit description above, divide-by-2 requires an extra bit to be set. For divide-by-2, set OUT0_RDIV_FORCE=1. See the description for register bit 0x0103[2] in this register map.

The R0-R9A dividers follow the same format as the R0A divider description above.

Table 12.61. Registers that Follow the R0_REG

Register Address	Description	Size	Same as Address
0x024A-0x024C	R0_REG	24-bit Integer Number	0x0247-0x0249
0x024D-0x024F	R1_REG	24-bit Integer Number	0x0247-0x0249
0x0250-0x0252	R2_REG	24-bit Integer Number	0x0247-0x0249
0x0253-0x0255	R3_REG	24-bit Integer Number	0x0247-0x0249
0x0256-0x0258	R4_REG	24-bit Integer Number	0x0247-0x0249
0x0259-0x025B	R5_REG	24-bit Integer Number	0x0247-0x0249
0x025C-0x025E	R6_REG	24-bit Integer Number	0x0247-0x0249
0x025F-0x0261	R7_REG	24-bit Integer Number	0x0247-0x0249
0x0262-0x0264	R8_REG	24-bit Integer Number	0x0247-0x0249
0x0268-0x026A	R9_REG	24-bit Integer Number	0x0247-0x0249
0x026B-0x026D	R9A_REG	24-bit Integer Number	0x0247-0x0249

Table 12.62. Register 0x026B0x0272 User Design Identifier

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by the ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, ULT. 1Anull character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6: 0x00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 12.63. Register 0x02780x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5380C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

See 11.3 Part Numbering Summary for more information on part numbers.

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Table 12.64. Register 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 12.65. Register 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. Note that this ratio of Nx_NUM / Nx_DEN should be an integer for proper operation of the device. The N output dividers feed into the final output R dividers through the output crosspoint.

Table 12.66. Register 0x0308-0x030B N0 Update

Reg Address	Bit Field	Type	Name	Description
0x030C	0	R/W	N0_UPDATE	Set this bit to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. A Soft Reset will have the same effect.

Table 12.67. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C
0x032E-0x0333	N4_NUM	44-bit Integer	0x0302-0x0307

Register Address	Description	Size	Same as Address
0x0334-0x0337	N4_DEN	32-bit Integer	0x0308-0x030B
0x0338	N4_UPDATE	one bit	0x030C

Table 12.68. Register 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	R/W	N_UPDATE_ALL	Writing a 1 to this bit will update the N output divider values. When this bit is written to 1, all other bits in this register must be written as zeros.

This bit is provided so that all of the divider bits can be changed at the same time. First, write all of the new values to Nx_NUM and Nx_DEN, then set the update bit to 1.

Table 12.69. Register 0x03590x35A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359-0x035A	7:0	R/W	N0_DELAY[15:8]	8-bit, 2s-complement delay for N0

N0_DELAY[7:0] is an 8-bit 2's-complement number that sets the output delay of the N0 divider. ClockBuilder Pro calculates the correct value for this register. A Soft Reset of the device, SOFT_RST (0x001C[0] = 1), required to latch in the new delay value(s). Note that the least significant byte (0x0359) is ignored.

t_{DLY} = Nx_DELAY * 67.8 ps

f_{VCO}=14.7456 GHz, 1/fVCO=67.8 ps

Table 12.70. Register 0x035B0x035C N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035B-0x035C	7:0	R/W	N1_DELAY[15:8]	8-bit, 2s-complement delay for N1

N1_DELAY behaves in the same manner as N0_DELAY.

Table 12.71. Register 0x035D0x035E N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035D-0x035E	7:0	R/W	N2_DELAY[15:8]	8-bit, 2s-complement delay for N2

N2_DELAY behaves in the same manner as N0_DELAY above.

Table 12.72. Register 0x035F0x0360 N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035F-0x0360	7:0	R/W	N3_DELAY[15:8]	8-bit, 2s-complement delay for N3

N3_DELAY behaves in the same manner as N0_DELAY above.

Table 12.73. Register 0x03610x0362 N4 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0361-0x0362	7:0	R/W	N4_DELAY[15:8]	8-bit, 2s-complement delay for N4

N4_DELAY behaves in the same manner as N0_DELAY above.

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Table 12.74. Register 0x0487 Zero Delay Mode Setup

Reg Address	Bit Field	Type	Name	Description
Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	Enable ZDM. 0: Disable Zero Delay Mode (default) 1: Enable Zero Delay Mode

To enable ZDM, set ZDM_EN 0x0487[0]=1. In ZDM, the DSPLL cannot use either Hitless switching or Automatic switching. The DSPLL input clock selection between IN0, IN1, and IN2 must be made manually. As with manual input clock switching discussed earlier in this manual, the ZDM manual selection can be done by either pins or register, depending on the state of the IN_SEL_REGCTRL register bit.

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Table 12.75. Register 0x0507

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3/FB_IN

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the voltages on the IN_SEL1 and INSEL0 pins or the register value. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented.

Table 12.76. Register 0x0508-0x050D DSPLL Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	7:0	R/W	BW0_PLL	DSPLL loop bandwidth parameters.
0x0509	7:0	R/W	BW1_PLL	
0x050A	7:0	R/W	BW2_PLL	
0x050B	7:0	R/W	BW3_PLL	
0x050C	7:0	R/W	BW4_PLL	
0x050D	7:0	R/W	BW5_PLL	

This group of registers determines the DSPLL loop bandwidth. In ClockBuilder Pro it is selectable from 0.1 Hz to 100 Hz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 12.77. Register 0x050E-0x0513 DSPLL Fastlock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	7:0	R/W	FAST_BW0_PLL	DSPLL Fastlock Bandwidth parameters.
0x050F	7:0	R/W	FAST_BW1_PLL	
0x0510	7:0	R/W	FAST_BW2_PLL	
0x0511	7:0	R/W	FAST_BW3_PLL	
0x0512	7:0	R/W	FAST_BW4_PLL	
0x0513	7:0	R/W	FAST_BW5_PLL	

This group of registers determines the DSPLL Fastlock bandwidth. In Clock Builder Pro, it is selectable from 100 Hz to 4 kHz in factors of roughly 2x each. Clock Builder Pro will then determine the values for each of these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the FAST_BWx_PLL parameters to take effect.

Table 12.78. Register 0x0514 DSPLL Bandwidth Update

Reg Address	Bit Field	Type	Name	Description
0x0514	0	S	BW_UPDATE	Set to 1 to latch updated BWx_PLL and FAST_BWx_PLL bandwidth registers into operation.

Setting this self-clearing bit high latches the new bandwidth register values into operation. Asserting this strobe will update both the normal loop bandwidth as well as the Fastlock mode bandwidth for the DSPLL. A Soft Reset will have the same effect.

Table 12.79. Register 0x0515-0x051B M Feedback Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	M feedback divider Numerator 56-bit Integer
0x0516	15:8			
0x0517	23:16			
0x0518	31:24			
0x0519	39:32			
0x051A	47:40			
0x051B	55:48			

Table 12.80. Register 0x051C-0x051F M Feedback Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	M feedback divider Denominator 32-bit Integer
0x051E	15:8			
0x051E	23:16			
0x051F	31:24			

The DSPLL M feedback divider values are calculated by Clock Builder Pro for a particular frequency plan and are written into these registers.
Note: This ration of M_NUM/M_DEN should be an integer for proper operation of the device.

Note: There is a divide-by-5 prescaler before the M divider, so if M_NUM/M_DEN=100, the effective feedback divide ration will be 500.

Table 12.81. Register 0x0520 M Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0520	0	R/W	M_UPDATE	Set this bit to latch the M feedback divider registers into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 12.82. Register 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	Manual Input Select control source. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection
0x052A	2:1	R/W	IN_SEL	Manual Input Select selection register. 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3/FB_IN

Input clock selection for manual register based and pin controlled clock selection.
Note: When ZDM_EN (0x0487[0]) and IN_SEL_REGCTRL are both 1, IN_SEL is disabled and the clock selection is pin controlled. When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 12.83. Register 0x052B Fastlock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
0x052B	1	R/W	FASTLOCK_MAN	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN=0 and FASTLOCK_AUTO_EN=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock Feature for more information on Fastlock behavior.

Table 12.84. Register 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP	Must be set to 1 for Normal Operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL	Selects the exit rate from Holdover bandwidth. 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 12.85. Register 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.6 Holdover Mode to calculate the window length from the register value.

Table 12.86. Register 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.6 Holdover Mode to calculate the ignore delay time from the register value.

Table 12.87. Register 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID = 0 =>Freerun Mode HOLD_HIST_VALID = 1 =>Holdover Mode

Table 12.88. Register 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 00: Manual (default), 01: Automatic Non-revertive, 02: Automatic Revertive, 03: Reserved
0x0536	2	R/W	HSW_EN	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 12.89. Register 0x0537 Input Fault Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic
0x0537	7:4	R/W	IN_OOF_MSK	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.
Note: The clock selection logic can affect entry into Holdover.

Table 12.90. Register 0x0538-0x0539 Clock Input Priorities

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4, or 0 for never selected 5-7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY	
0x0539	2:0	R/W	IN2_PRIORITY	
0x0539	6:4	R/W	IN3_PRIORITY	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 12.91. Register 0x053F DSPLL Hold Valid and Fastlock Status

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R	HOLD_HIST_VALID	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Free-run on input fail 1: Valid Holdover History - Holdover on input fail
0x053F	2	R	FASTLOCK_STATUS	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

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Table 12.92. Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	This bit selects between the Crystal or External reference clock on the XAXB pins. 0: Crystal on XAXB, enable internal XO (default) 1: External XAXB signal, internal XO disabled
0x090E	1	R/W	XAXB_XO_EN	Powerdown the built-in low noise crystal oscillator when using an external reference input. 0: Powerdown Internal Oscillator 1: Internal Oscillator Powered (default) - required when using a crystal with the XAXB input.

Table 12.93. Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	Select digital I/O operating voltage. 0: 1.8 V digital I/O connections 1: 3.3 V digital I/O connections

The IO_VDD_SEL configuration bit selects between 1.8V and 3.3V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3V tolerant. Setting this to the default 1.8V is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I^2C or SPI host is operating at 3.3V and the Si5380 at VDD=1.8V, the host must write IO_VDD_SEL=1. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 12.94. Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	Select Pulsed CMOS input buffer for IN3-IN0. See for more information. 0: Standard Input Format 1: Pulsed CMOS Input Format

When a clock input is disabled, it is powered down as well.

- IN0: IN_EN 0x0949[0], IN_PULSED_CMOS_EN 0x0949[4]
- IN1: IN_EN 0x0949[1], IN_PULSED_CMOS_EN 0x0949[5]
- IN2: IN_EN 0x0949[2], IN_PULSED_CMOS_EN 0x0949[6]

- IN3/FB_IN: IN_EN 0x0949[3], IN_PULSED_CMOS_EN 0x0949[7]

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Table 12.95. Register 0x0A03 Output N Divider to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Enable the output N dividers. Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

Clock Builder Pro handles these bits when changing settings for the device.

Table 12.96. Register 0x0A04 Output N Divider Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Must be set to 1 for Normal Operation.

Clock Builder Pro handles these bits when changing settings for the device.

Table 12.97. Register 0x0A05 Output N Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the output N4 - N0 dividers. 0: Powerdown unused N dividers 1: Power-up active N dividers See related registers 0x0A03 and 0x0B4A[4:0].

Clock Builder Pro handles these bits when changing settings for the device.

12.9 Page B Registers

Table 12.98. Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Making Register Changes During Device Operation for more information.

Table 12.99. Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Making Register Changes During Device Operation for more information.

Table 12.100. Register 0x0B46 Loss of Signal Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS clock for IN3 - IN0. Must be set to 0 to enable the LOS function of the respective inputs.

Clock Builder Pro handles these bits when changing settings for all portions of the device.

Table 12.101. Register 0x0B24 Reserved Control_2

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

Clock Builder Pro handles these bits when changing settings for the device.

Table 12.102. Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M divider. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

Clock Builder Pro handles these bits when changing settings for the device.

Appendix 1. Custom Differential Amplitude Controls

In some customer applications, it may be desirable to have larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings generated by ClockBuilder Pro. For example, "CML" format is sometimes desired for an application, but CML is not a defined standard, and, hence, the input amplitude of CML signals may differ between receivers. In these cases, the following information describes how to implement nonstandard differential amplitudes.

The differential output driver has two basic modes of operation as well as variable output amplitude capability. The Normal mode has an internal impedance of 100 Ω differential, while the Low Power mode has an internal impedance of >500 Ω differential. In both cases, when properly terminated with 100 Ω differential externally, the typical amplitudes listed in the table below result.

Table 1.1. Differential Output Amplitude Typical Values

OUTx_AMPL	Normal Mode OUTx_FORMAT = 1 (mVpp-SE)	Low-Power Mode OUTx_FORMAT = 2 (mVpp-SE)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Note:
1. In Low-Power mode with VDDO=1.8 V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon 100 Ω differential termination.

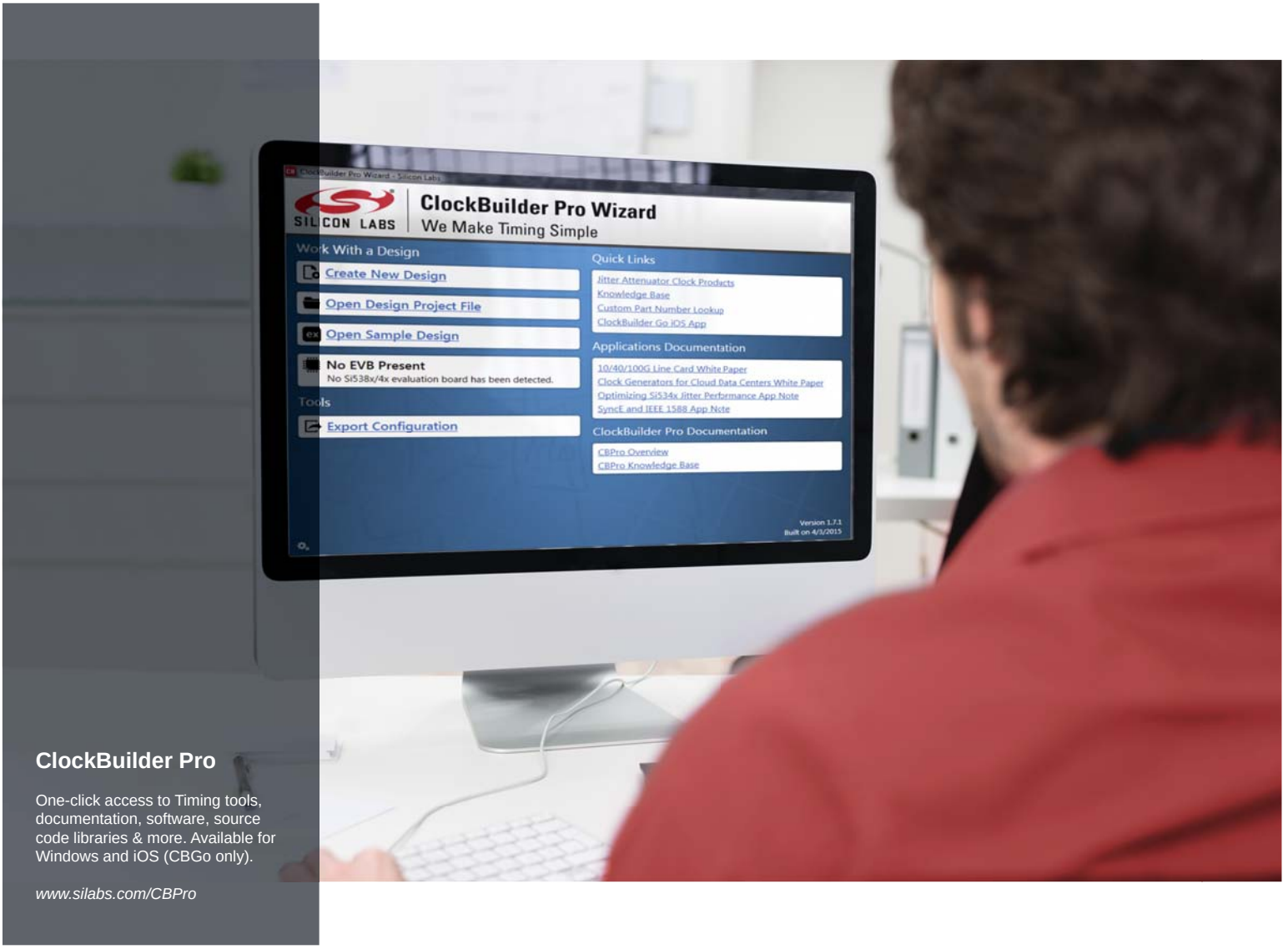
For applications using a custom differential output amplitude, the common mode voltage should be selected as shown in the table below. These selections, along with the settings given in Table 4.6 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 35, have been verified to produce good signal integrity. Some extreme combinations of amplitude and common mode may have impaired signal integrity.

Also, in cases where the receiver is dc-based, either internally or through an external network, the outputs of the device must be ac-coupled. Output driver performance is not guaranteed when dc-coupled to a biased-input receiver.

Table 1.2. Differential Output Common Mode Voltage Selections

VDDO (Volts)	Differential Format	OUTx_FORMAT	Common Mode Voltage (Volts)	OUTx_CM
3.3	Normal	0x1	2.0	0xB
3.3	Low-Power	0x2	1.6	0x7
2.5	Normal	0x1	1.3	0xC
2.5	Low-Power	0x2	1.1	0xA
1.8	Normal	0x1	0.8	0xD
1.8	Low-Power	0x2	0.8	0xD

See also Table 4.6 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 35 for additional information on the OUTx_FORMAT_OUTx_AMPL, and OUTx_CM controls.



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