

## TL1431-EP Precision-Programmable Reference

### 1 Features

- 0.4% Initial Voltage Tolerance
- 0.2- $\Omega$  Typical Output Impedance
- Fast Turnon: 500 ns
- Sink Current Capability: 1 to 100 mA
- Low Reference Current (REF)
- Adjustable Output Voltage:  $V_{I(\text{ref})}$  to 36 V
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

### 2 Applications

- Shunt Regulators
- Temperature-Compensated Comparators
- PWM Converter Reference
- Photodiode Reference Drivers
- Precision Current Limiters
- Precision Current Sink

### 3 Description

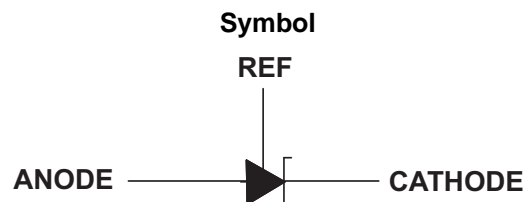
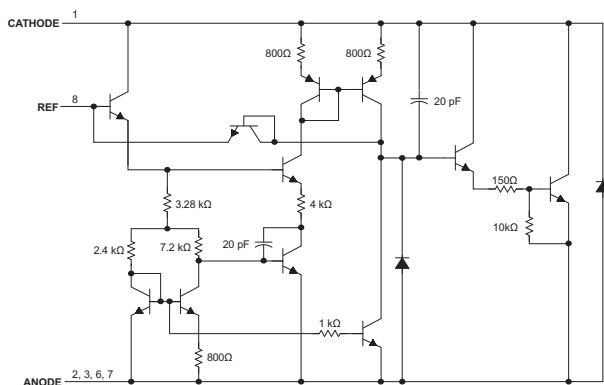
The TL1431-EP device is a precision-programmable reference with specified thermal stability over the military temperature range. The output voltage can be set to any value from  $V_{I(\text{ref})}$  (approximately 2.5 V) to 36 V with two external resistors (see [Figure 21](#)). This device has a typical output impedance of 0.2  $\Omega$ . Active output circuitry provides a very sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| TL1431-EP   | SOIC (8) | 3.91 mm x 4.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



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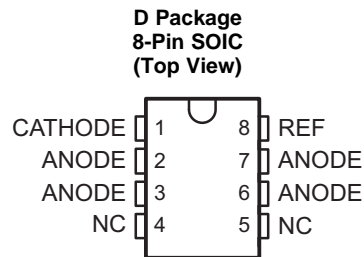
## 5 Revision History

### Changes from Revision C (December 2006) to Revision D

**Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....
- Changed pinout title from JG to D Package .....

## 6 Pin Configuration and Functions



NC – No internal connection

### Pin Functions

| PIN |         | I/O | DESCRIPTION                         |
|-----|---------|-----|-------------------------------------|
| NO. | NAME    |     |                                     |
| 1   | CATHODE | I/O | Cathode                             |
| 2   | ANODE   | I/O | ANODE pins are connected internally |
| 3   |         | I/O |                                     |
| 6   |         | I/O |                                     |
| 7   |         | I/O |                                     |
| 4   | NC      | —   | No internal connection              |
| 5   |         |     |                                     |
| 8   | REF     | I   | Reference                           |

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|   | MIN      | MAX | UNIT |
|---|----------|-----|------|
| Cathode voltage <sup>(2)</sup> , $V_{KA}$                     |          | 37  | V    |
| Continuous cathode current, $I_{KA}$                          | -100     | 150 | mA   |
| Reference input current, $I_{I(ref)}$                         | -0.00005 | 10  | mA   |
| Operating virtual junction temperature <sup>(3)</sup> , $T_J$ |          | 150 | °C   |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 s        |          | 260 | °C   |
| Storage temperature, $T_{stg}$                                | -65      | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ANODE, unless otherwise noted.
- (3) Long-term high-temperature storage and/or use at the absolute maximum ratings may result in a reduction of overall device life. See [www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

### 7.2 ESD Ratings

|             |                         | VALUE  | UNIT |
|-------------|-------------------------|--|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | V    |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> |      |
|             |                         | ±4000  |      |
|             |                         | ±2000  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|          |                                | MIN          | MAX | UNIT |
|----------|--------------------------------|--------------|-----|------|
| $V_{KA}$ | Cathode voltage                | $V_{I(ref)}$ | 36  | V    |
| $I_{KA}$ | Cathode current                | 1            | 100 | mA   |
| $T_A$    | Operating free-air temperature | -55          | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |   | TL1431-EP | UNIT |
|-------------------------------|---|-----------|------|
|                               |   | D         |      |
|                               |   | 8 PINS    |      |
| $R_{\theta JA(high)}$         | Junction-to-ambient thermal resistance (high K board) | 97        | °C/W |
| $R_{\theta JA(low)}$          | Junction-to-ambient thermal resistance (low K board)  | 165       |      |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://SPRA953).

### 7.5 Dissipation Rating Table

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | PACKAGE<br>THERMAL<br>IMPEDANCE | DERATING<br>FACTOR<br>ABOVE $T_A =$<br>$25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>ABSOLUTE<br>MAXIMUM<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>ABSOLUTE<br>MAXIMUM<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>ABSOLUTE<br>MAXIMUM<br>POWER RATING |
|---------|---|---------------------------------|---|---|---|--|
| D       | 1102 mW                                     | 97°C/W (High K board)           | 10 mW/°C  | 824 mW  | 670 mW  | 257 mW   |
|         |   | 165°C/W (Low K board)           | 6 mW/°C   | 484 mW  | 393 mW  | 151 mW   |

## 7.6 Electrical Characteristics

 at specified free-air temperature,  $I_{KA} = 10 \text{ mA}$  (unless otherwise noted)

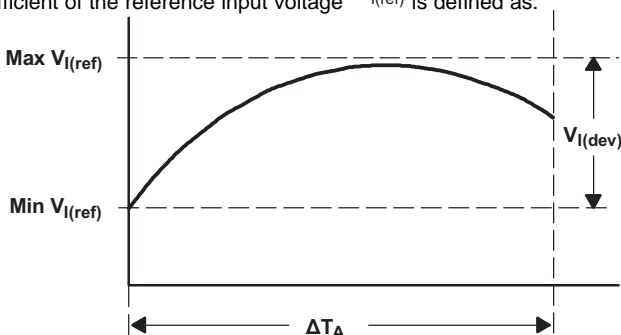
| PARAMETER  |   | TEST CONDITIONS   | $T_A$ (1)  | TEST CIRCUIT | MIN  | TYP  | MAX  | UNIT          |
|--|---|---|------------|--------------|------|------|------|---------------|
| $V_{I(\text{ref})}$                              | Reference input voltage   | $V_{KA} = V_{I(\text{ref})}$  | 25°C       | Figure 8     | 2490 | 2500 | 2510 | mV            |
|  |   |   | Full range |              | 2470 |      | 2530 |               |
| $V_{I(\text{dev})}$                              | Deviation of reference input voltage over full temperature range(2)         | $V_{KA} = V_{I(\text{ref})}$  | Full range | Figure 8     |      | 17   |      | mV            |
| $\frac{\Delta V_{I(\text{ref})}}{\Delta V_{KA}}$ | Ratio of change in reference input voltage to the change in cathode voltage | $\Delta V_{KA} = 3 \text{ to } 36 \text{ V}$  | Full range | Figure 9     |      | -1.1 | -2   | mV/V          |
| $I_{I(\text{ref})}$                              | Reference input current   | $R1 = 10 \text{ k}\Omega, R2 = \infty$  | 25°C       | Figure 9     |      | 1.5  | 2.5  | $\mu\text{A}$ |
|  |   |   | Full range |              |      |      | 4    |               |
| $I_{I(\text{dev})}$                              | Deviation of reference input current over full temperature range(2)         | $R1 = 10 \text{ k}\Omega, R2 = \infty$  | Full range | Figure 9     |      | 0.5  |      | $\mu\text{A}$ |
| $I_{\text{min}}$                                 | Minimum cathode current for regulation                                      | $V_{KA} = V_{I(\text{ref})}$  | 25°C       | Figure 8     |      | 0.45 | 1    | mA            |
| $I_{\text{off}}$                                 | Off-state cathode current   | $V_{KA} = 36 \text{ V}, V_{I(\text{ref})} = 0$  | 25°C       | Figure 10    |      | 0.18 | 0.5  | $\mu\text{A}$ |
|  |   |   | Full range |              |      |      | 2    |               |
| $ z_{KA} $                                       | Output impedance(3)   | $V_{KA} = V_{I(\text{ref})}, f \leq 1 \text{ kHz}, I_{KA} = 1 \text{ to } 100 \text{ mA}$ | 25°C       | Figure 8     |      | 0.2  | 0.4  | $\Omega$      |

 (1) Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for Q-suffix devices;  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for M-suffix devices.

 (2) The deviation parameters  $V_{I(\text{dev})}$  and  $I_{I(\text{dev})}$  are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage  $\alpha_{V_{I(\text{ref})}}$  is defined as:

$$\alpha_{V_{I(\text{ref})}} \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left( \frac{V_{I(\text{dev})}}{V_{I(\text{ref}) \text{ at } 25^\circ\text{C}}} \right) \times 10^6}{\Delta T_A}$$

where:

 $\Delta T_A$  is the rated operating temperature range of the device.

 $\alpha_{V_{I(\text{ref})}}$  is positive or negative, depending on whether minimum  $V_{I(\text{ref})}$  or maximum  $V_{I(\text{ref})}$ , respectively, occurs at the lower temperature.

 (3) The output impedance is defined as:  $z_{KA} = \frac{\Delta V_{KA}}{\Delta I_{KA}}$   
 When the device is operating with two external resistors (see Figure 9), the total dynamic impedance of the circuit is given by:

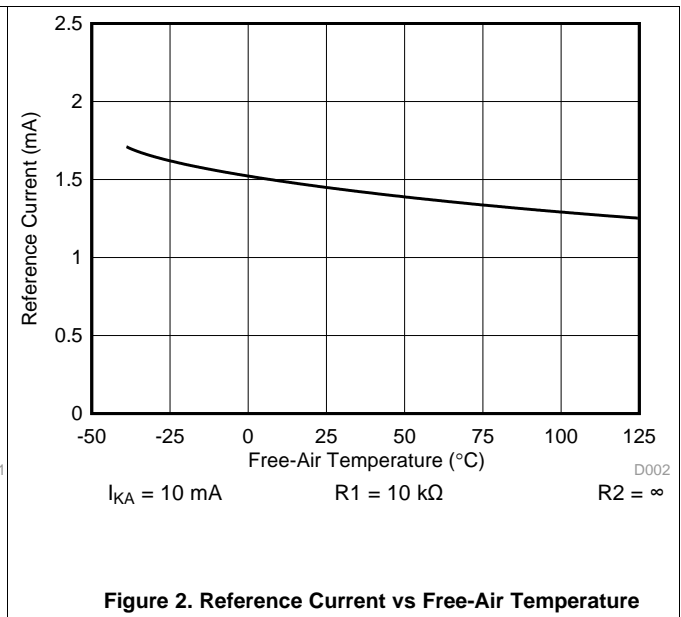
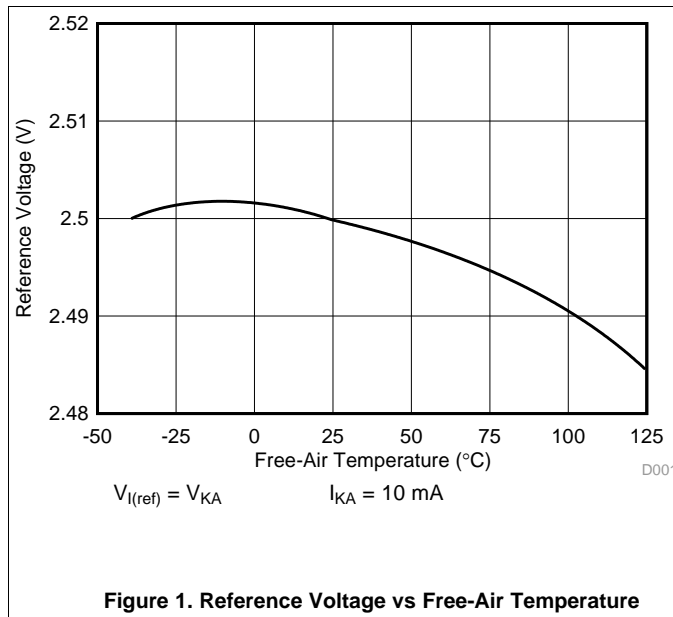
$$|z| = \frac{\Delta V}{\Delta I}, \text{ which is approximately equal to } z_{KA} = \left( 1 + \frac{R1}{R2} \right).$$

## 7.7 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature range.

**Table 1. Table of Graphs**

| GRAPH TITLE   | FIGURE             |
|---|--------------------|
| Reference voltage vs Free-Air Temperature   | Figure 1           |
| Reference current vs Free-Air Temperature   | Figure 2           |
| Cathode Current vs Cathode Voltage  | Figure 3, Figure 4 |
| Off-State Cathode Current vs Free-Air Temperature                                 | Figure 5           |
| Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-Air Temperature | Figure 6           |
| Equivalent Input-Noise Voltage vs Frequency                                       | Figure 7           |
| Equivalent Input-Noise Voltage Over a 10-s Period                                 | Figure 11          |
| Small-Signal Voltage Amplification vs Frequency                                   | Figure 13          |
| Reference Impedance vs Frequency  | Figure 15          |
| Pulse Response  | Figure 17          |
| Stability Boundary Conditions   | Figure 19          |



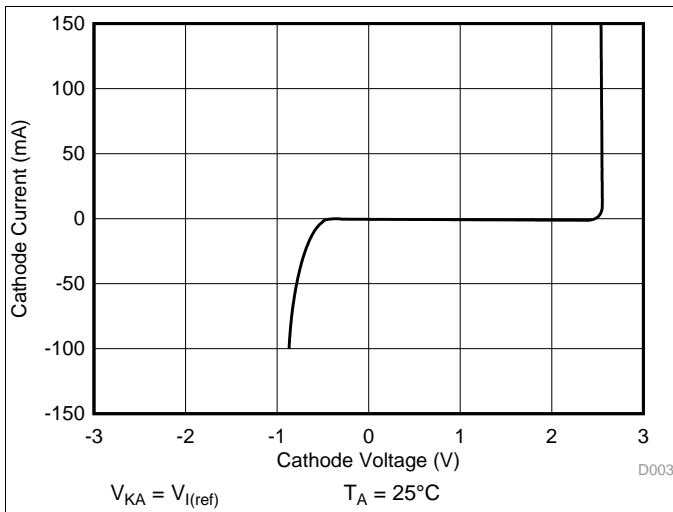


Figure 3. Cathode Current vs Cathode Voltage

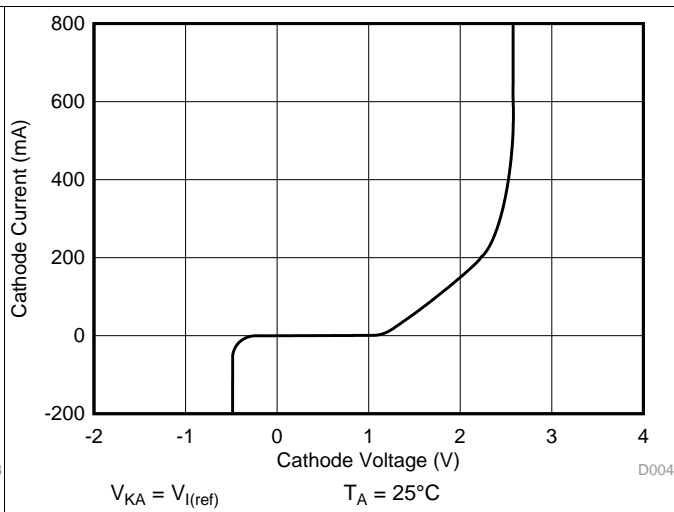


Figure 4. Cathode Current vs Cathode Voltage

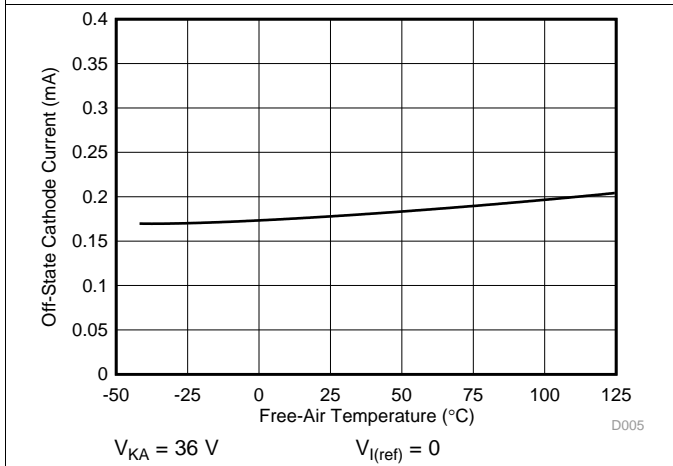


Figure 5. Off-State Cathode Current vs Free-Air Temperature

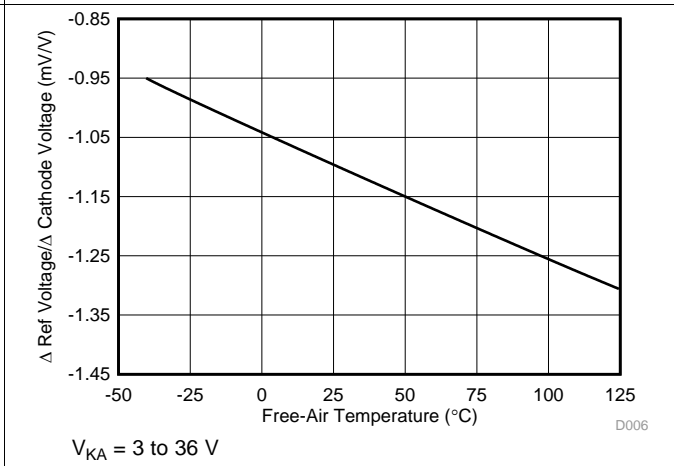


Figure 6. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-Air Temperature

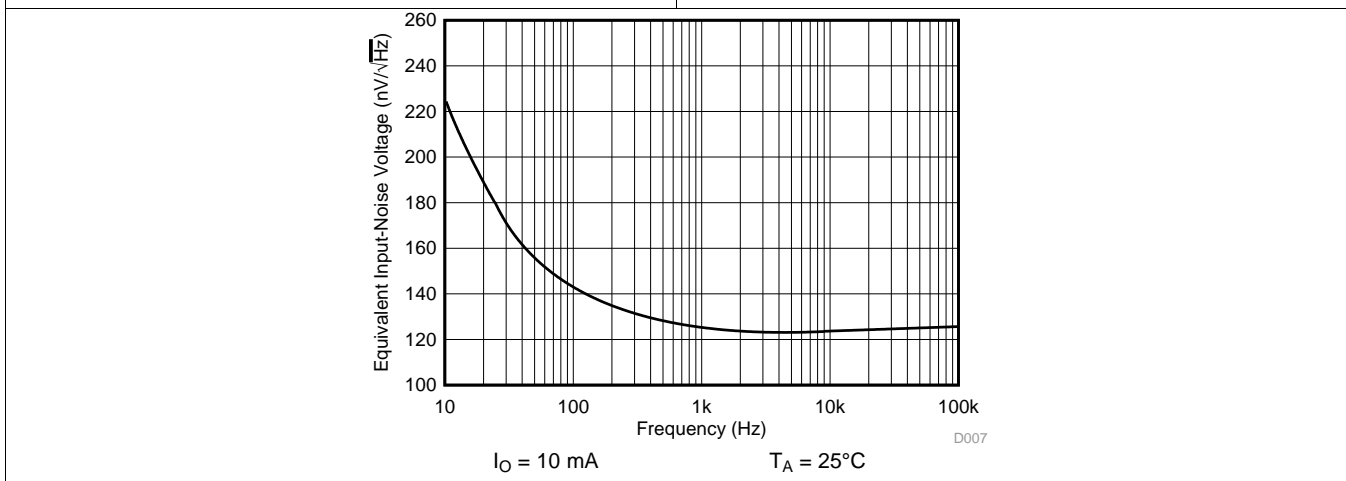


Figure 7. Equivalent Input-Noise Voltage vs Frequency

## 8 Parameter Measurement Information

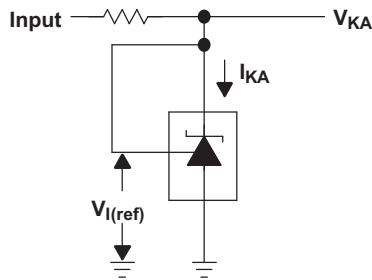


Figure 8. Test Circuit for  $V_{(KA)} = V_{ref}$

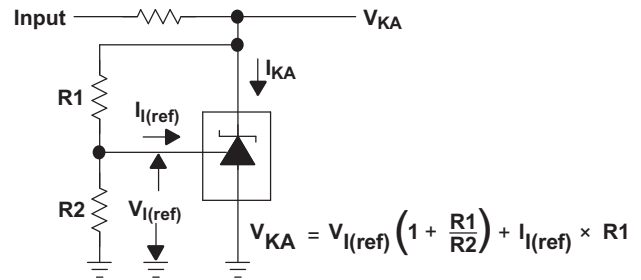


Figure 9. Test Circuit for  $V_{(KA)} > V_{ref}$

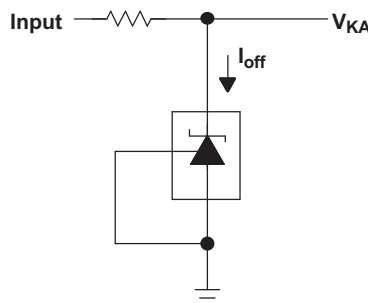


Figure 10. Test Circuit for  $I_{off}$

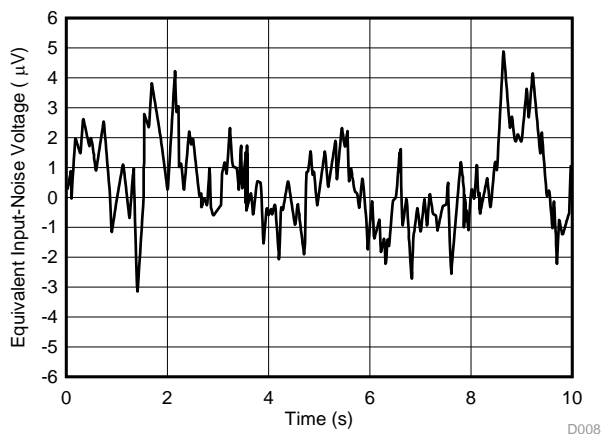


Figure 11. Equivalent Input-Noise Voltage Over a 10-s Period

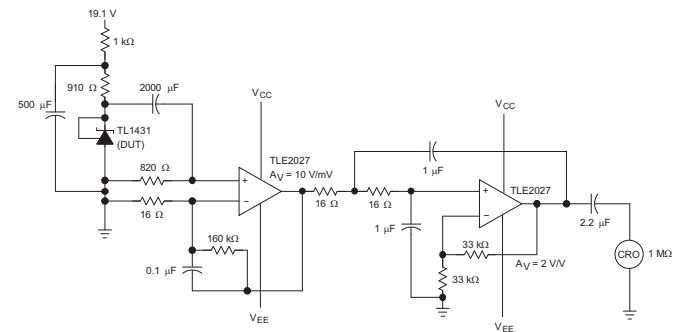


Figure 12. Test Circuit for 0.1- to 10-Hz Equivalent Input-Noise Voltage



Parameter Measurement Information (continued)

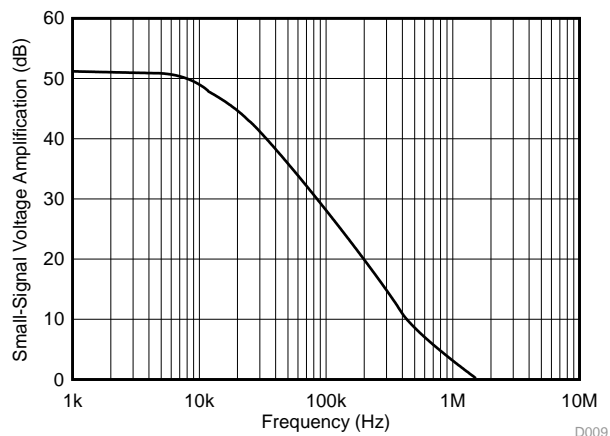


Figure 13. Small-Signal Voltage Amplification vs Frequency

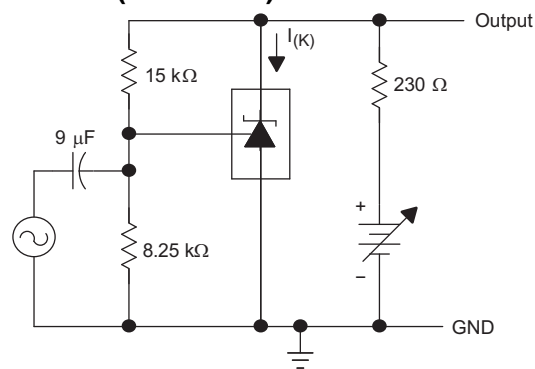


Figure 14. Test Circuit for Voltage Amplification

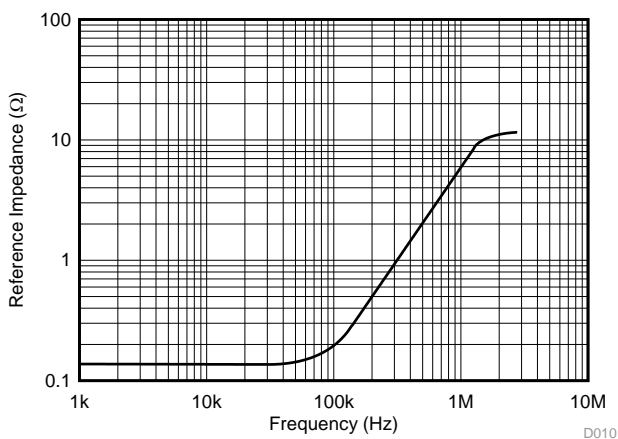


Figure 15. Reference Impedance vs Frequency

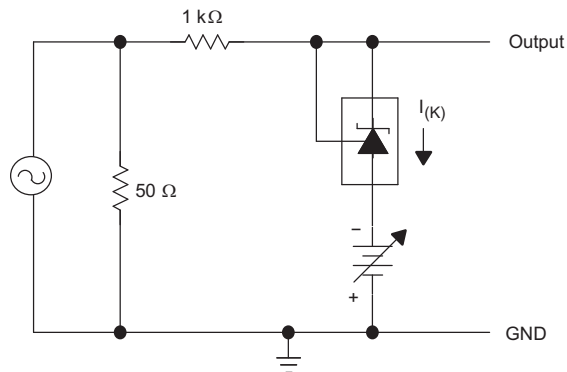


Figure 16. Test Circuit for Reference Impedance

Parameter Measurement Information (continued)

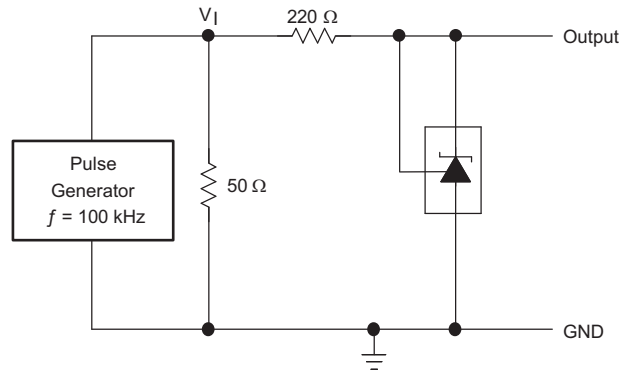
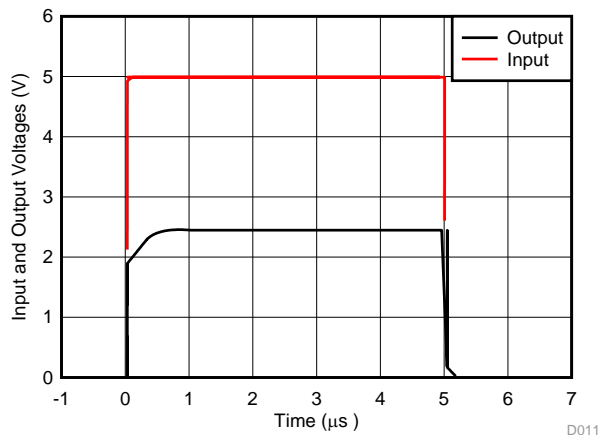


Figure 17. Pulse Response

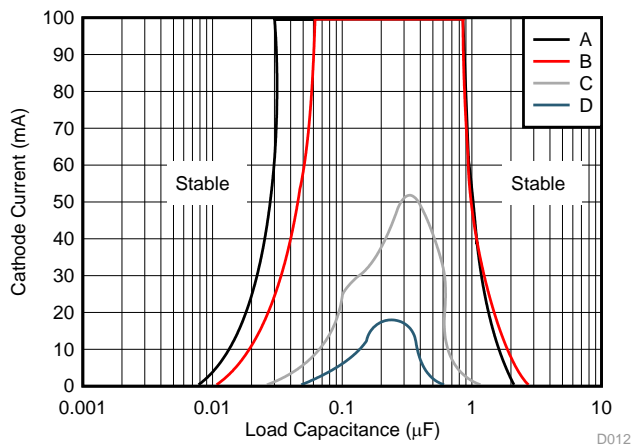
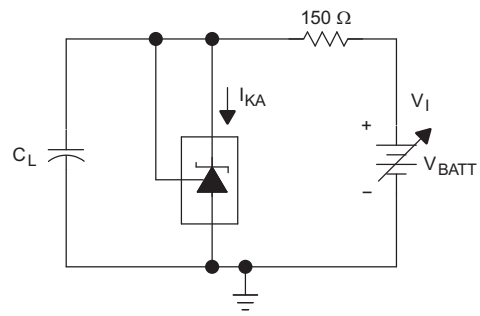
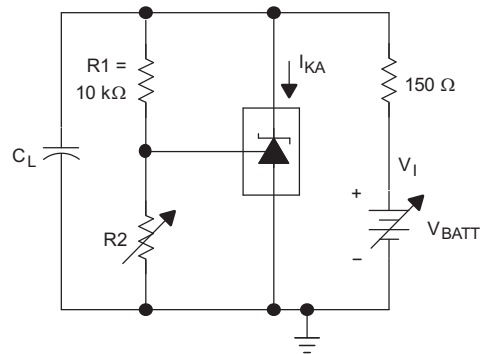


Figure 18. Test Circuit for Pulse Response



Test Circuit for Curve A



Test Circuit for Curves B, C, and D

Figure 19. Stability Boundary Conditions

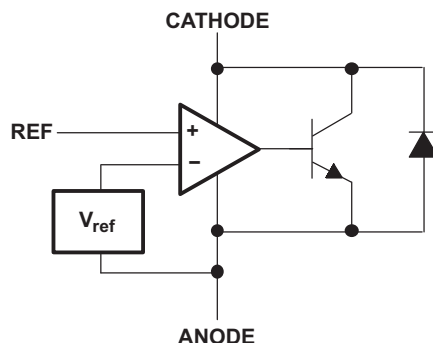
Figure 20. Test Circuits for Curves A through D

## 9 Detailed Description

### 9.1 Overview

The TL1431-EP is a precision-programmable reference with specified thermal stability over the military temperature range. The device can be used in a very wide array of applications, and can enter operational mode with as little as two external resistors.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

The output voltage can be set to any value between  $V_{I(\text{ref})}$  and 36 V. Active output circuitry provides a very sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

TI's EP line is certified to the Aerospace Qualified Electronic Component (AQEC) Standard (ANSI/GEIA STD-0002-1). The AQEC Standard was jointly developed by the aerospace and semiconductor industries to define the minimum requirements for commercial-off-the-shelf (COTS) components used in military, avionic, aerospace, medical and other rugged operating environments where high-reliability and long service life are required.

### 9.4 Device Functional Modes

The device only has one functional mode, which is enabled at power up. Operation of the device is determined by external parameters described [Application and Implementation](#).

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The ability to set the shunt voltage,  $V_{KA}$ , to any voltage between  $V_{REF}$  and the maximum rated voltage for the shunt regulator provides a lot of flexibility. It takes two resistors to set the shunt voltage. In an ideal common anode shunt regulator, the shunt voltage would be  $V_{REF} \times (R_1/R_2 + 1)$ .

Real world shunt regulators have limited gain, non-zero reference input current, and suffer from cathode voltage modulation. This application report derives comprehensive formulas that accurately represent the relationship between the shunt voltage and feedback resistors. It also shows a practical example.

#### 10.1.1 Shunt Regulator Limitations

Real world shunt regulators have three parameters that should be considered.

- Dynamic impedance,  $Z_{KA}$
- Reference pin current,  $I_{REF}$
- Ratio of change in reference voltage to the change in cathode voltage,  $\Delta V_{REF}/\Delta V_{KA}$ .

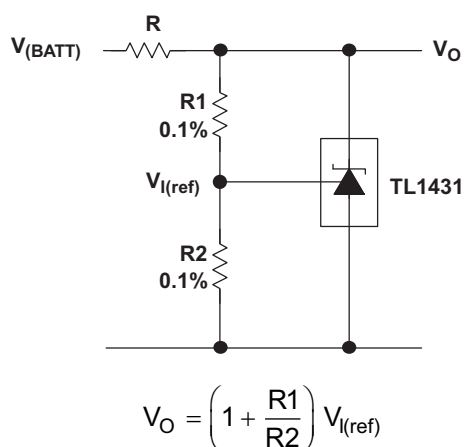
The first parameter will cause a  $V_{REF}$  shift for all  $V_{KA}$  values and the last two only apply when  $V_{KA}$  is set greater than  $V_{REF}$ .

$Z_{KA}$  offsets the  $V_{REF}$  in direct proportion to the cathode current. The data sheet generally specifies  $V_{REF}$  at a specific current. At any other current  $Z_{KA}$  impacts  $V_{REF}$ .

$I_{REF}$  causes an inequality in the feedback resistor currents which changes the effective DC feedback ratio. This factor is often included in data sheet formulas.

$\Delta V_{REF}/\Delta V_{KA}$  specifies how much the  $V_{REF}$  voltage changes when the cathode voltage changes. This is a frequently ignored factor although the effect can be significant.

### 10.2 Typical Application



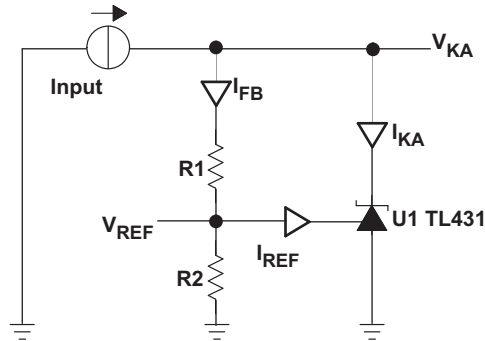
NOTE: R should provide cathode current  $\geq 1$  mA to the TL1431-EP at minimum  $V_{(BATT)}$ .

**Figure 21. Shunt Regulator**

## Typical Application (continued)

### 10.2.1 Design Requirements

To calculate the values for resistors  $R_1$  and  $R_2$ , the values of the following parameters must be known: the feedback current, ( $I_{FB}$ ), cathode current, ( $I_{KA}$ ), and desired shunt voltage, ( $V_{KA}$ ).



The [Electrical Characteristics](#) table specifies when  $V_{KA} = V_{REF}$  and  $I_{KA}$  is 10 mA the nominal  $V_{REF}$ , (labeled  $V_{NOM}$ ) is 2.5 V. The reference voltage varies with cathode voltage at two different rates. The reference voltage is  $-1.1$  mV/V from  $V_{REF}$  to 10 V then  $-1.5$  mV/V above 10 V. The reference pin current is 4  $\mu$ A.

The  $Z_{KA}$  parameter offsets  $V_{REF}$  by  $(I_{KA} - I_{NOM}) \times Z_{KA}$ .

In addition, the  $\Delta V_{REF} / \Delta V_{KA}$  parameter offsets  $V_{REF}$  by either  $-1.1$  mV  $\times (V_{KA} - 2.5$  V) if  $V_{KA} \leq 10$  V or  $-8.25$  mV  $-1.5$  mV/V  $\times (V_{KA} - 10$  V) if  $V_{KA} > 10$  V. The  $-8.25$ -mV constant is the  $V_{REF}$  offset as  $V_{KA}$  changes from  $V_{NOM}$  to 10 V,  $(10$  V  $- 2.5$  V)  $\times -1.1$  mV/V.

Therefore:

If  $V_{KA} \leq 10$  V then;

$$V_{REF} = V_{NOM} + (I_{KA} - I_{NOM}) \times Z_{KA} + (V_{KA} - V_{NOM}) \times -1.1 \text{ mV/V} \quad (1)$$

If  $V_{KA} > 10$  then;

$$V_{REF} = V_{NOM} + (I_{KA} - I_{NOM}) \times Z_{KA} + (V_{KA} - 10 \text{ V}) \times -1.5 \text{ mV/V} - 8.25 \text{ mV} \quad (2)$$

Now that the value of  $V_{REF}$  is calculated, use [Equation 1](#) and [Equation 2](#) to calculate the value of  $R_1$  and  $R_2$ .

$$R_1 = (V_{KA} - V_{REF}) / I_{FB} \quad (3)$$

$$R_2 = V_{REF} / (I_{FB} - I_{REF}) \quad (4)$$

#### NOTE

$R_2$  has less current than  $R_1$ .

### 10.2.2 Detailed Design Procedure

The goal of the design is: the TL1431 cathode set to 12 V, the cathode current at 2 mA, and a feedback current of 0.2 mA.

Using the formula derived in the general example for  $V_{KA} > 10$  V.

$$V_{REF} = V_{NOM} + (I_{KA} - I_{NOM}) \times Z_{KA} + (V_{KA} - 10 \text{ V}) \times -1.1 \text{ mV} - 8.25 \text{ mV} \quad (5)$$

$$V_{REF} = 2.500 \text{ V} + (2 \text{ mA} - 10 \text{ mA}) \times 2 \Omega + (12 \text{ V} - 10 \text{ V}) \times -1.1 \text{ mV} - 8.25 \text{ mV} \quad (6)$$

Using [Equation 5](#) and [Equation 6](#), the value of  $V_{REF} = 2.473$  V

$$R_1 = (V_{KA} - V_{REF}) / I_{FB} \quad (7)$$

$$R_1 = (12 \text{ V} - 2.473 \text{ V}) / 0.2 \text{ mA} \quad (8)$$

Using [Equation 7](#) and [Equation 8](#), the value of  $R_1 = 46.285$  k $\Omega$

### Typical Application (continued)

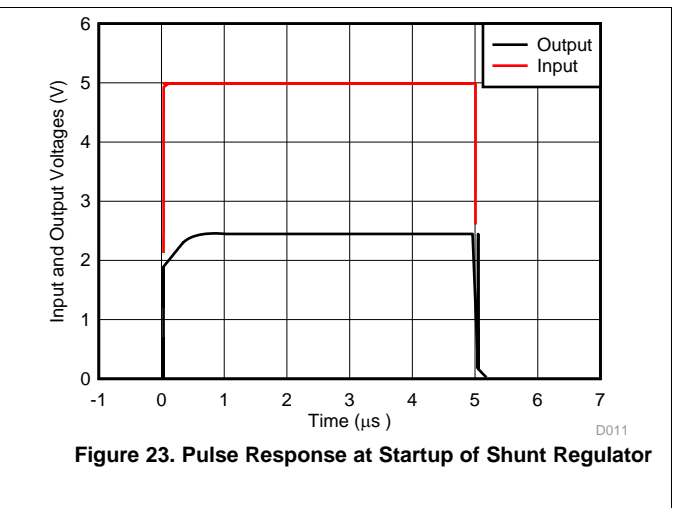
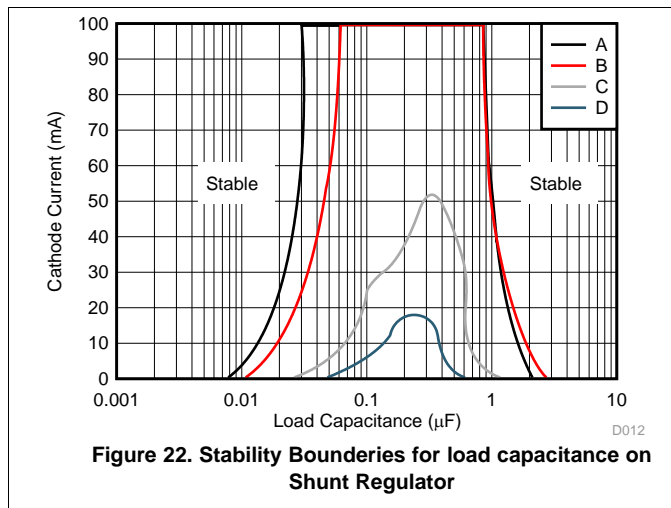
$$R_2 = V_{REF} / (I_{FB} - I_{REF}) \tag{9}$$

$$R_2 = 2.473 \text{ V} / (0.2 \text{ mA} - 4 \mu\text{A}) \tag{10}$$

Using Equation 9 and Equation 10, the value of  $R_2 = 12.617 \text{ k}\Omega$

The closest standard 1% resistor values are  $R_1 = 46.4 \text{ k}\Omega$  and  $R_2 = 12.7 \text{ k}\Omega$ . Other resistor combinations may provide a shunt voltage that is centered better. A formula to test for  $R_1$  values that may be closer to standard values using standard  $R_2$  resistors is  $R_1 = (V_{KA} - V_{REF}) / (V_{REF} / R_2 + I_{REF})$ .

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

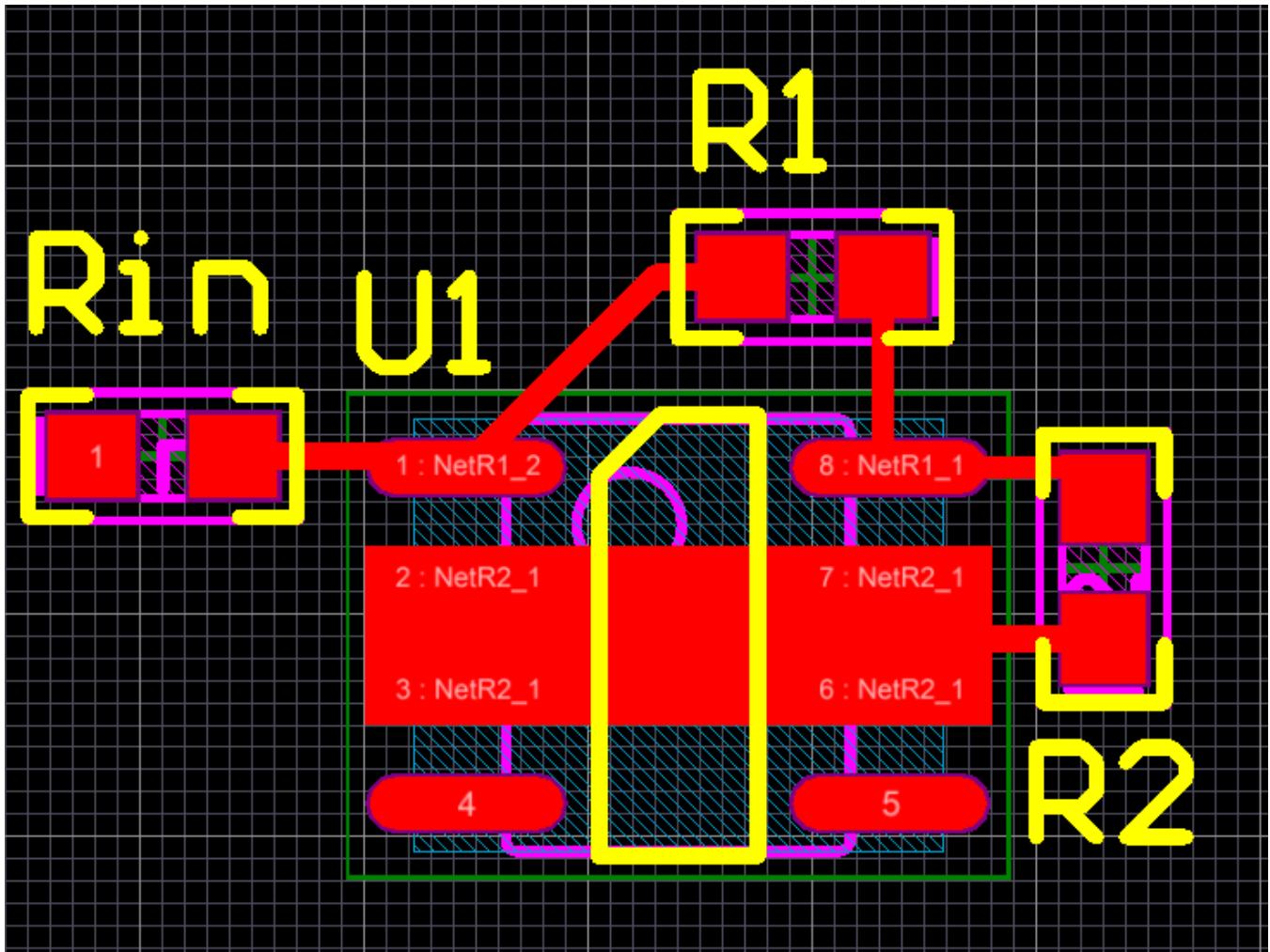
Do not exceed the values listed in the *Recommended Operating Conditions* and *Electrical Characteristics*. To ensure proper operation, deliver a minimum of 1 mA of current to the cathode. Ensure that the power source can provide at least 1 mA of current across the entire voltage range.

## 12 Layout

### 12.1 Layout Guidelines

Pins 2, 3, 6, and 7 are connected internally to the anode. For the most precision, tie these pins together externally as well. Resistors should be placed as close as possible to the device.

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL1431MDREP      | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | 1431ME                  | <a href="#">Samples</a> |
| TL1431MDREPG4    | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | 1431ME                  | <a href="#">Samples</a> |
| TL1431QDREP      | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 1431QE                  | <a href="#">Samples</a> |
| V62/04756-01XE   | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 1431QE                  | <a href="#">Samples</a> |
| V62/04756-02XE   | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | 1431ME                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TL1431-EP :**

- Catalog: [TL1431](#)
- Automotive: [TL1431-Q1](#)
- Military: [TL1431M](#)
- Space: [TL1431-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL1431MDREP | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL1431QDREP | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL1431MDREP | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| TL1431QDREP | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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