Mobile Low-Power SDR SDRAM

MT48H16M16LF – 4 Meg x 16 x 4 banks
MT48H8M32LF – 2 Meg x 32 x 4 banks

Features

- V_{DD}/V_{DDQ} = 1.7–1.95V
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, and continuous
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive strength (DS)
- 64ms refresh period

Options	Marking
• V_{DD}/V_{DDQ}: 1.8V/1.8V	H
• Addressing	
– Standard addressing option	LF
• Configuration	
– 16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
– 8 Meg x 32 (2 Meg x 32 x 4 banks)	8M32
• Plastic “green” packages	
– 54-ball VFBGA (8mm x 9mm)[1]	BF
– 90-ball VFBGA (8mm x 13mm)[2]	B5
• Timing – cycle time	
– 6ns @ CL = 3	-6
– 7.5ns @ CL = 3	-75
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Revision	:H

Notes: 1. Available only for x16 configuration.
2. Available only for x32 configuration.

Table 1: Configuration Addressing

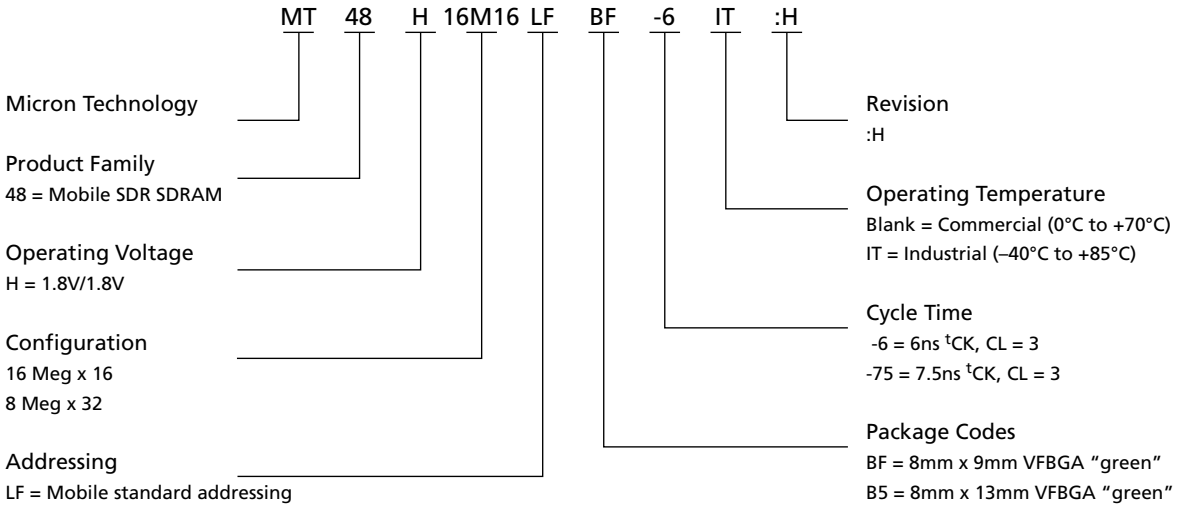
Architecture	16 Meg x 16	8 Meg x 32
Number of banks	4	4
Bank address balls	BA0, BA1	BA0, BA1
Row address balls	A[12:0]	A[11:0]
Column address balls	A[8:0]	A[8:0]

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	104	166	8.0ns	5.0ns
-75	104	133	8.0ns	5.4ns

Note: 1. CL = CAS (READ) latency

Figure 1: 256Mb Mobile LPSDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

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General Description

The 256Mb Mobile LPSDR is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks is organized as 8192 rows by 512 columns by 16 bits. Each of the x32's 67,108,864-bit banks is organized as 4096 rows by 512 columns by 32 bits.

Note:

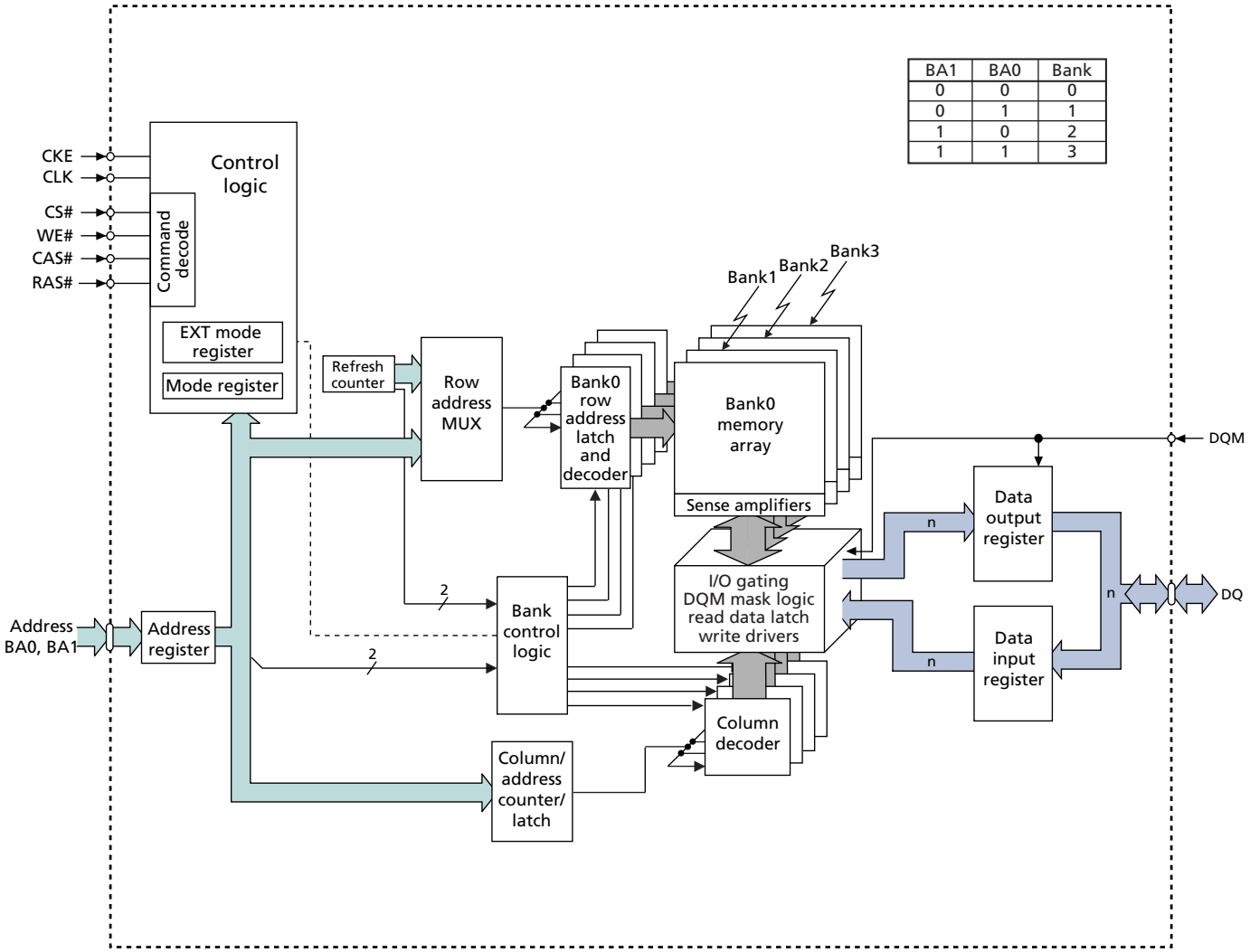
1. Throughout the data sheet, various figures and text refer to DQs as DQ. DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DQM refers to LDQM. For the upper byte (DQ[15:8]), DQM refers to UDQM. The x32 is divided into four bytes. For DQ[7:0], DQM refers to DQM0. For DQ[15:8], DQM refers to DQM1. For DQ[23:16], DQM refers to DQM2, and for DQ[31:24], DQM refers to DQM3.

2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

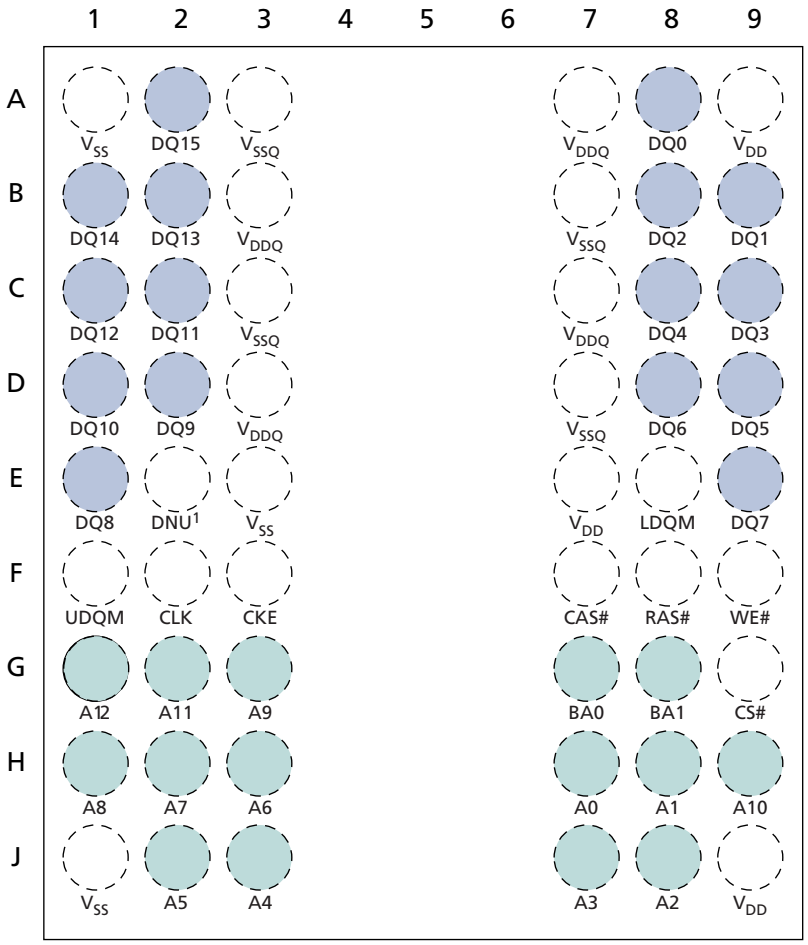
Functional Block Diagram

Figure 2: Functional Block Diagram



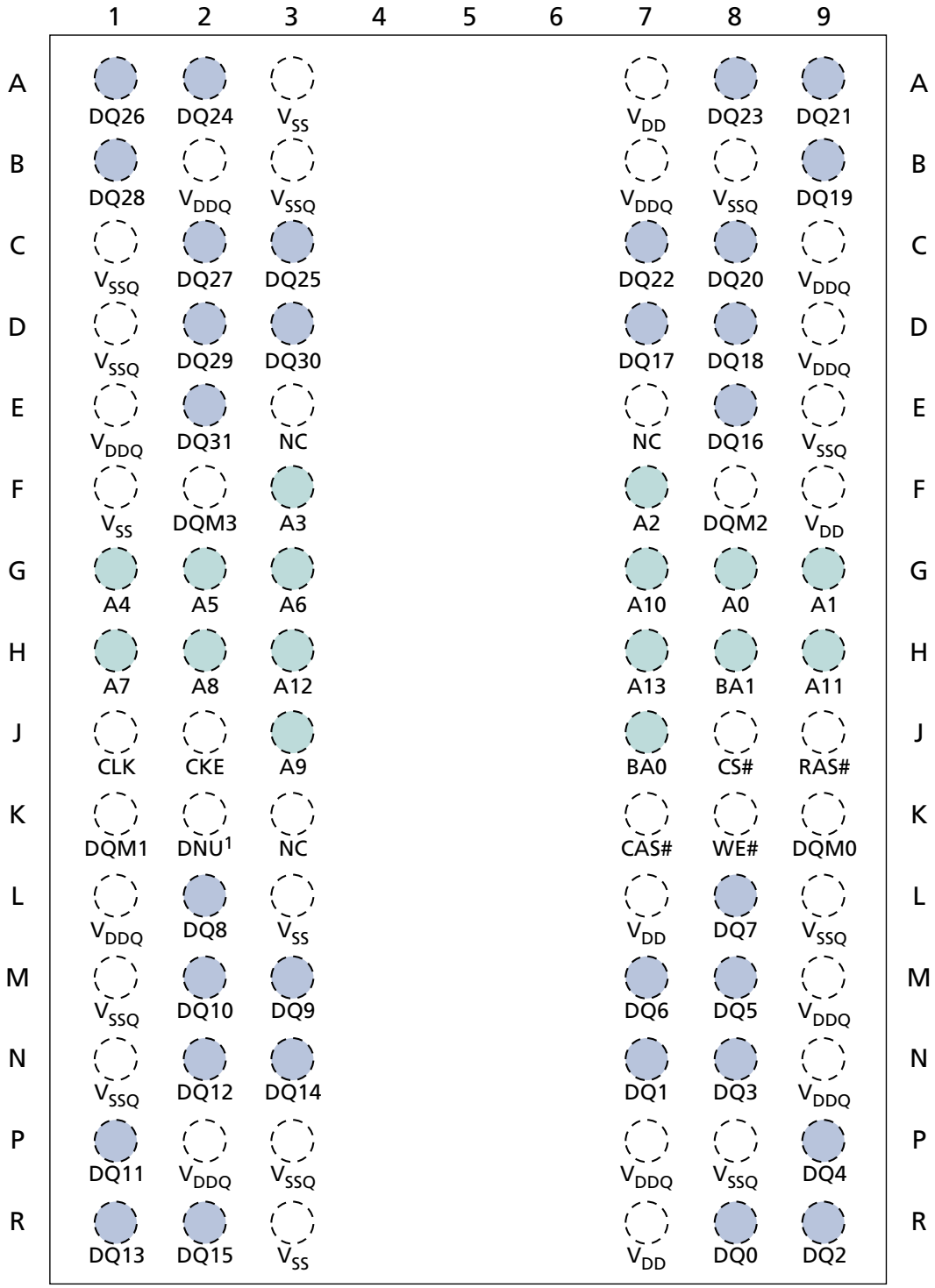
Ball Assignments and Descriptions

Figure 3: 54-Ball VFBGA (Top View)



Note: 1. The E2 pin must be connected to V_{SS}, V_{SSQ}, or left floating.

Figure 4: 90-Ball VFBGA (Top View)



Note: 1. The K2 pin must be connected to V_{SS}, V_{SSQ}, or left floating.

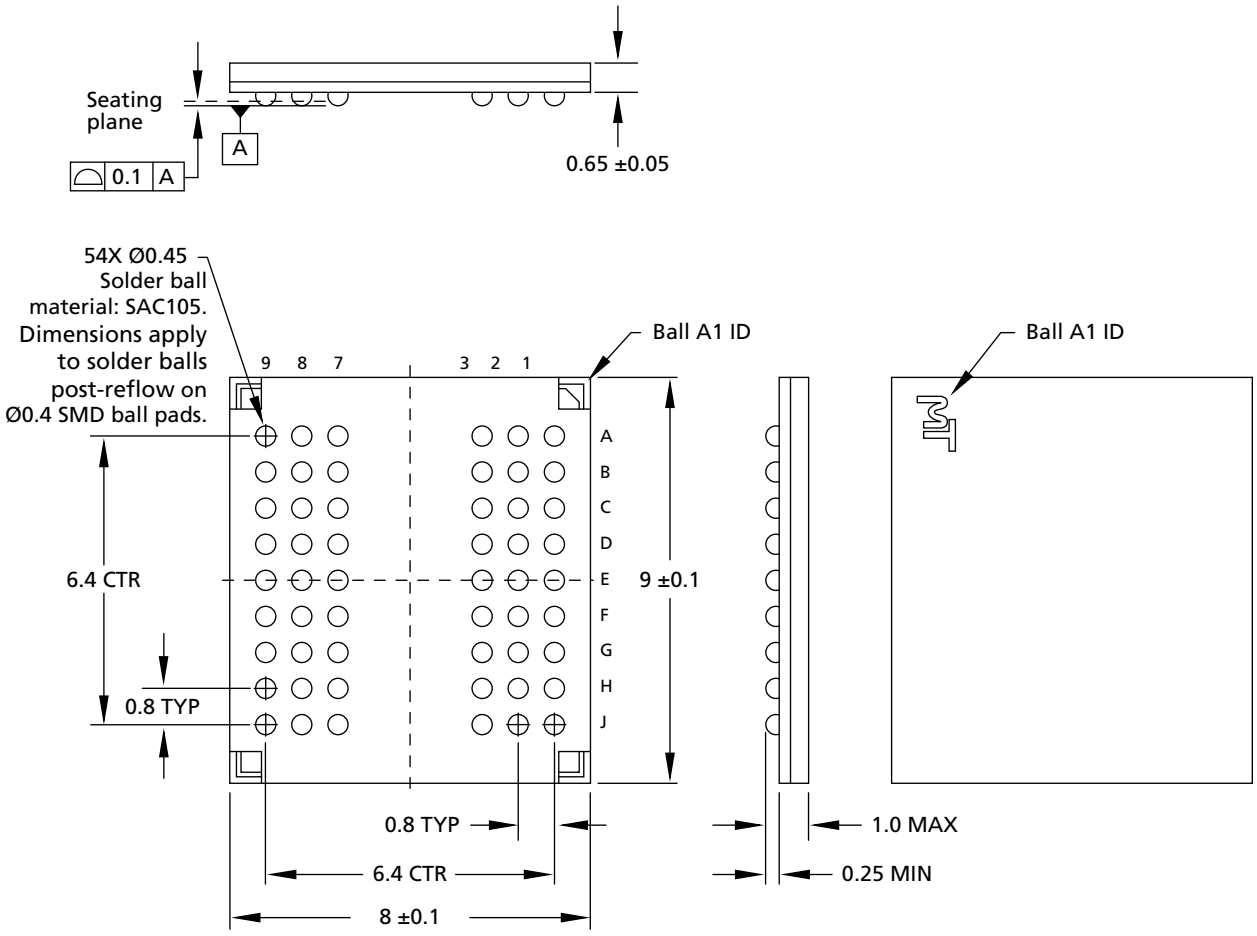
Table 3: VFBGA Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
LDQM, UDQM (54-ball) DQM[3:0] (90-ball)	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ[7:0] and UDQM corresponds to DQ[16:8]. For the x32, DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] (or LDQM and UDQM if x16) are considered same state when referenced as DQM.
BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 become "Don't Care" when registering an ALL BANK PRECHARGE (A10 HIGH).
A[13:0]	Input	Address inputs: Addresses are sampled during the ACTIVE command (row) and READ/WRITE command [column); column address A[9:0] (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address pins become RFU.[1]
DQ[31:0]	I/O	Data input/output: Data bus.
V_{DDQ}	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
V_{SSQ}	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
V_{DD}	Supply	Core power supply.
V_{SS}	Supply	Ground.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	Internally not connected. These balls can be left unconnected but it is recommended that they be connected to V_{SS}.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.

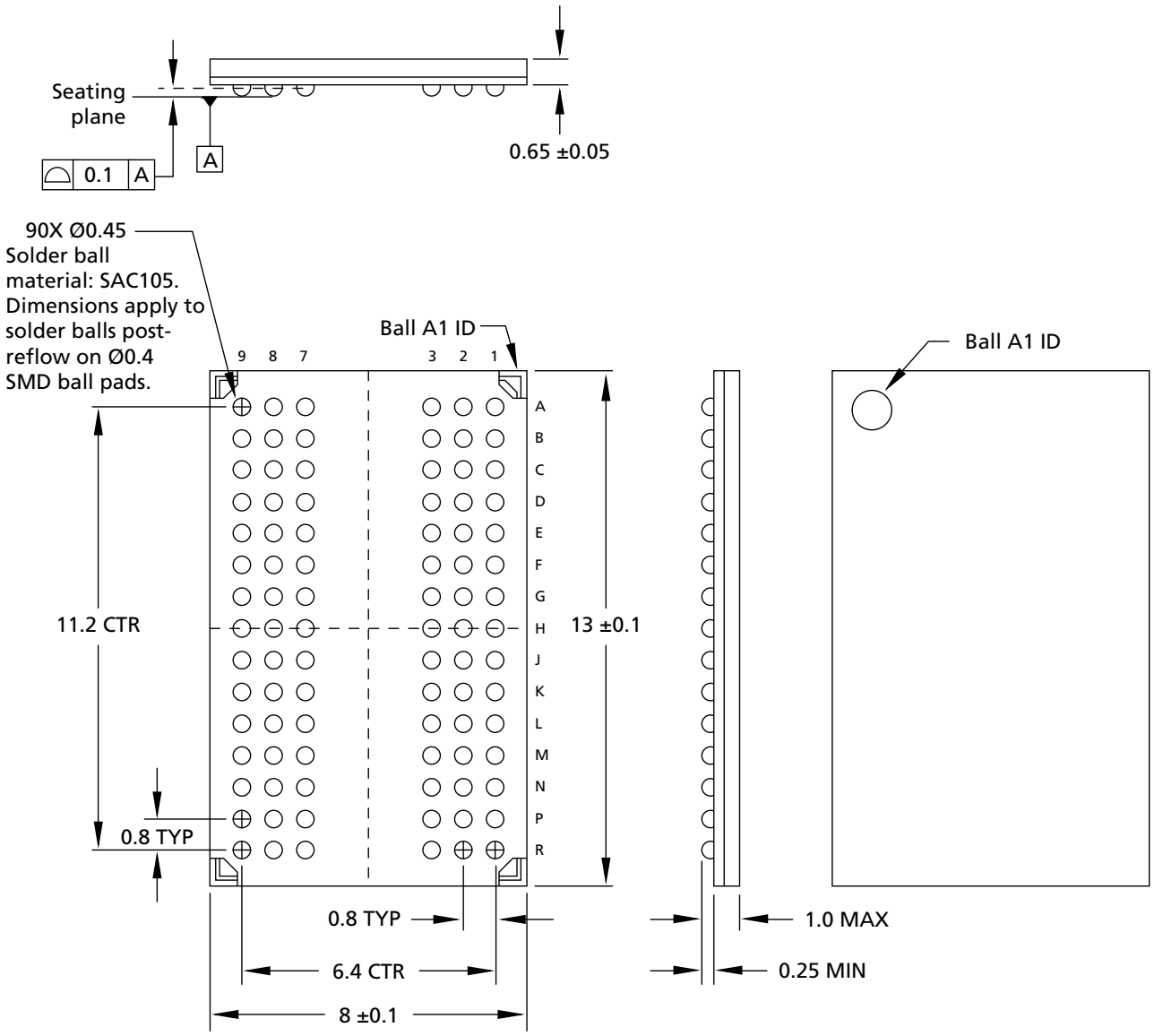
Package Dimensions

Figure 5: 54-Ball VFBGA (8mm x 9mm)



Note: 1. All dimensions are in millimeters.

Figure 6: 90-Ball VFBGA (8mm x 13mm)



Note: 1. All dimensions are in millimeters.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Unit
Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS}	V_{DD}/V_{DDQ}	–0.35	+2.7	V
Voltage on inputs, NC, or I/O balls relative to V_{SS}	V_{IN}	–0.35	+2.7	
Storage temperature (plastic)	T_{STG}	–55	+150	°C

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 5: DC Electrical Characteristics and Operating Conditions

Notes 1 and 2 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 1.7–1.95V

Parameter/Condition		Symbol	Min	Max	Unit	Notes
Supply voltage		V_{DD}	1.7	+1.95	V	
I/O supply voltage		V_{DDQ}	1.7	+1.95	V	
Input high voltage: Logic 1; All inputs		V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	3
Input low voltage: Logic 0; All inputs		V_{IL}	–0.3	+0.3	V	3
Output high voltage		V_{OH}	0.9 × V_{DDQ}	–	V	4
Output low voltage		V_{OL}	–	+0.2	V	4
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)		I_L	–1.0	+1.0	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		I_{OZ}	–1.5	+1.5	µA	
Operating temperature:	Industrial	T_A	–40	+85	°C	
	Commercial	T_A	0	+70	°C	

Notes: 1. All voltages referenced to V_{SS}.
2. A full initialization sequence is required before proper device operation is ensured.
3. V_{IH} overshoot: $V_{IH,max}$ = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: $V_{IL,min}$ = –2V for a pulse width ≤3ns.
4. I_{OUT} = 4mA for full drive strength. Other drive strengths require appropriate scale.

Table 6: Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	Min	Max	Unit
Input capacitance: CLK	C_{L1}	2.0	5.0	pF
Input capacitance: All other input-only balls	C_{L2}	2.0	5.0	pF
Input/output capacitance: DQ	C_{L0}	2.5	6.0	pF

Note: 1. This parameter is sampled. V_{DD}, V_{DDQ} = +1.8V; T_A = 25°C; ball under test biased at 0.9V, f = 1 MHz.

Electrical Specifications – I_{DD} Parameters

Table 7: I_{DD} Specifications and Conditions (x16)

Note 1 applies to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max		Unit	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	50	45	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P}	300	300	µA	5
Standby current: Nonpower-down mode; All banks idle; CKE = HIGH		I_{DD2N}	15	12	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	3	3	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	20	20	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half of DQ toggling every cycle		I_{DD4}	80	70	mA	2, 3, 4
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	90	85	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	I_{DD6}	1	1	mA	2, 3, 4, 7
Deep power-down		I_{ZZ}	10	10	µA	5, 8

Table 8: I_{DD} Specifications and Conditions (x32)

Note 1 applies to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max		Unit	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	75	60	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P}	300	300	µA	5
Standby current: Nonpower-down mode; All banks idle; CKE = HIGH		I_{DD2N}	15	12	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	3	3	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	20	20	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half of DQ toggling every cycle		I_{DD4}	100	85	mA	2, 3, 4
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	90	85	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	I_{DD6}	1	1	mA	2, 3, 4, 7
Deep power-down		I_{ZZ}	10	10	µA	5, 8

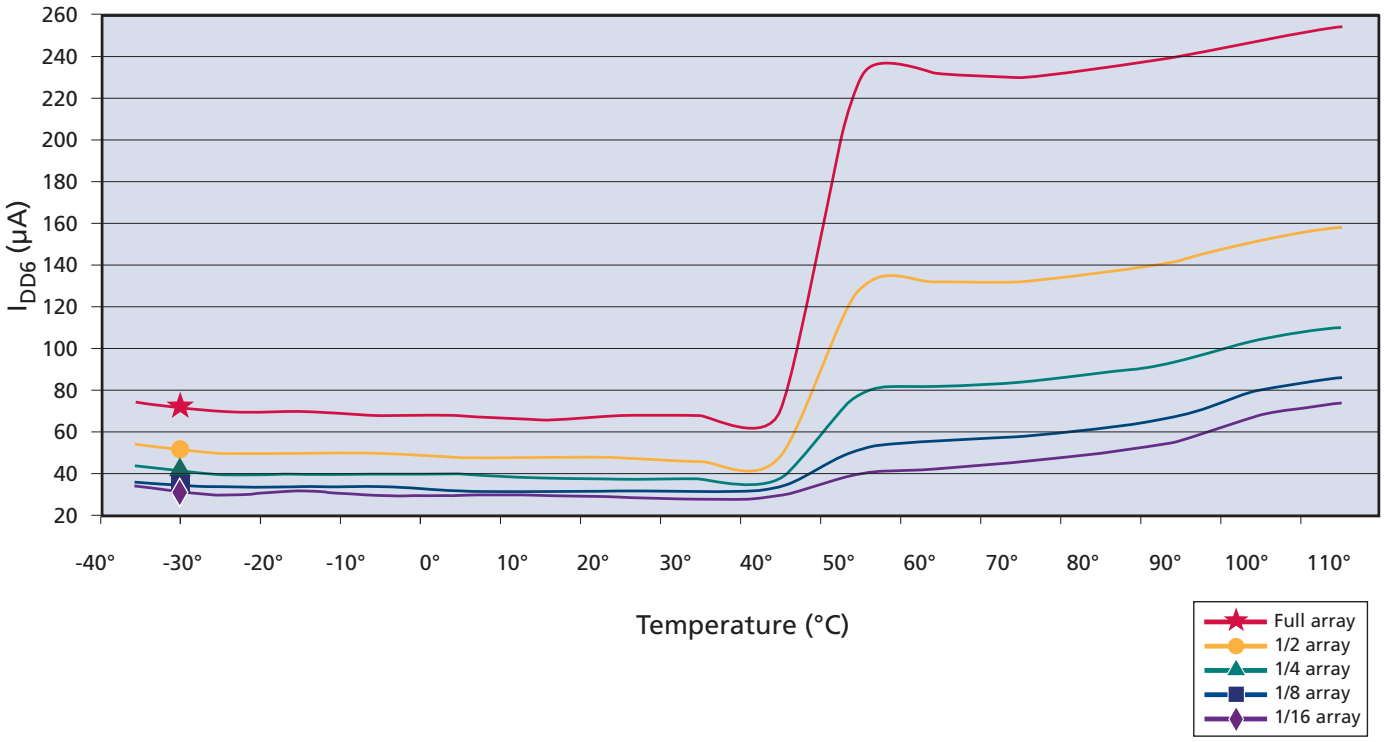
Table 9: I_{DD7} Specifications and Conditions (x16 and x32)

Notes 1, 5, 9, and 10 apply to all parameters and conditions; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	I_{DD7}	Unit
Self refresh: CKE = LOW; ^{t}CK = ^{t}CK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 85˚C	I_{DD7}	300	µA
	Full array, 45˚C		190	µA
	1/2 array, 85˚C		250	µA
	1/2 array, 45˚C		150	µA
	1/4 array, 85˚C		230	µA
	1/4 array, 45˚C		130	µA
	1/8 array, 85˚C		220	µA
	1/8 array, 45˚C		120	µA
	1/16 array, 85˚C		200	µA
	1/16 array, 45˚C		110	µA

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. Measurement is taken 500ms after entering into this operating mode to provide tester measuring unit settling time.
6. Other input signals can transition only one time for every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
7. CKE is HIGH during REFRESH command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD7} limit is a nominal value and does not result in a fail value.
8. Typical values at 25˚C (not a maximum value).
9. Enables on-die refresh and address counters.
10. Values for I_{DD7} 85˚C full array and partial array are guaranteed for the entire temperature range. All other I_{DD7} values are estimated.

Figure 7: Typical Self Refresh Current vs. Temperature



Electrical Specifications – AC Operating Conditions

Table 10: Electrical Characteristics and Recommended AC Operating Conditions

Notes 1–5 apply to all parameters and conditions

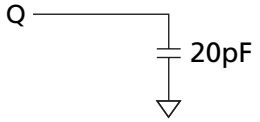
Parameter		Symbol	-6		-75		Unit	Notes
			Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	tAC	–	5	–	5.4	ns	
	CL = 2		–	8	–	8		
Address hold time		tAH	1	–	1	–	ns	
Address setup time		tAS	1.5	–	1.5	–	ns	
CLK high-level width		tCH	2.5	–	2.5	–	ns	
CLK low-level width		tCL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	tCK	6	–	7.5	–	ns	6
	CL = 2		9.6	–	9.6	–		
CKE hold time		tCKH	1	–	1	–	ns	
CKE setup time		tCKS	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	0.5	–	0.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	1.5	–	1.5	–	ns	
Data-in hold time		tDH	1	–	1	–	ns	
Data-in setup time		tDS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	tHZ	–	5	–	5.4	ns	7
	CL = 2		–	8	–	8	ns	
Data-out Low-Z time		tLZ	1	–	1	–	ns	
Data-out hold time (load)		tOH	2.5	–	2.5	–	ns	
Data-out hold time (no load)		tOH*n*	1.8	–	1.8	–	ns	
ACTIVE-to-PRECHARGE command		tRAS	52.5	120,000	52.5	120,000	ns	
ACTIVE-to-ACTIVE command period		tRC	60	–	67.5	–	ns	
ACTIVE-to-READ or WRITE delay		tRCD	18	–	19.2	–	ns	
Refresh period (8192 rows)		tREF	–	64	–	64	ms	8
AUTO REFRESH period		tRFC	72	–	72	–	ns	
PRECHARGE command period		tRP	18	–	19.2	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	2	–	2	–	tCK	
Transition time		tT	0.3	1.2	0.3	1.2	ns	9
WRITE recovery time		tWR	15	–	15	–	ns	10
Exit SELF REFRESH-to-ACTIVE command		tXSR	112.5	–	112.5	–	ns	11

Table 11: AC Functional Characteristics

Notes 1–5 apply to all parameters and conditions

Parameter		Symbol	-6	-75	Unit	Notes
Last data-in to burst STOP command		tBDL	1	1	tCK	12
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	12
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	12
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	13
Data-in to ACTIVE command		tDAL	5	5	tCK	14, 16
Data-in to PRECHARGE command		tDPL	2	2	tCK	15, 16
DQM to input data delay		tDQD	0	0	tCK	12
DQM to data mask during WRITEs		tDQM	0	0	tCK	12
DQM to data High-Z during READs		tDQZ	2	2	tCK	12
WRITE command to input data delay		tDWD	0	0	tCK	12
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	
CKE to clock enable or power-down exit mode		tPED	1	1	tCK	13
Last data-in to PRECHARGE command		tRDL	2	2	tCK	15, 16
Data-out High-Z from PRECHARGE command	CL = 3	tROH	3	3	tCK	12
	CL = 2		2	2	tCK	

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (–40°C ≤ T_A ≤ +85°C industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. Outputs measured for 1.8V at 0.9V with equivalent load:



   Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.
5. AC timing tests have V_{IL} and V_{IH} with timing referenced to $V_{IH/2}$ = crossover point. If the input transition time is longer than tTmax, then the timing is referenced at $V_{IL,max}$ and $V_{IH,min}$ and no longer at the $V_{IH/2}$ crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet tOH before going High-Z.
8. This device requires 8192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8125µs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), one time for every 64ms.
9. AC characteristics assume tT = 1ns. For command and address input slew rates <0.5V/ns, timing must be derated. Input setup times require an additional 50ps for each 100 mV/

ns reduction in slew rate. Input hold times remain unchanged. If the slew rate exceeds 4.5V/ns, functionality is uncertain.

10. For auto precharge mode, the precharge timing budget (^{t}RP) begins at ^{t}RP – (1 × ^{t}CKns), after the first clock delay and after the last WRITE is executed.
11. CLK must be toggled a minimum of two times during this period.
12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by ^{t}CKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by ^{t}WR plus ^{t}RP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by ^{t}WR.
16. Based on ^{t}CK (MIN), CL = 3.

Output Drive Characteristics

Table 12: Target Output Drive Characteristics (Full Strength)

Notes 1–2 apply to all parameters and conditions; characteristics are specified under best and worst process variations/conditions

	Pull-Down Current (mA)		Pull-Up Current (mA)	
Voltage (V)	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	23.80	60.45	–23.80	–60.45
1.90	23.80	61.75	–23.80	–61.75

Notes:
1. Table values based on nominal impedance of 25Ω (full drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.

Table 13: Target Output Drive Characteristics (Three-Quarter Strength)

Notes 1–2 apply to all parameters and conditions; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	–1.96	–12.97
0.20	3.92	18.76	–3.92	–18.76
0.30	5.88	22.96	–5.88	–22.96
0.40	7.84	25.94	–7.84	–25.94
0.50	9.80	28.00	–9.80	–28.00
0.60	11.76	29.75	–11.76	–29.75
0.70	13.72	31.20	–13.72	–31.20
0.80	15.68	32.55	–15.68	–32.55
0.85	16.66	33.24	–16.66	–33.24
0.90	16.66	33.95	–16.66	–33.95
0.95	16.66	34.58	–16.66	–34.58
1.00	16.66	35.04	–16.66	–35.04
1.10	16.66	35.95	–16.66	–35.95
1.20	16.66	36.86	–16.66	–36.86
1.30	16.66	37.77	–16.66	–37.77
1.40	16.66	38.68	–16.66	–38.68
1.50	16.66	39.59	–16.66	–39.59
1.60	16.66	40.50	–16.66	–40.50
1.70	16.66	41.41	–16.66	–41.41
1.80	16.66	42.32	–16.66	–42.32
1.90	16.66	43.23	–16.66	–43.23

Notes:
1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.

Table 14: Target Output Drive Characteristics (One-Half Strength)

Notes 1–3 apply to all parameters and conditions; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	10.80	26.48	–10.80	–26.48
1.90	10.80	26.95	–10.80	–26.95

Notes:
1. Table values based on nominal impedance of 55Ω (one-half drive strength) at $V_{DDQ/2}$.
2. The full variation in drive current, from minimum to maximum (due to process, voltage, and temperature) will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50% of one-half drive strength.

Functional Description

Mobile LPSDR devices are quad-bank DRAM that operate at 1.8V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK.

Read and write accesses to the device are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The device provides for programmable READ or WRITE burst lengths. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The device uses an internal pipelined architecture that enables changing the column address on every clock cycle to achieve high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles.

The device is designed to operate in 1.8V memory systems. An auto refresh mode is provided, along with power-saving, power-down, and deep power-down modes. All inputs and outputs are LVTTL-compatible.

The device offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Commands

The following table provides a quick reference of available commands, followed by a written description of each command. Additional Truth Tables (Table 16 (page 33), Table 17 (page 35), and Table 18 (page 37)) provide current state/next state information.

Table 15: Truth Table – Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE or deep power-down (enter deep power-down mode)	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	6
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	7, 8
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	9
Write enable/output enable	X	X	X	X	L	X	Active	10
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	10

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
5. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
6. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
9. A[11:0] define the op-code written to the mode register.
10. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the device, regardless of whether the CLK signal is enabled. The device is effectively de-selected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to the selected device (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

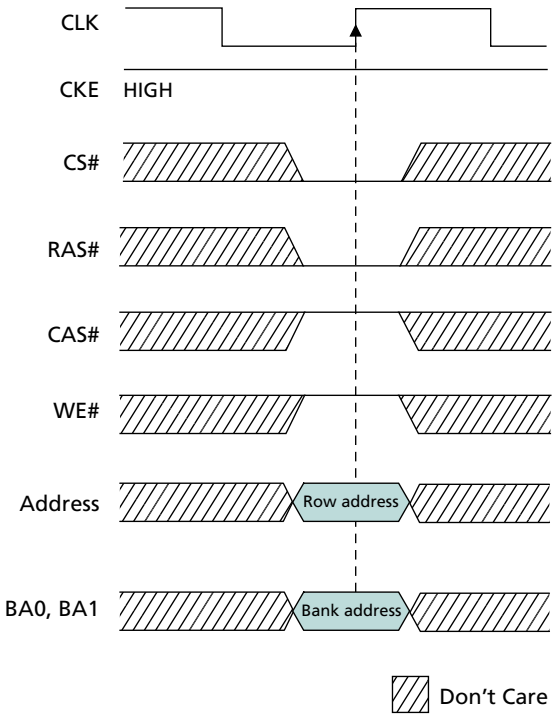
LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A[*n:0]* (where A*n* is the most significant address term), BA0, and BA1(see Mode Register (page 40)). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

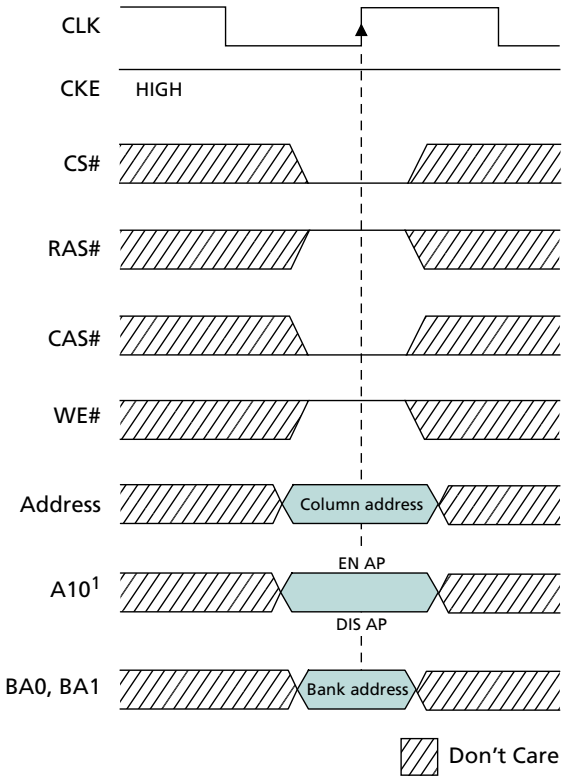
Figure 8: ACTIVE Command



READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

Figure 9: READ Command

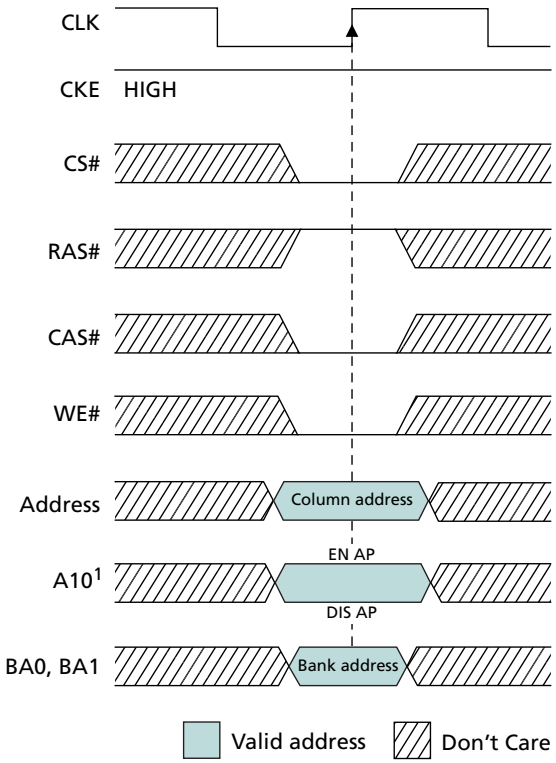


Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array, subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location.

Figure 10: WRITE Command

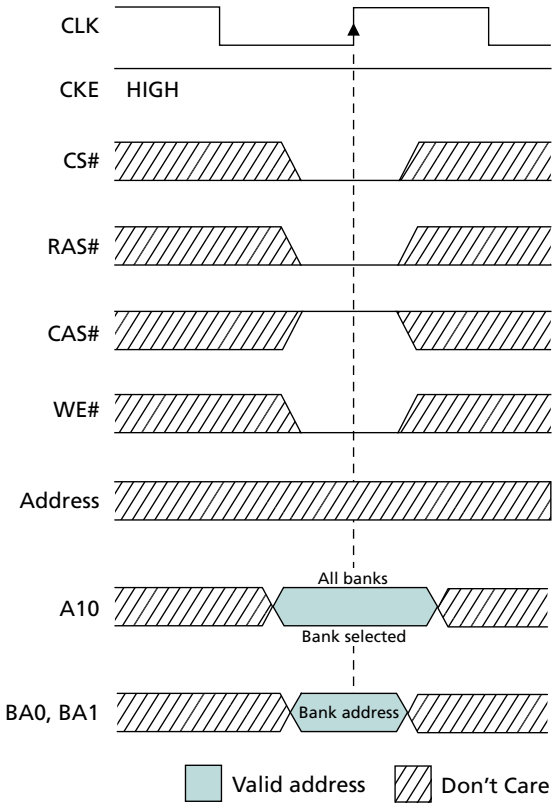


Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands are issued to that bank.

Figure 11: PRECHARGE Command



BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command is truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAM. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

SELF REFRESH

The SELF REFRESH command is used to place the device in self refresh mode. The self refresh mode is used to retain data in the SDRAM while the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). After the SELF REFRESH command is registered, the inputs become “Don’t Care,” with the exception of CKE, which must remain LOW.

DEEP POWER-DOWN

The DEEP POWER-DOWN (DPD) command is used to enter deep power-down mode, achieving maximum power reduction by eliminating the power to the memory array. To enter DPD, all banks must be idle. While CKE is LOW, hold CS# and WE# LOW, and hold RAS# and CAS# HIGH at the rising edge of the clock. To exit DPD, assert CKE HIGH.

Truth Tables

Table 16: Truth Table – Current State Bank *n*, Command to Bank *n*

Notes 1–6 apply to all parameters and conditions

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	8
Row active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	10
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	9, 11
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	9, 11

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 18 (page 37)) and after ^{t}XSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown can be issued to that bank when in that state). Exceptions are covered below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to any other bank are determined by the bank's current state and the conditions described in this and the following table.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. After ^{t}RP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. After ^{t}RCD is met, the bank will be in the row active state.

Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the device will be in the all banks idle state.

   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the device will be in the all banks idle state.

   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank specific; requires that all banks are idle.
8. Does not affect the state of the bank and acts as a NOP to that bank.
9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. May or may not be bank specific; if all banks need to be precharged, each must be in a valid state for precharging.
11. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.

Table 17: Truth Table – Current State Bank n, Command to Bank *m*

Notes 1–6 apply to all parameters and conditions

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise supported for bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 12
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (Table 18 (page 37)), and after ^{t}XSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; for example, the current state is for bank *n* and the commands shown can be issued to bank *m*, assuming that bank *m* is in such a state that the given command is supported. Exceptions are covered below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands can only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
9. The burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency (CL) later.
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Table 18: Truth Table – CKE

Notes 1–4 apply to all parameters and conditions

Current State	CKE_{n-1}	CKE_n	$Command_n$	$Action_n$	Notes
Power-down	L	L	X	Maintain power-down	
Self refresh			X	Maintain self refresh	
Clock suspend			X	Maintain clock suspend	
Deep power-down			X	Maintain deep power-down	
Power-down	L	H	COMMAND INHIBIT or NOP	Exit power-down	5
Deep power-down			X	Exit deep power-down	
Self refresh			COMMAND INHIBIT or NOP	Exit self refresh	6
Clock suspend			X	Exit clock suspend	7
All banks idle	H	L	COMMAND INHIBIT or NOP	Power-down entry	
All banks idle			BURST TERMINATE	Deep power-down entry	8
All banks idle			AUTO REFRESH	Self refresh entry	
Reading or writing			VALID	Clock suspend entry	
	H	H	Table 17 (page 35)		

Notes:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^tCKS is met).
6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state after ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during the ^tXSR period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.
8. Deep power-down is a power-saving feature of this device. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.

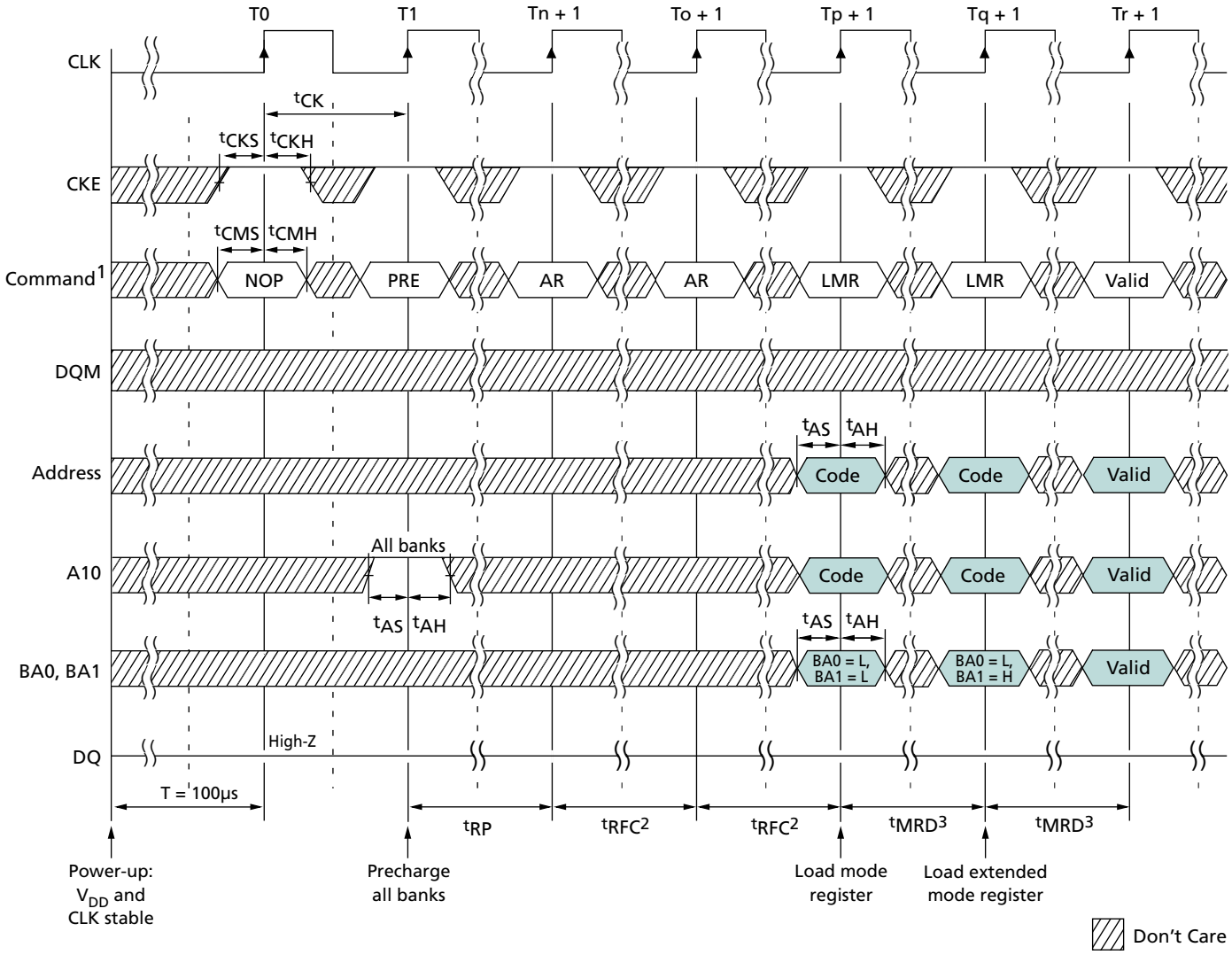
Initialization

Low-power SDRAM devices must be powered up and initialized in a predefined manner. Using initialization procedures other than those specified may result in undefined operation. After power is simultaneously applied to V_{DD} and V_{DDQ} and the clock is stable (a stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the device requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

After the 100µs delay is satisfied by issuing at least one COMMAND INHIBIT or NOP command, a PRECHARGE command must be issued. All banks must then be precharged, which places the device in the all banks idle state.

When in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the device is ready for mode register programming. Because the mode register powers up in an unknown state, it should be loaded prior to issuing any operational command.

Figure 12: Initialize and Load Mode Register



Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. NOPs or DESELECTs must only be provided during ^{t}RFC time.
3. NOPs or DESELECTs must only be provided during ^{t}MRD time.

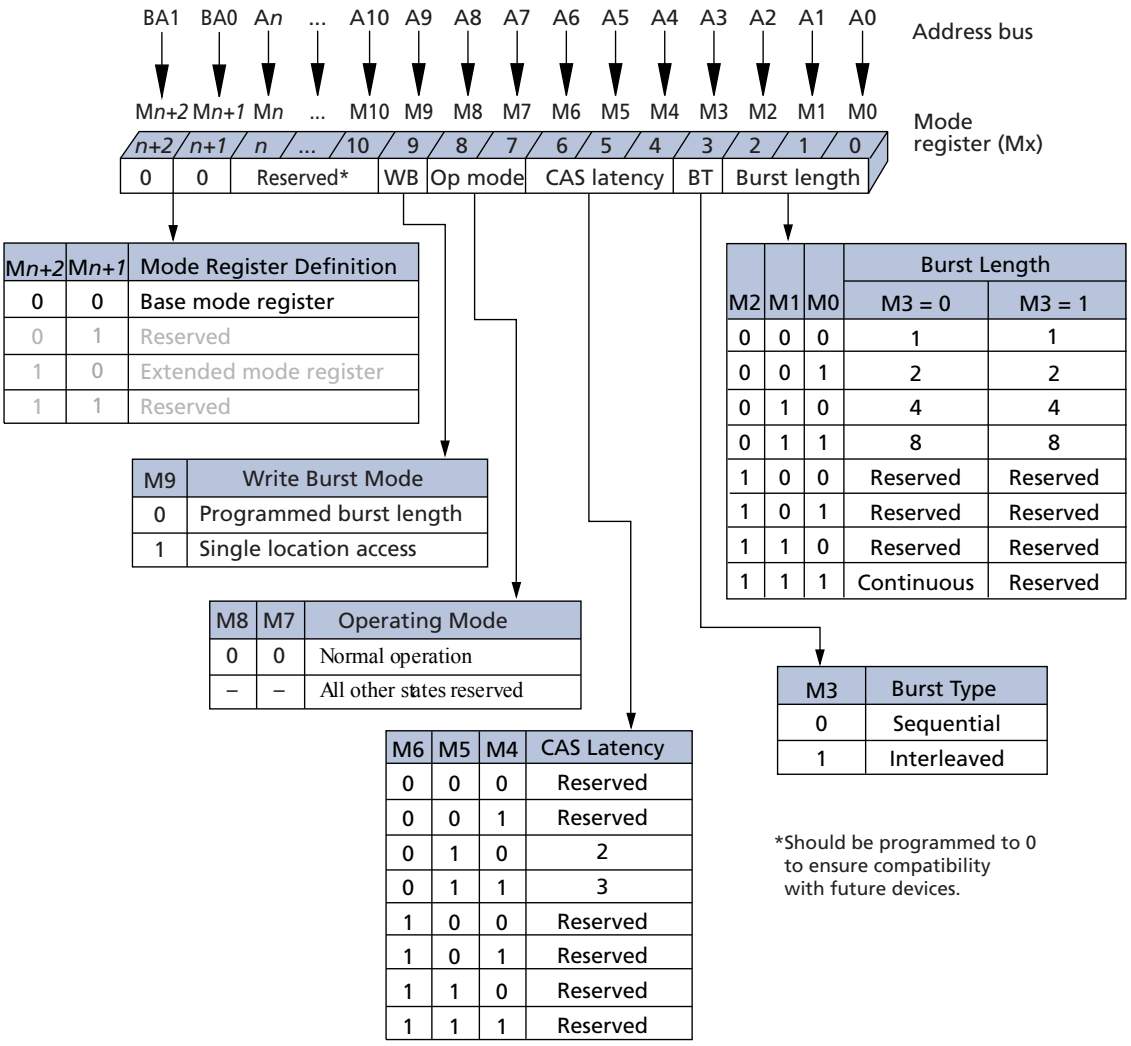
Mode Register

The mode register defines the specific mode of operation, including burst length (BL), burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and retains the stored information until it is programmed again or the device loses power.

Mode register bits M[2:0] specify the BL; M3 specifies the type of burst; M[6:4] specify the CL; M7 and M8 specify the operating mode; M9 specifies the write burst mode; and M10–M*n* should be set to zero to ensure compatibility with future revisions. M*n* + 1 and M*n* + 2 should be set to zero to select the mode register.

The mode registers must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 13: Mode Register Definition



Mn+2	Mn+1	Mode Register Definition
0	0	Base mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	Operating Mode
0	0	Normal operation
–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M2	M1	M0	Burst Length M3 = 0	Burst Length M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Continuous	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Burst Length

Read and write accesses to the device are burst oriented, and the burst length (BL) is programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, 8, or continuous locations are available for both the sequential and the interleaved burst types, and a continuous page burst is available for the sequential type. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block when a boundary is reached. The block is uniquely selected by A[8:1] when BL = 2, A[8:2] when BL = 4, and A[8:3] when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Continuous page bursts wrap within the page when the boundary is reached.

Burst Type

Accesses within a given burst can be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address.

Table 19: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Continuous					
	n = A0–An/9/8 (location 0–y)			Cn, Cn + 1, Cn + 2, Cn + 3...Cn - 1, Cn...	Not supported

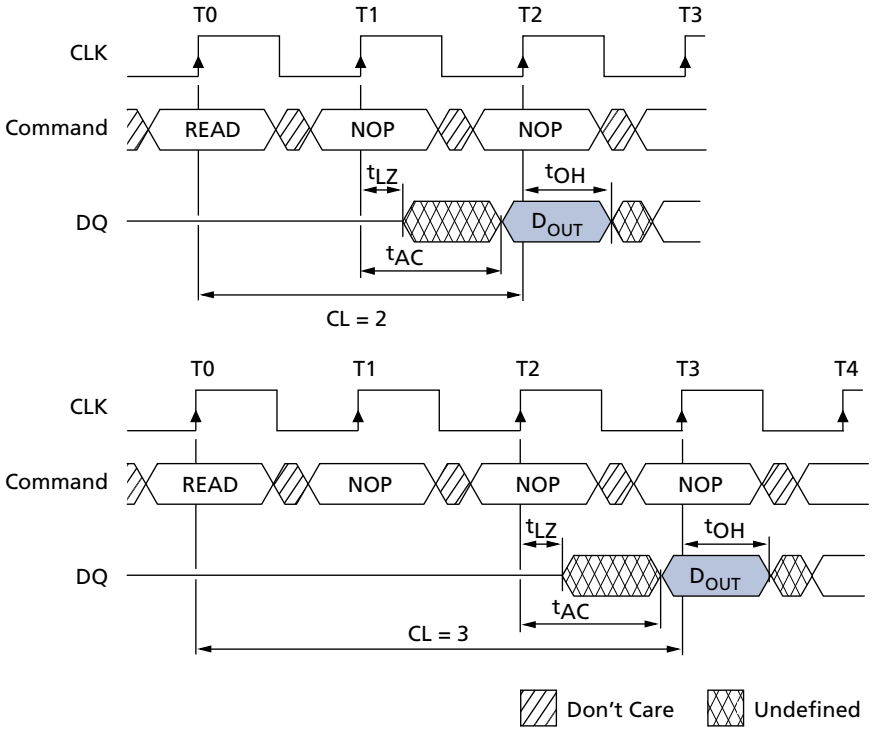
CAS Latency

The CAS latency (CL) is the delay, in clock cycles, between the registration of a READ command and the availability of the output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQ start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data is valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQ start driving after T1 and the data is valid by T2.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 14: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M[2:0] applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

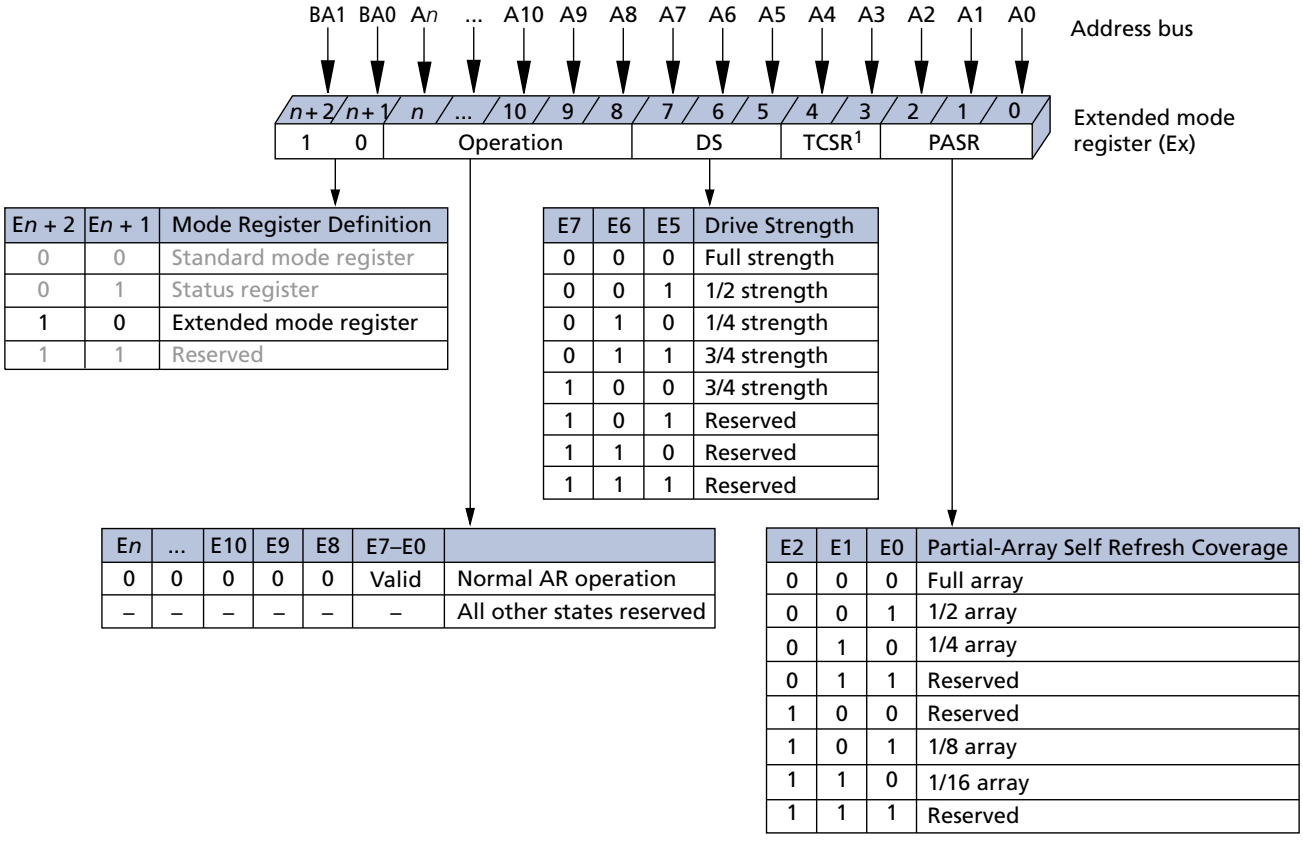
Extended Mode Register

The extended mode register (EMR) controls additional functions beyond those controlled by the mode register. These additional functions include TCSR, PASR, and output drive strength.

The EMR is programmed via the LMR command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

The EMR must be programmed with E[*n:7]* set to 0. It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. After the values are entered, the EMR settings are retained even after exiting deep power-down mode.

Figure 15: Extended Mode Register Definition



En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Drive Strength
0	0	0	Full strength
0	0	1	1/2 strength
0	1	0	1/4 strength
0	1	1	3/4 strength
1	0	0	3/4 strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal AR operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	1/2 array
0	1	0	1/4 array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array
1	1	0	1/16 array
1	1	1	Reserved

Note: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

Temperature-Compensated Self Refresh

This device includes a temperature sensor that is implemented for automatic control of the self refresh oscillator. Programming the temperature-compensated self refresh (TCSR) bits has no effect on the device. The self refresh oscillator will continue refresh at the optimal factory-programmed rate for the device temperature.

Partial-Array Self Refresh

For further power savings during self refresh, the partial-array self refresh (PASR) feature enables the controller to select the amount of memory to be refreshed during self refresh. The refresh options are:

- Full array: banks 0, 1, 2, and 3
- One-half array: banks 0 and 1
- One-quarter array: bank 0
- One-eighth array: bank 0 with row address most significant bit (MSB) = 0
- One-sixteenth array: bank 0 with row address MSB = 0 and row address MSB - 1 = 0

READ and WRITE commands can still be issued to any bank selected during standard operation, but only the selected banks or segments of a bank in PASR are refreshed during self refresh. It is important to note that data in unused banks or portions of banks is lost when PASR is used.

Output Drive Strength

Because the device is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: 25Ω, 37Ω, 55Ω, and 80Ω internal impedance. These are full, three-quarter, one-half, and one-quarter drive strengths, respectively.

Bank/Row Activation

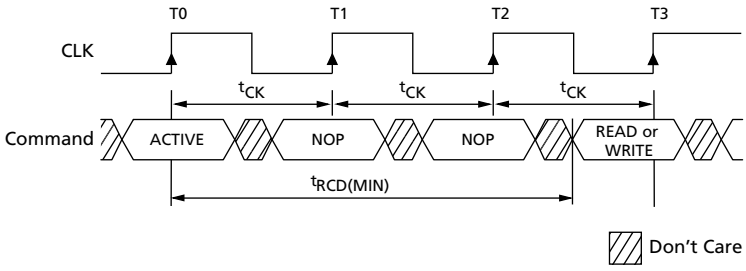
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with the ACTIVE command, a READ or WRITE command can be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 16 (page 46), which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been precharged. The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 16: Example: Meeting ^{t}RCD (MIN) When $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$



READ Operation

READ bursts are initiated with a READ command, as shown in Figure 9 (page 29). The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. In the following figures, auto precharge is disabled.

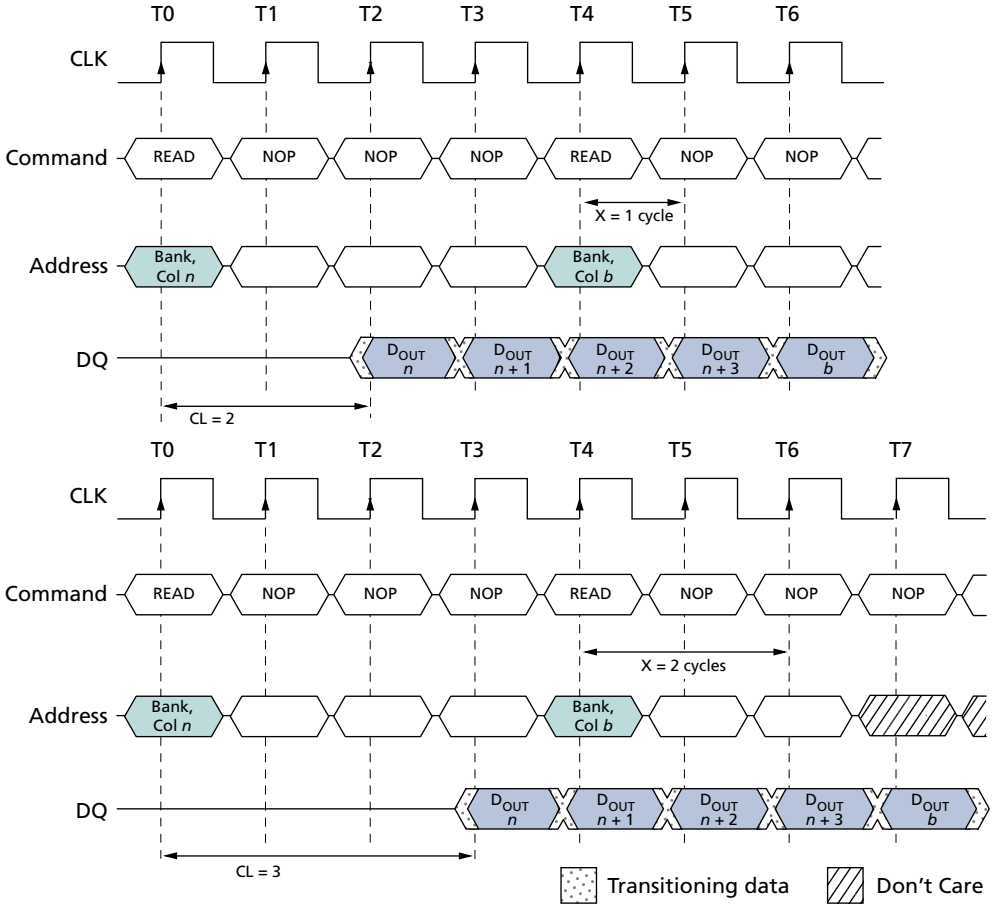
During READ bursts, the valid data-out element from the starting column address is available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 18 (page 49) shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ signals will go to High-Z. A continuous page burst continues until terminated. At the end of the page, it wraps to column 0 and continues.

Data from any READ burst can be truncated with a subsequent READ command, and data from a fixed-length READ burst can be followed immediately by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 18 (page 49) for CL2 and CL3.

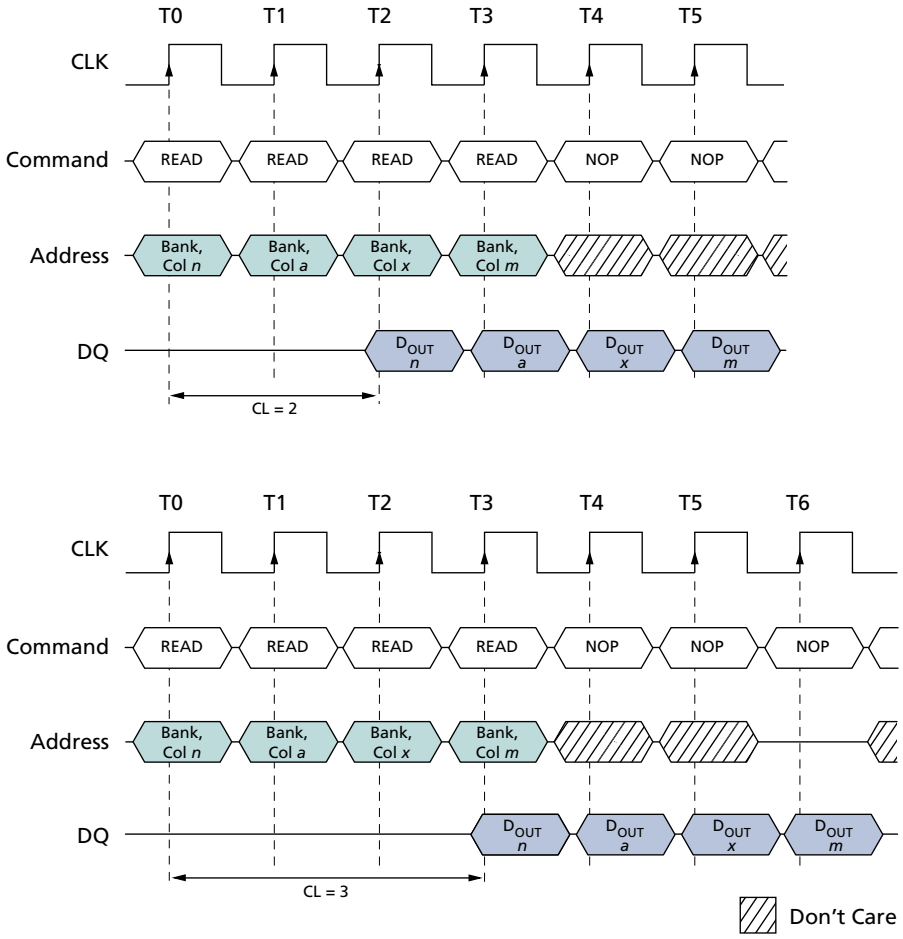
Mobile LPSDR devices use a pipelined architecture and therefore do not require the $2n$ rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a READ command. Full-speed random read accesses can be performed to the same bank, or each subsequent READ can be performed to a different bank.

Figure 17: Consecutive READ Bursts



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

Figure 18: Random READ Accesses



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

Data from any READ burst can be truncated with a subsequent WRITE command, and data from a fixed-length READ burst can be followed immediately by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst can be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there is a possibility that the device driving the input data will go Low-Z before the DQ go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

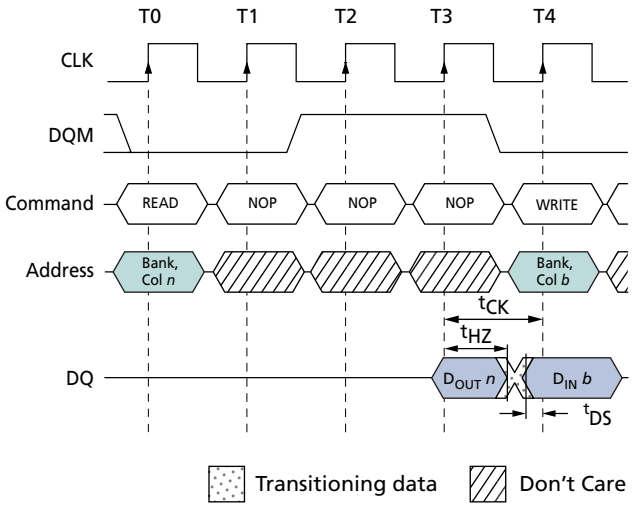
The DQM input is used to avoid I/O contention, as shown in Figure 19 (page 50) and Figure 20 (page 51). The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. After the WRITE command is registered, the DQ will go to High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4, then the WRITEs at T5 and T7 would be valid, and the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 19 (page 50) shows where, due to the clock cycle frequency, bus contention is avoided without having to add a NOP cycle, while Figure 20 (page 51) shows the case where an additional NOP cycle is required.

A fixed-length READ burst may be followed by or truncated with a PRECHARGE command to the same bank, provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 21 (page 51) for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

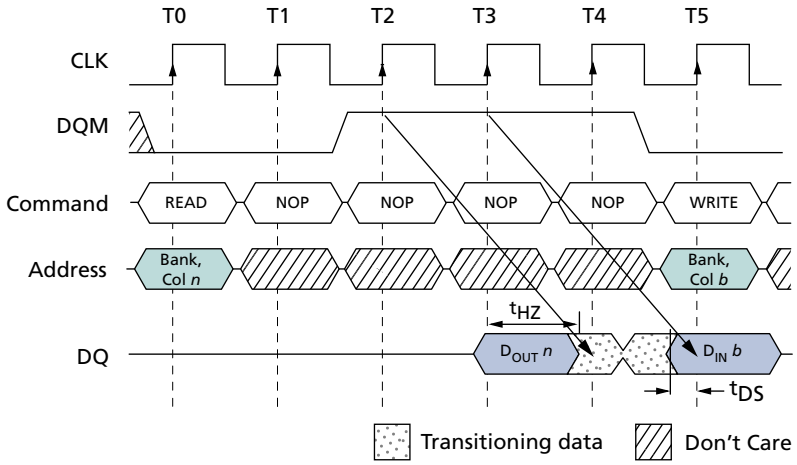
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate fixed-length or continuous page bursts.

Figure 19: READ-to-WRITE



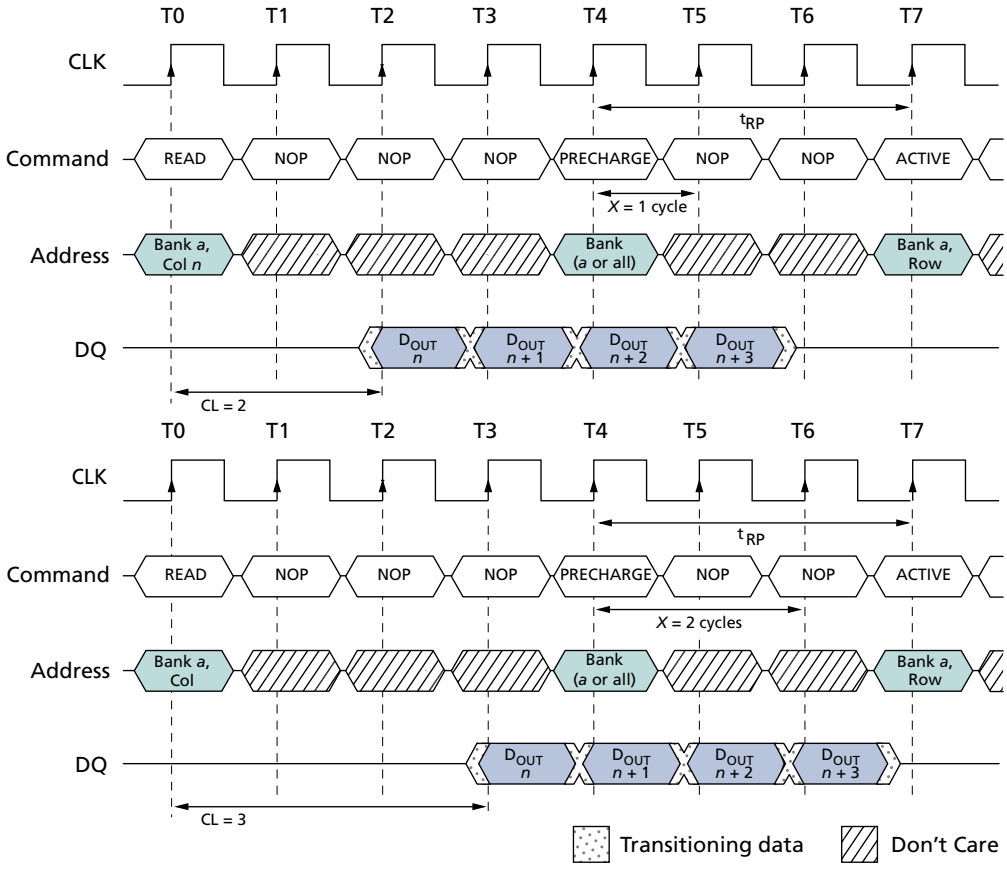
Note: 1. CL = 3. The READ command can be issued to any bank, and the WRITE command can be to any bank. If a burst of one is used, DQM is not required.

Figure 20: READ-to-WRITE With Extra Clock Cycle



Note: 1. CL = 3. The READ command can be issued to any bank, and the WRITE command can be to any bank.

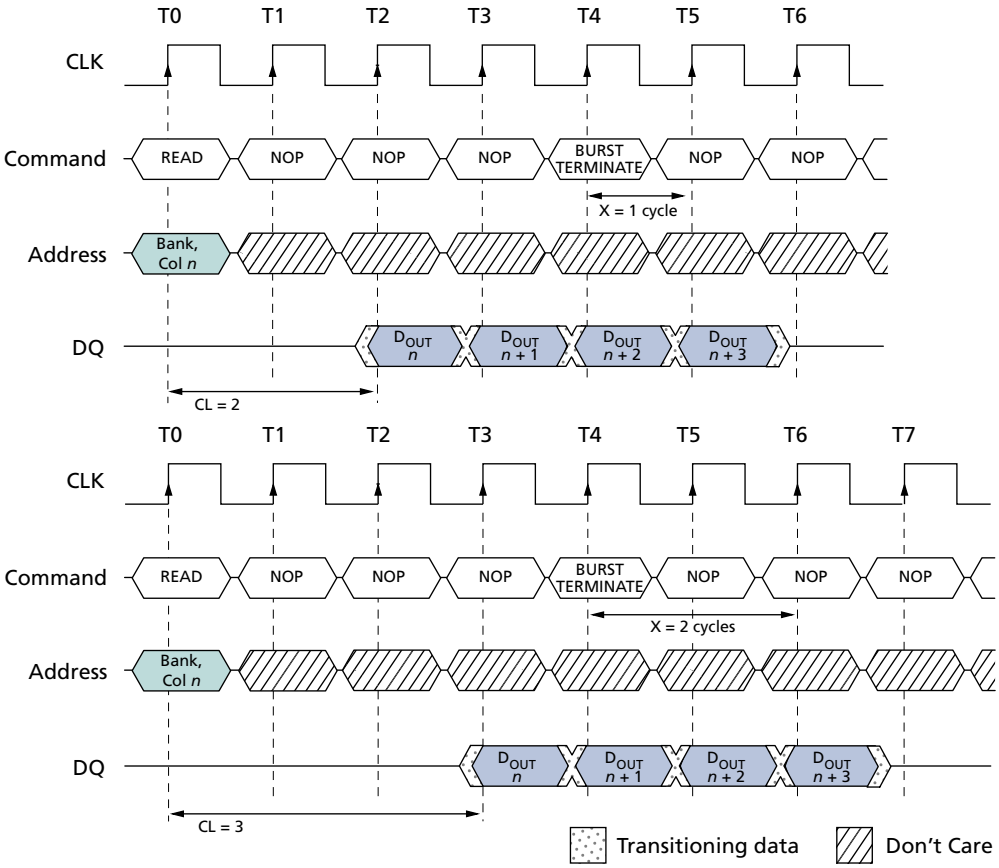
Figure 21: READ-to-PRECHARGE



Note: 1. DQM is LOW.

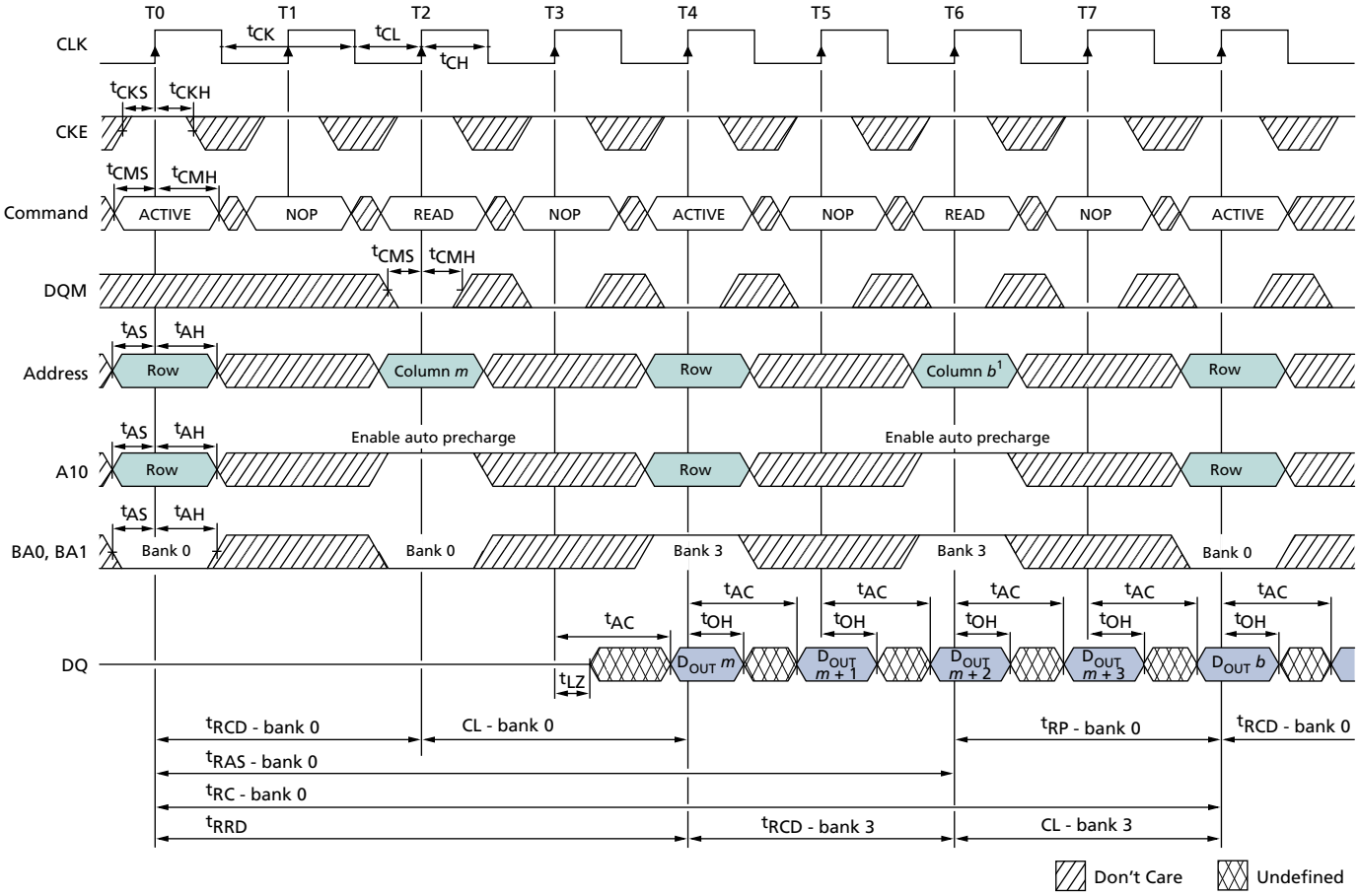
Continuous-page READ bursts can be truncated with a BURST TERMINATE command and fixed-length READ bursts can be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 22 (page 52) for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

Figure 22: Terminating a READ Burst



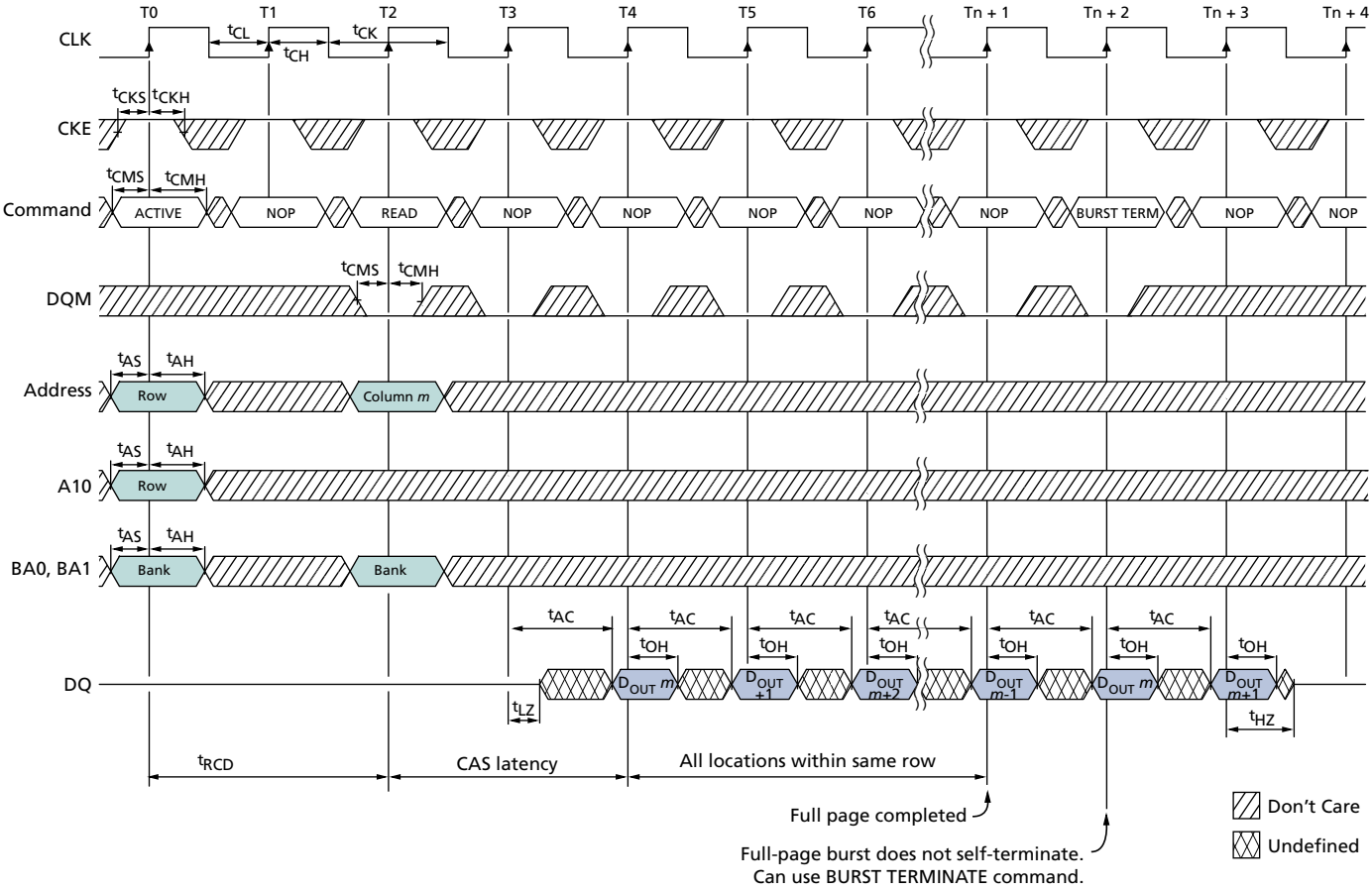
Note: 1. DQM is LOW.

Figure 23: Alternating Bank Read Accesses



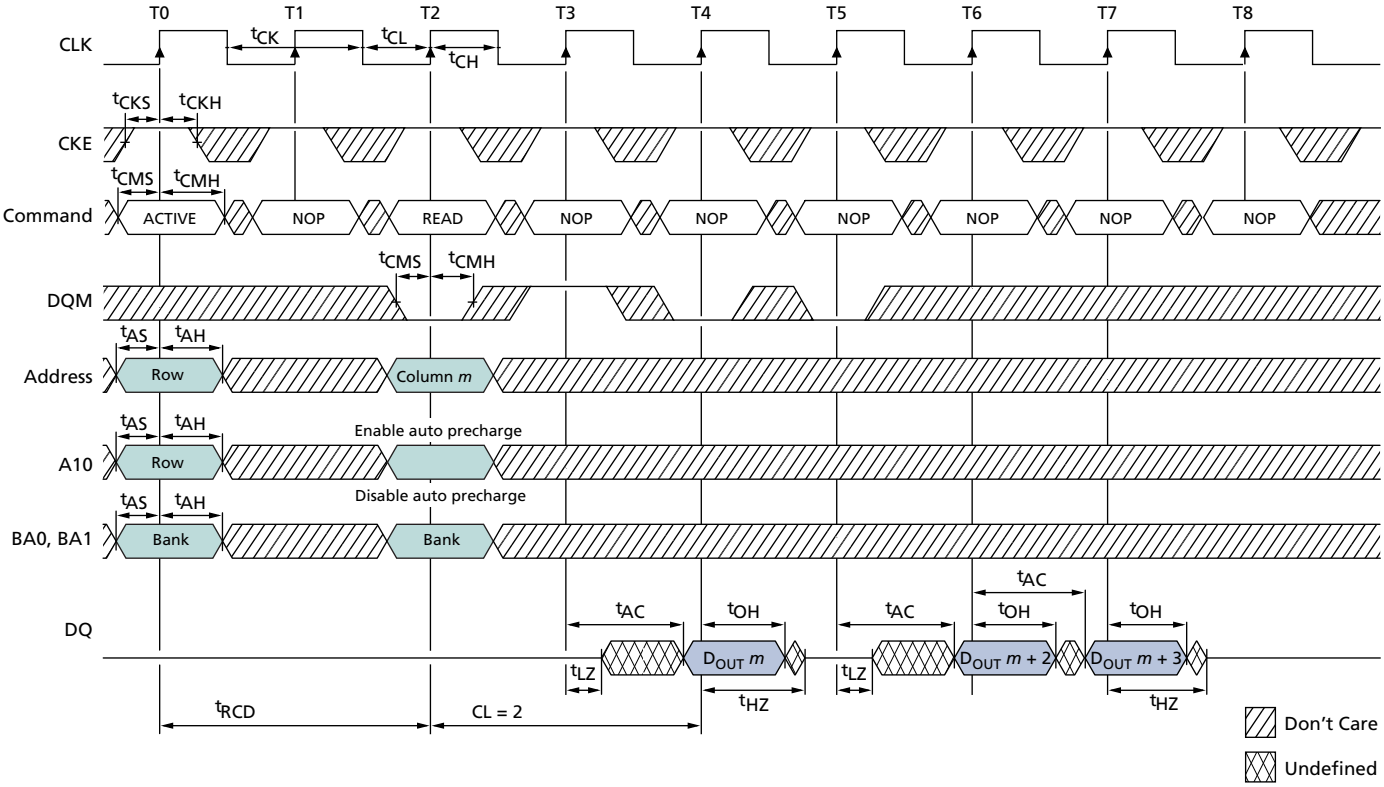
Note: 1. For this example, BL = 4 and CL = 2.

Figure 24: READ Continuous Page Burst



Note: 1. For this example, CL = 2.

Figure 25: READ – DQM Operation



Note: 1. For this example, BL = 4 and CL = 2.

WRITE Operation

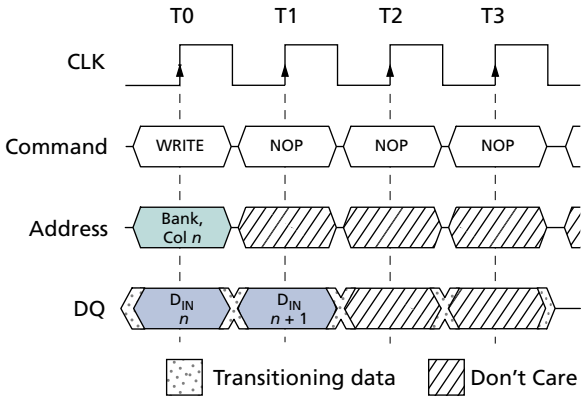
WRITE bursts are initiated with a WRITE command, as shown in Figure 10 (page 30). The starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following figures, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command. Subsequent data elements are registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain at High-Z and any additional input data will be ignored (see Figure 26 (page 56)). A continuous page burst continues until terminated; at the end of the page, it wraps to column 0 and continues.

Data for any WRITE burst can be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst can be followed immediately by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command (see Figure 27 (page 57)). Data $n + 1$ is either the last of a burst of two or the last desired data element of a longer burst.

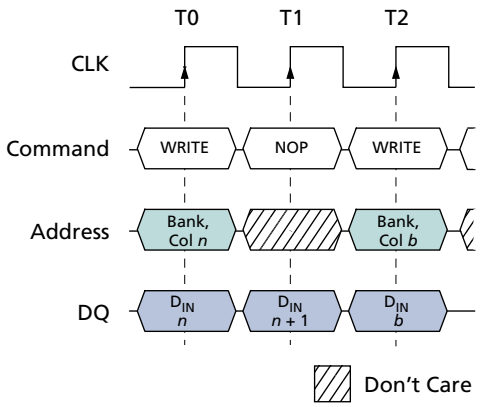
Mobile LPSDR devices use a pipelined architecture and therefore do not require the $2n$ rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 28 (page 58), or each subsequent WRITE can be performed to a different bank.

Figure 26: WRITE Burst



Note: 1. BL = 2. DQM is LOW.

Figure 27: WRITE-to-WRITE



Note: 1. DQM is LOW. Each WRITE command may be issued to any bank.

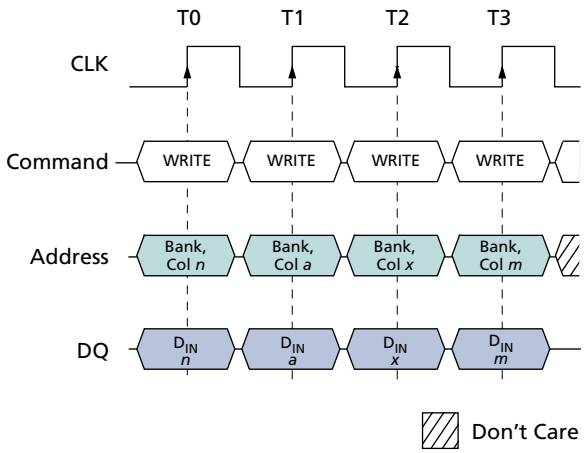
Data for any WRITE burst can be truncated with a subsequent READ command, and data for a fixed-length WRITE burst can be followed immediately by a READ command. After the READ command is registered, data input is ignored and WRITEs will not be executed (see Figure 29 (page 58)). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst.

Data for a fixed-length WRITE burst can be followed by or truncated with a PRECHARGE command to the same bank, provided that auto precharge was not activated. A continuous-page WRITE burst can be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock with time to complete, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to and the clock edge coincident with the PRECHARGE command (see Figure 30 (page 59)). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

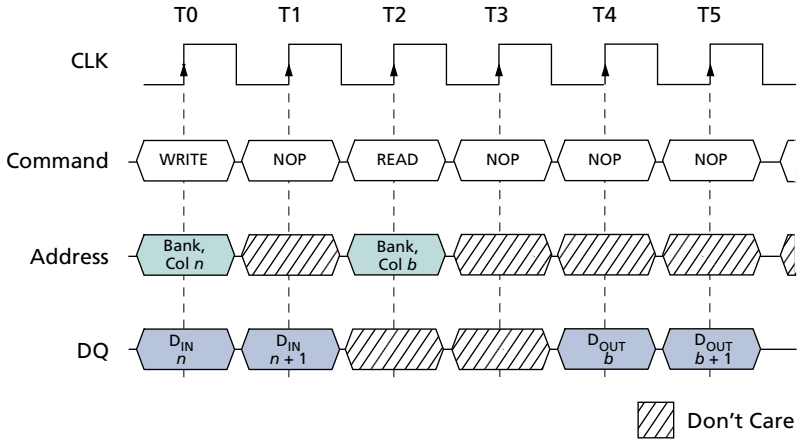
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts or continuous page bursts.

Figure 28: Random WRITE Cycles



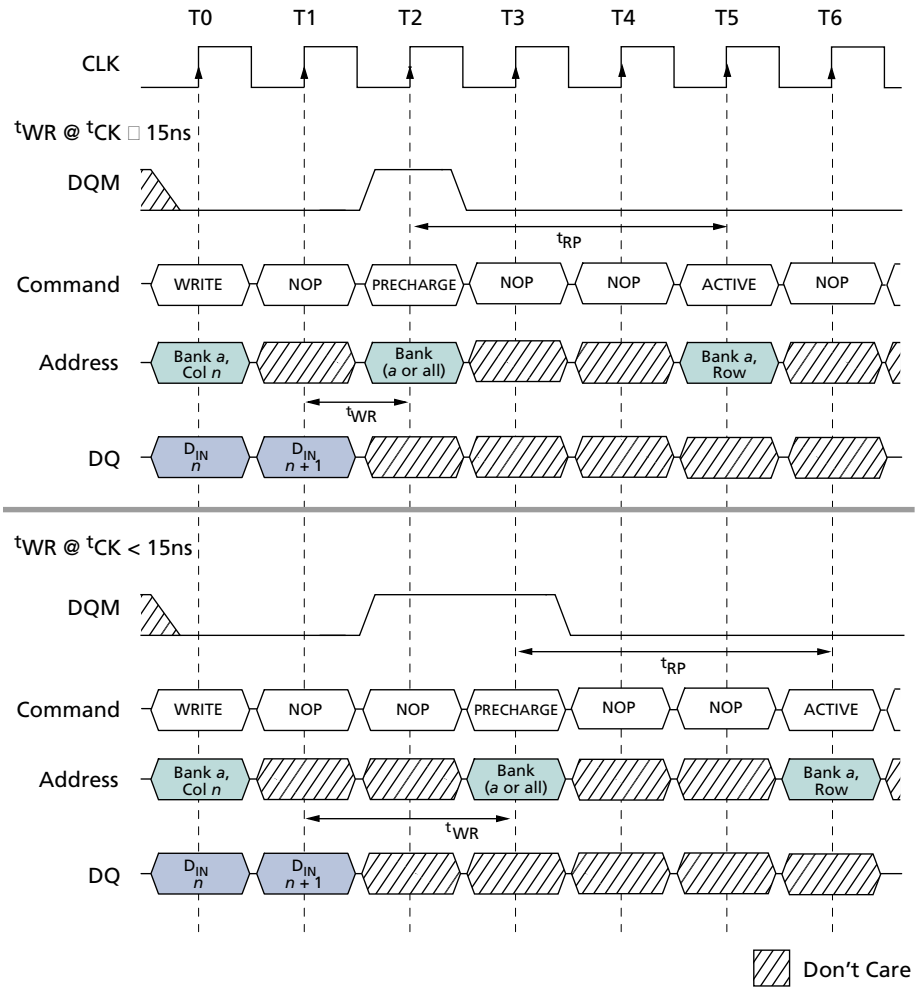
Note: 1. Each WRITE command can be issued to any bank. DQM is LOW.

Figure 29: WRITE-to-READ



Note: 1. The WRITE command can be issued to any bank, and the READ command can be to any bank. DQM is LOW. CL = 2 for illustration.

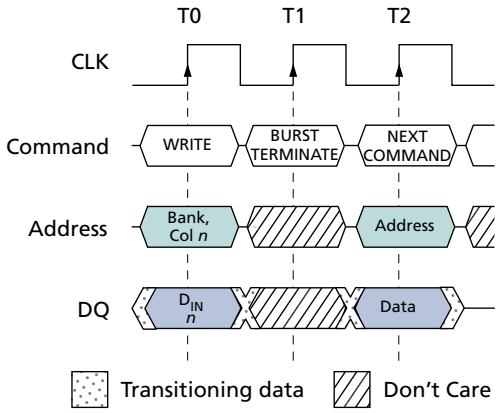
Figure 30: WRITE-to-PRECHARGE



Note: 1. In this example DQM could remain LOW if the WRITE burst is a fixed length of two.

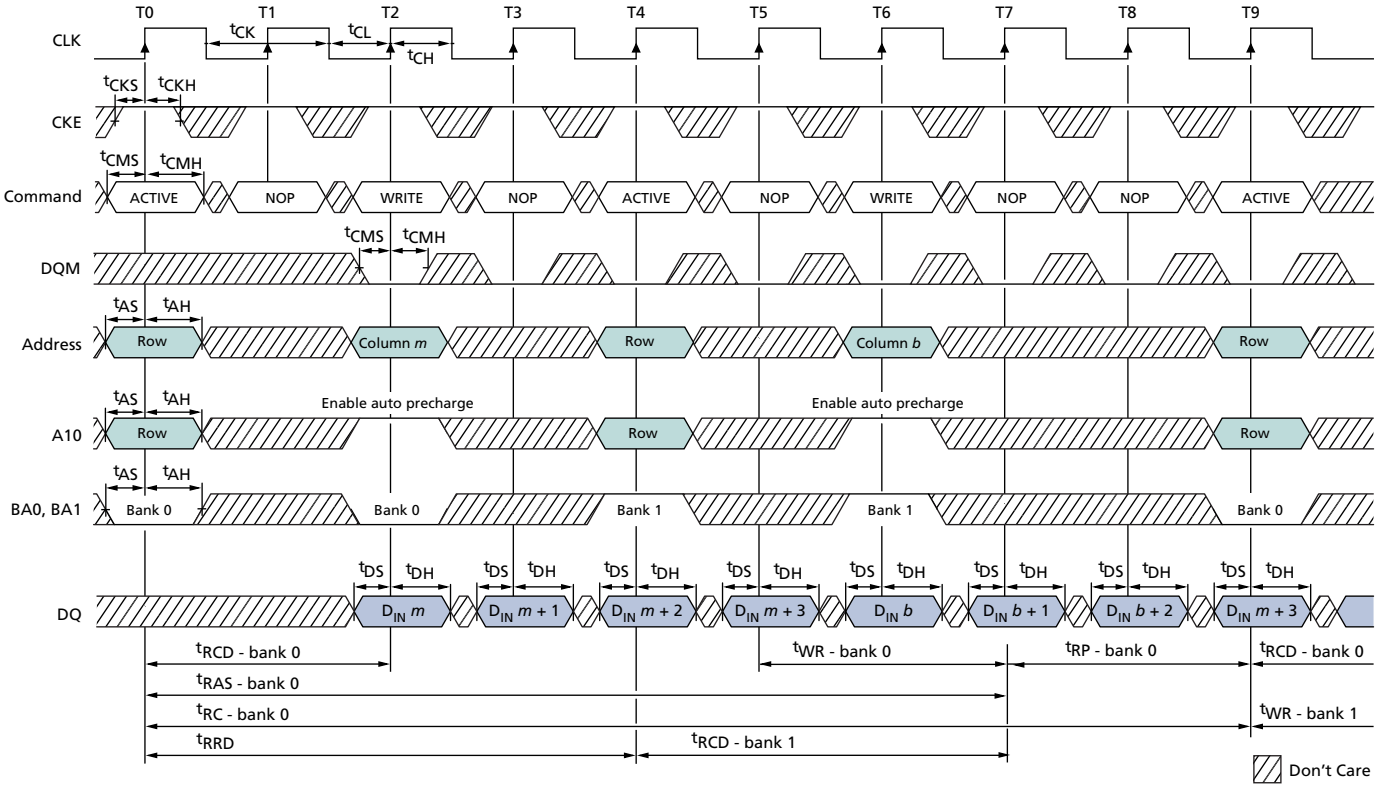
Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command is ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 31 (page 60), where data *n* is the last desired data element of a longer burst.

Figure 31: Terminating a WRITE Burst



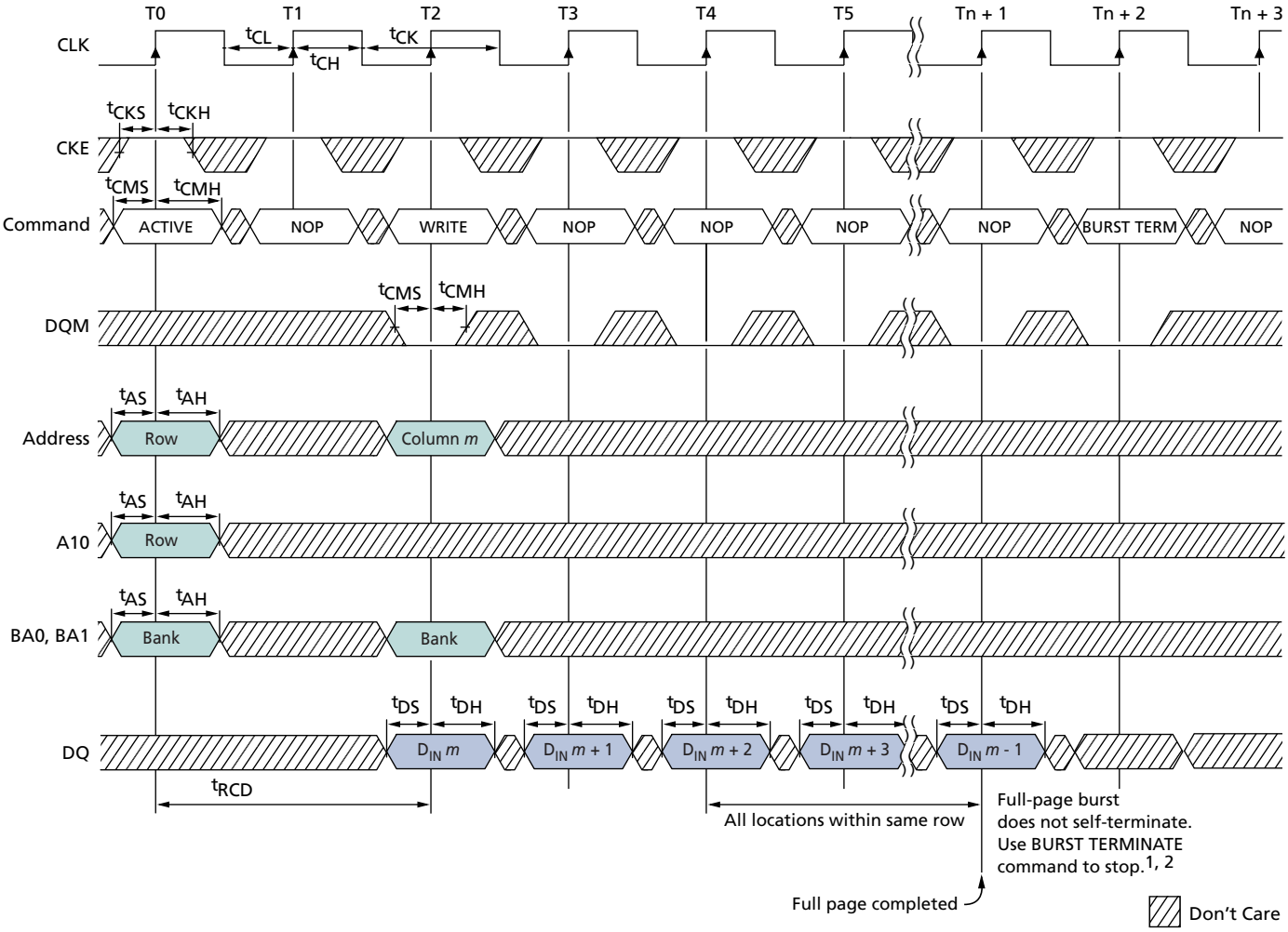
Note: 1. DQM is LOW.

Figure 32: Alternating Bank Write Accesses



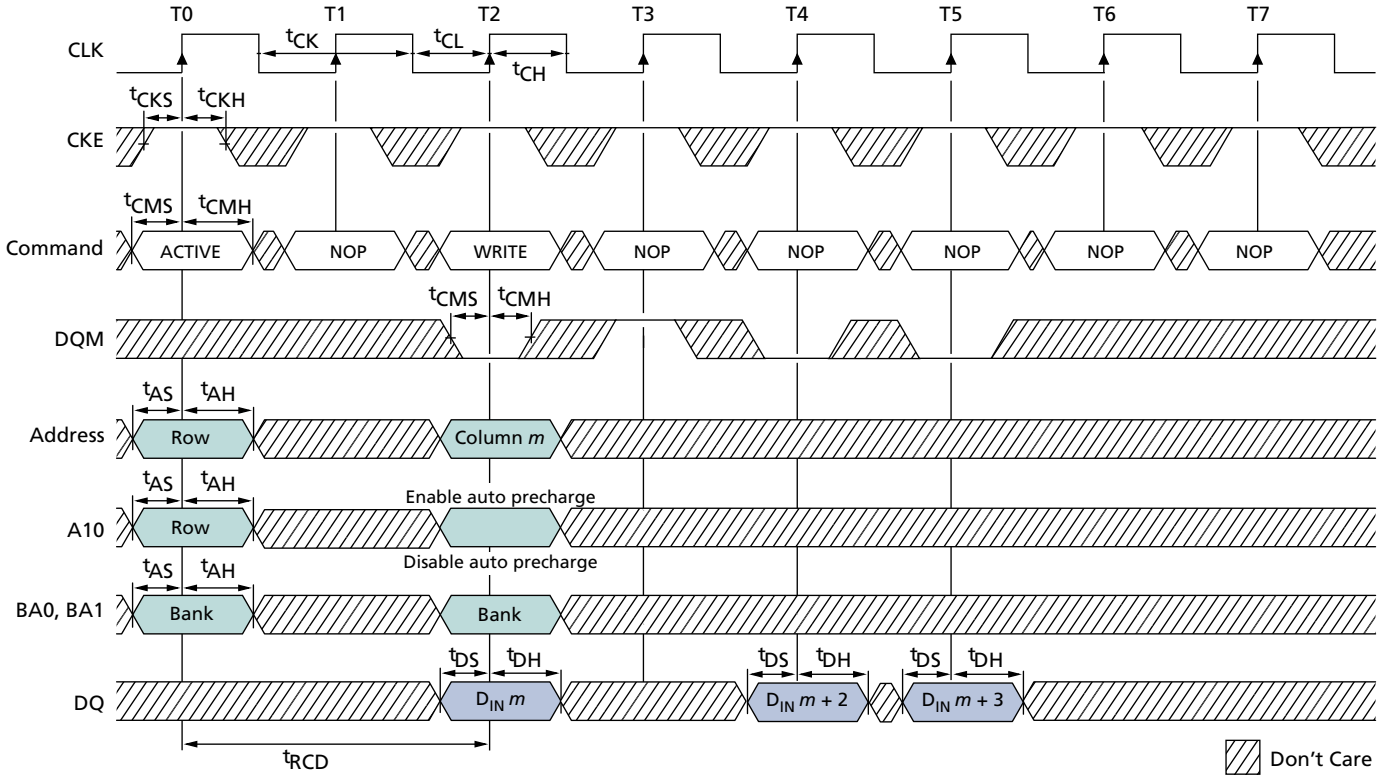
Note: 1. For this example, BL = 4.

Figure 33: WRITE – Continuous Page Burst



Notes:
1. tWR must be satisfied prior to issuing a PRECHARGE command.
2. Page left open; no tRP.

Figure 34: WRITE – DQM Operation



Note: 1. For this example, BL = 4.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

PRECHARGE Operation

The PRECHARGE command (see Figure 11 (page 31)) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged (A10 = LOW), inputs BA0 and BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described previously, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the continuous page burst mode where auto precharge does not apply. In the specific case of write burst mode set to single location access with burst length set to continuous, the burst length setting is the overriding setting and auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. Another command cannot be issued to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Burst Type (page 41) section.

This device supports ^{t}RAS lock-out. In the case of a single READ with auto precharge, or a single WRITE with auto precharge, issued at ^{t}RCD (MIN), the internal precharge will be delayed until ^{t}RAS (MIN) has been satisfied.

Micron SDRAM supports concurrent auto precharge; cases of concurrent auto precharge for READs and WRITEs are defined below.

READ with auto precharge interrupted by a READ (with or without auto precharge)

A READ to bank *m* will interrupt a READ on bank *n* following the programmed CAS latency. The precharge to bank *n* begins when the READ to bank *m* is registered (see Figure 35 (page 65)).

READ with auto precharge interrupted by a WRITE (with or without auto precharge)

A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* begins when the WRITE to bank *m* is registered (see Figure 36 (page 66)).

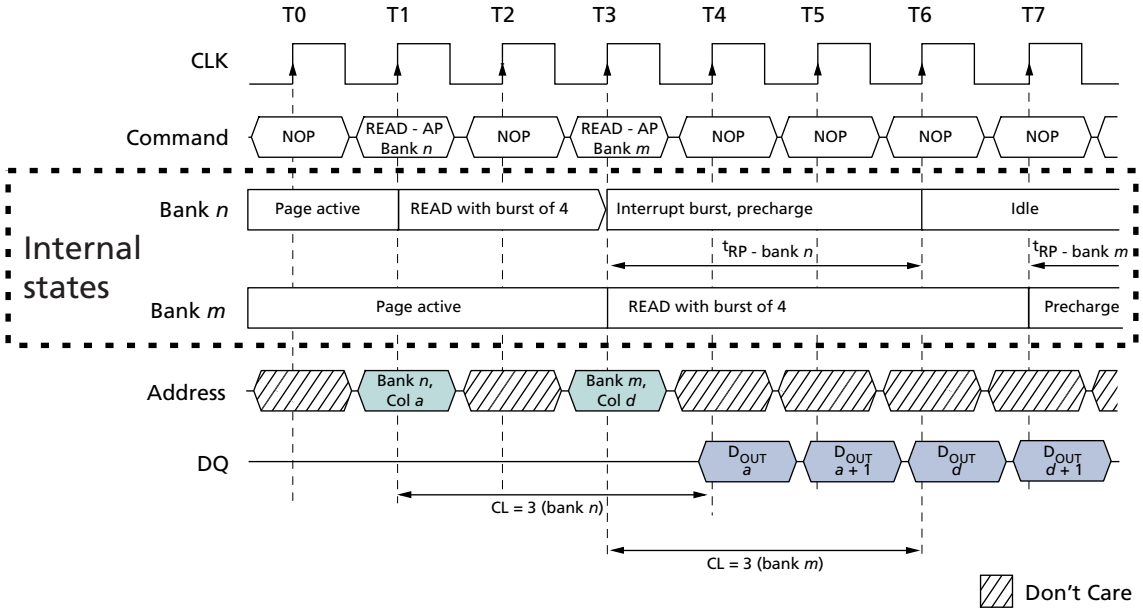
WRITE with auto precharge interrupted by a READ (with or without auto precharge)

A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 41 (page 71)).

WRITE with auto precharge interrupted by a WRITE (with or without auto precharge)

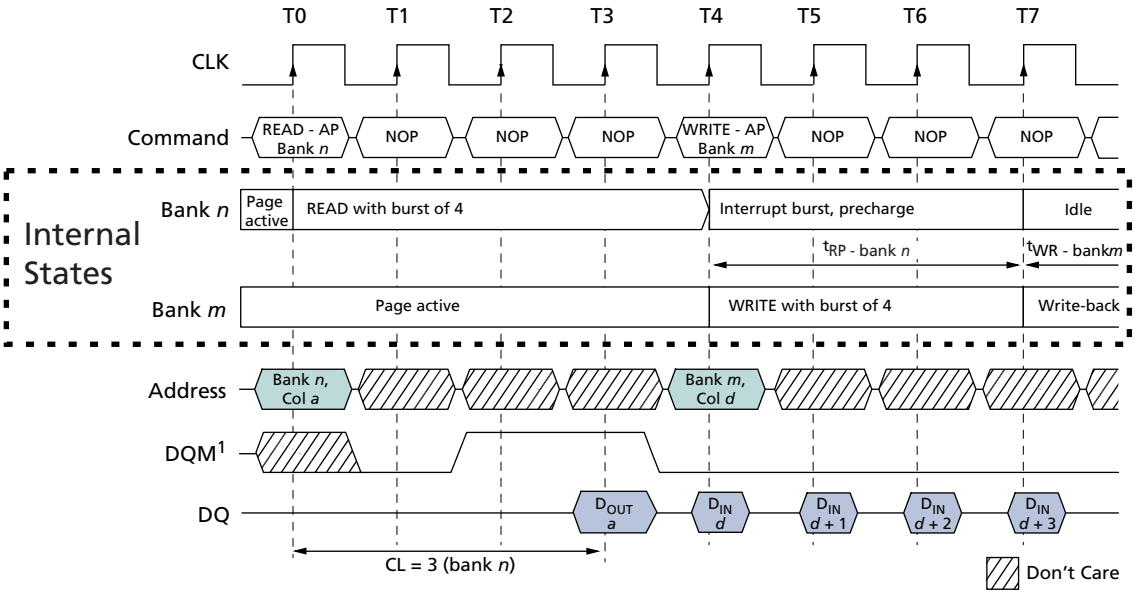
A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 42 (page 71)).

Figure 35: READ With Auto Precharge Interrupted by a READ



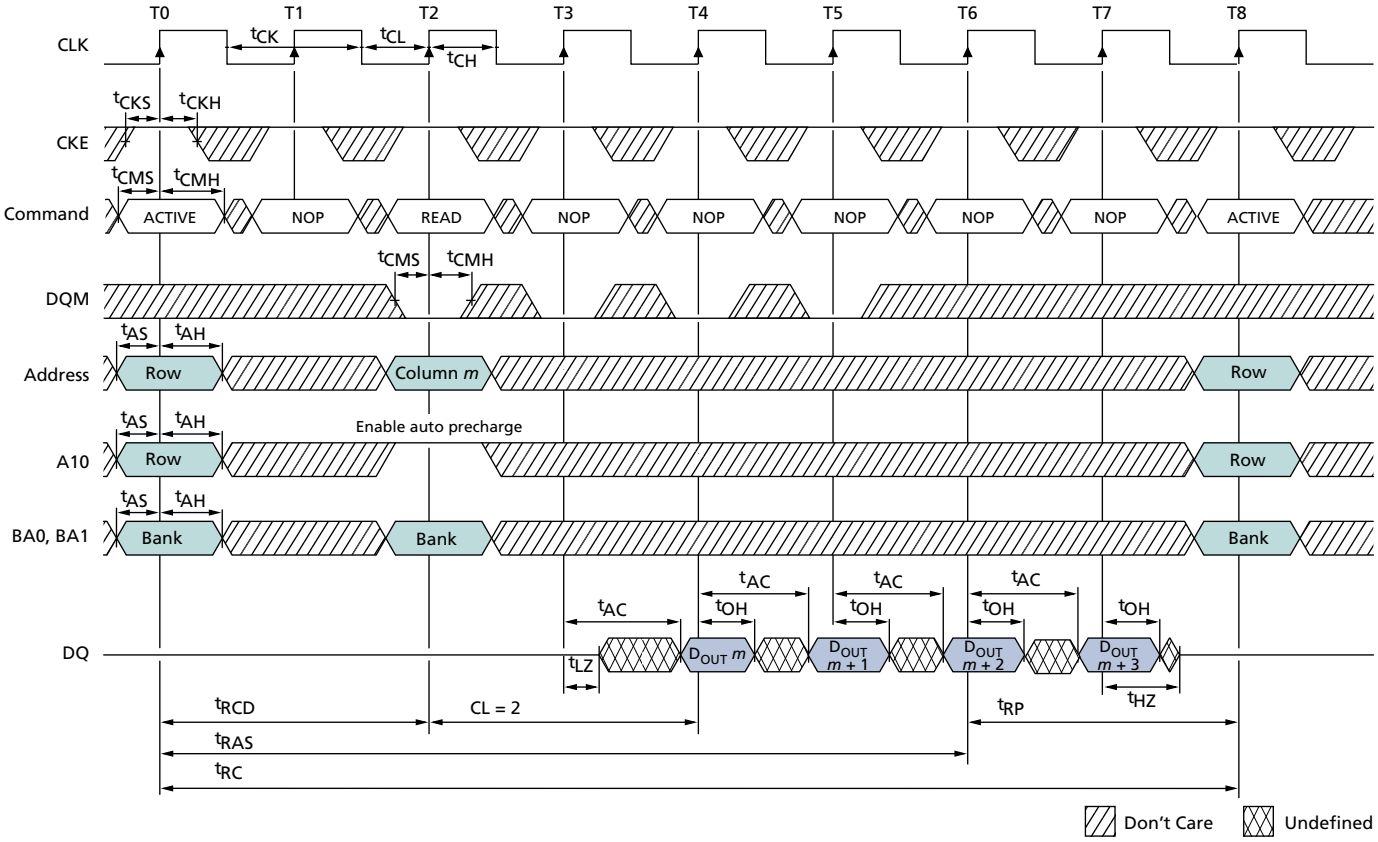
Note: 1. DQM is LOW.

Figure 36: READ With Auto Precharge Interrupted by a WRITE



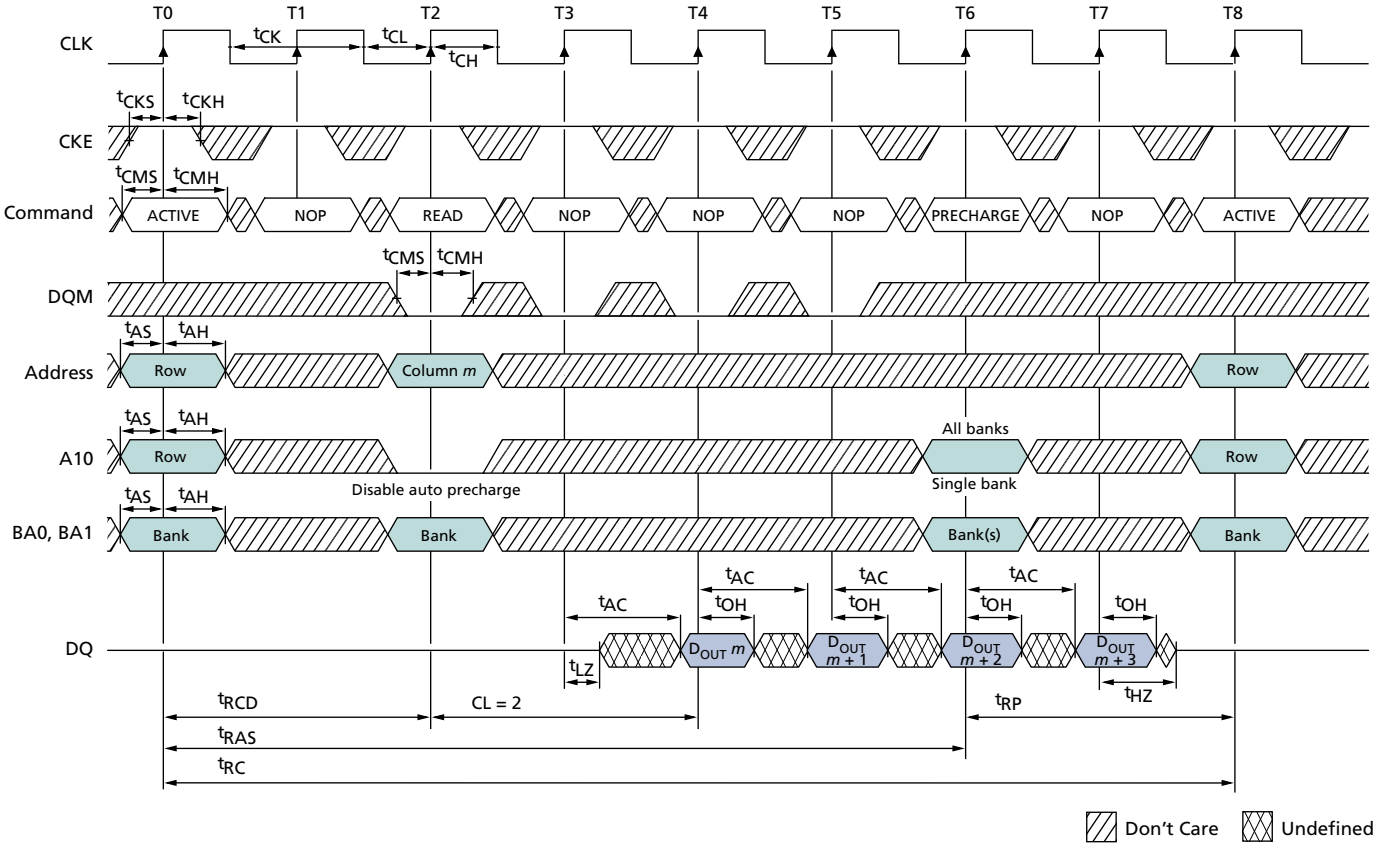
Note: 1. DQM is HIGH at T2 to prevent $D_{OUT}a + 1$ from contending with $D_{IN}d$ at T4.

Figure 37: READ With Auto Precharge



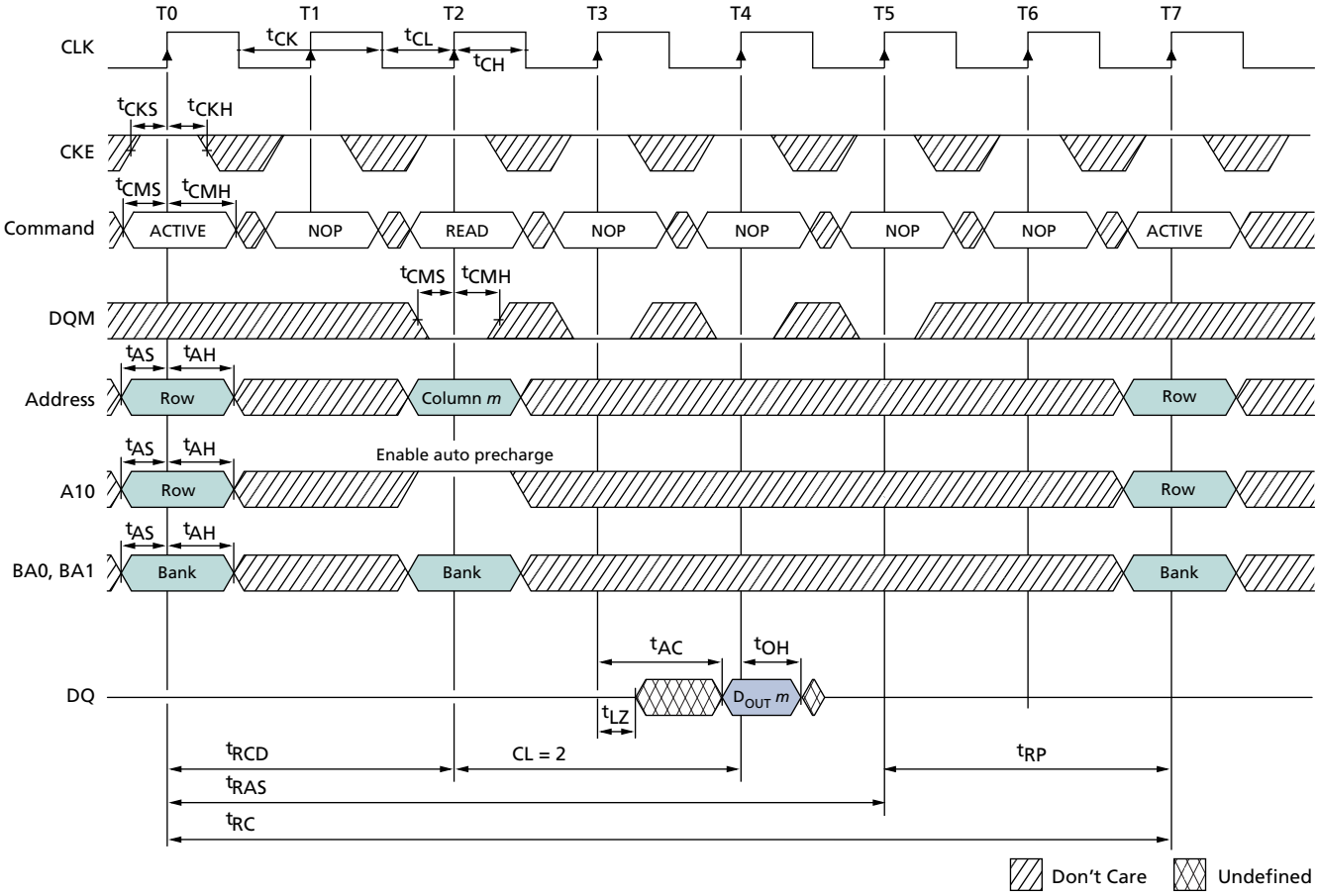
Note: 1. For this example, BL = 4 and CL = 2.

Figure 38: READ Without Auto Precharge



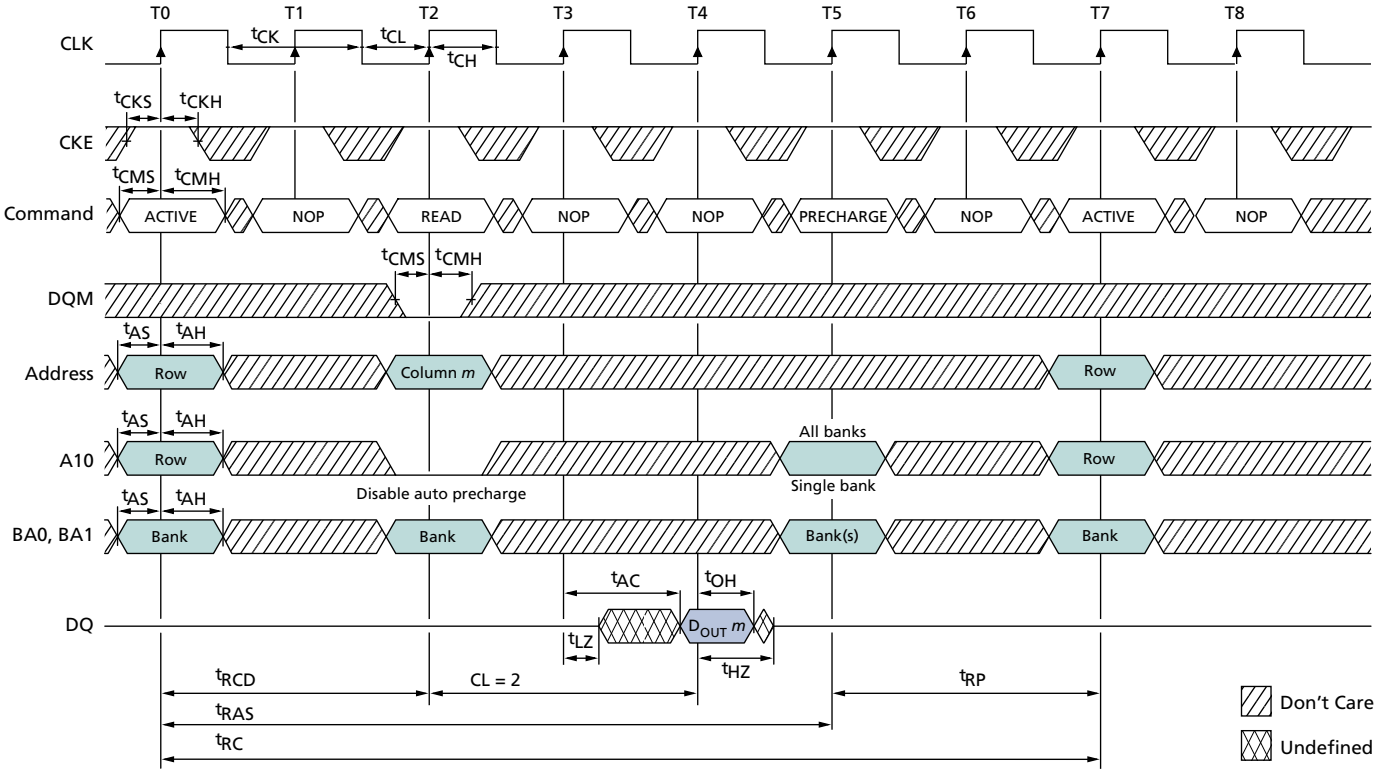
Note: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 39: Single READ With Auto Precharge



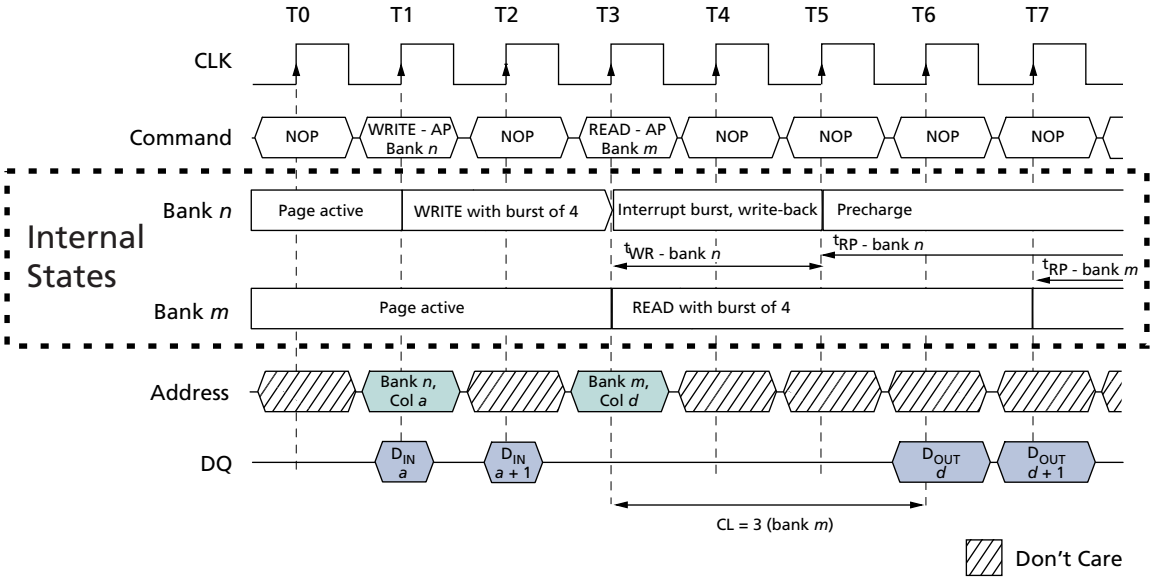
Note: 1. For this example, BL = 1 and CL = 2.

Figure 40: Single READ Without Auto Precharge



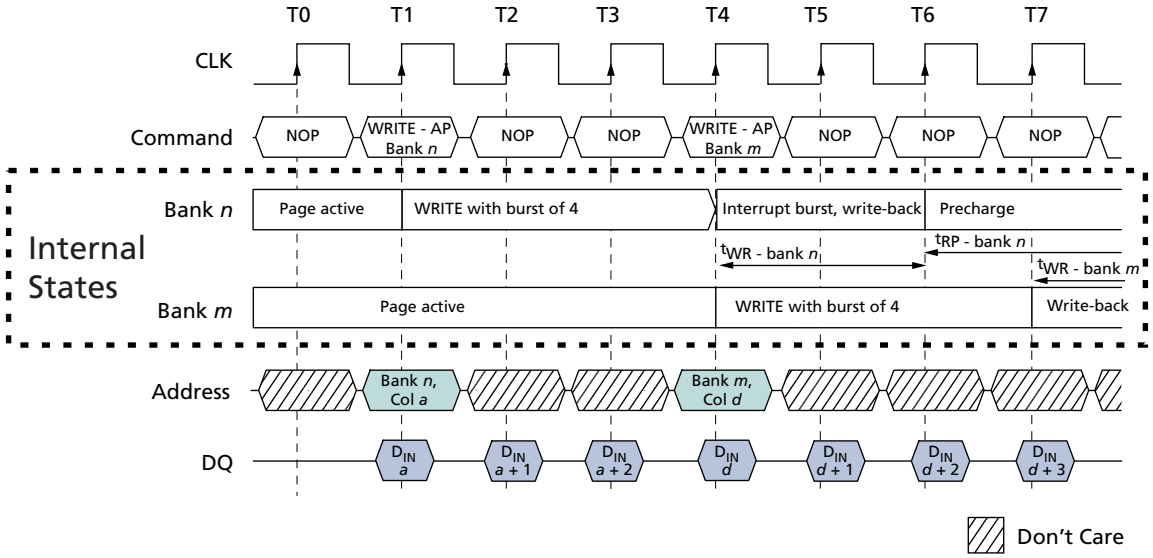
Note: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 41: WRITE With Auto Precharge Interrupted by a READ



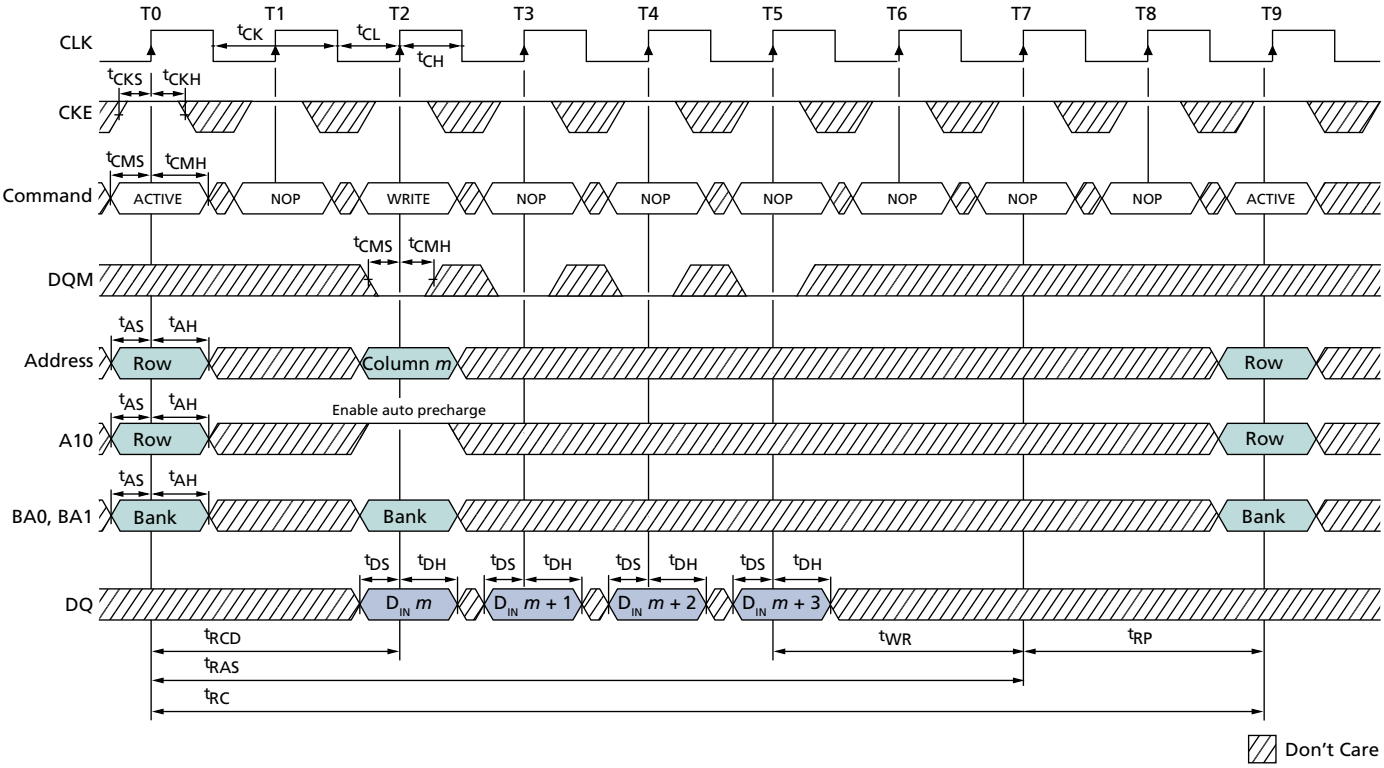
Note: 1. DQM is LOW.

Figure 42: WRITE With Auto Precharge Interrupted by a WRITE



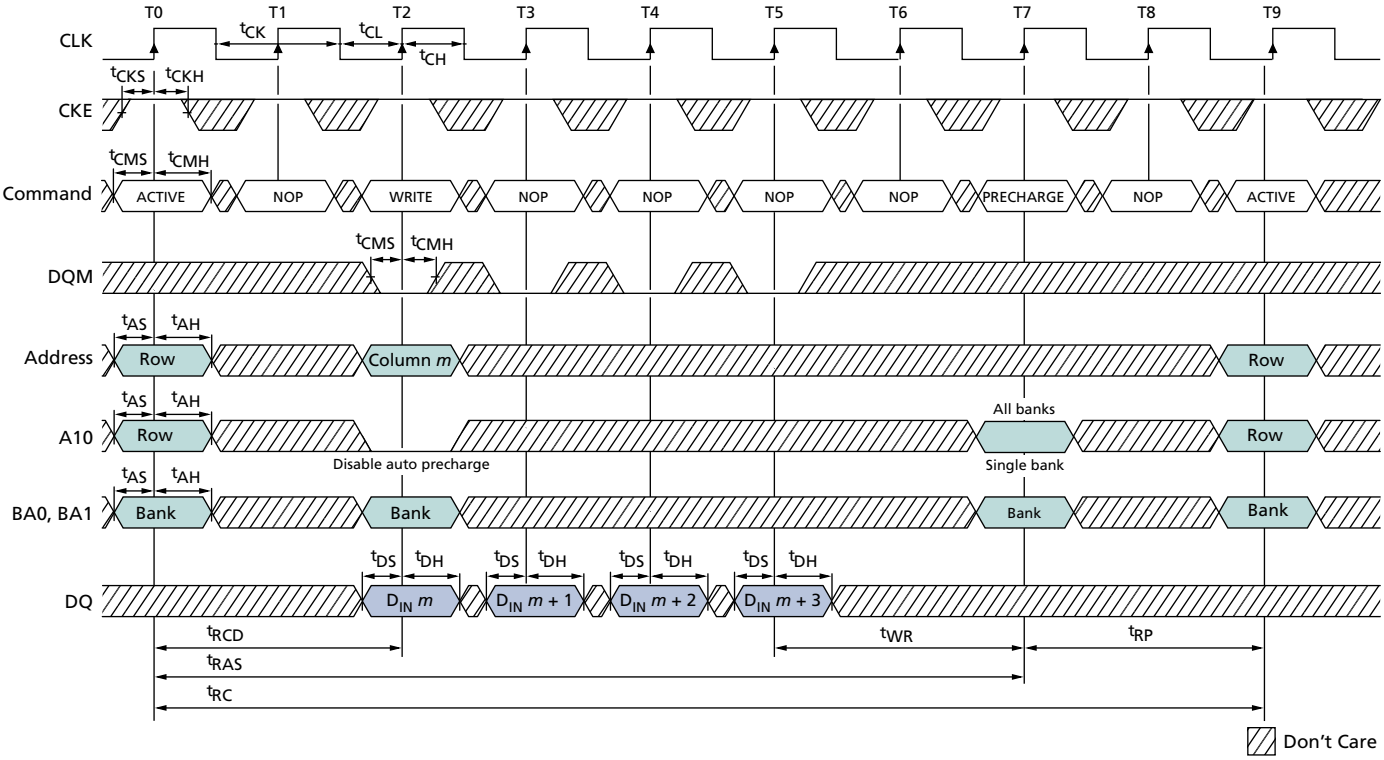
Note: 1. DQM is LOW.

Figure 43: WRITE With Auto Precharge



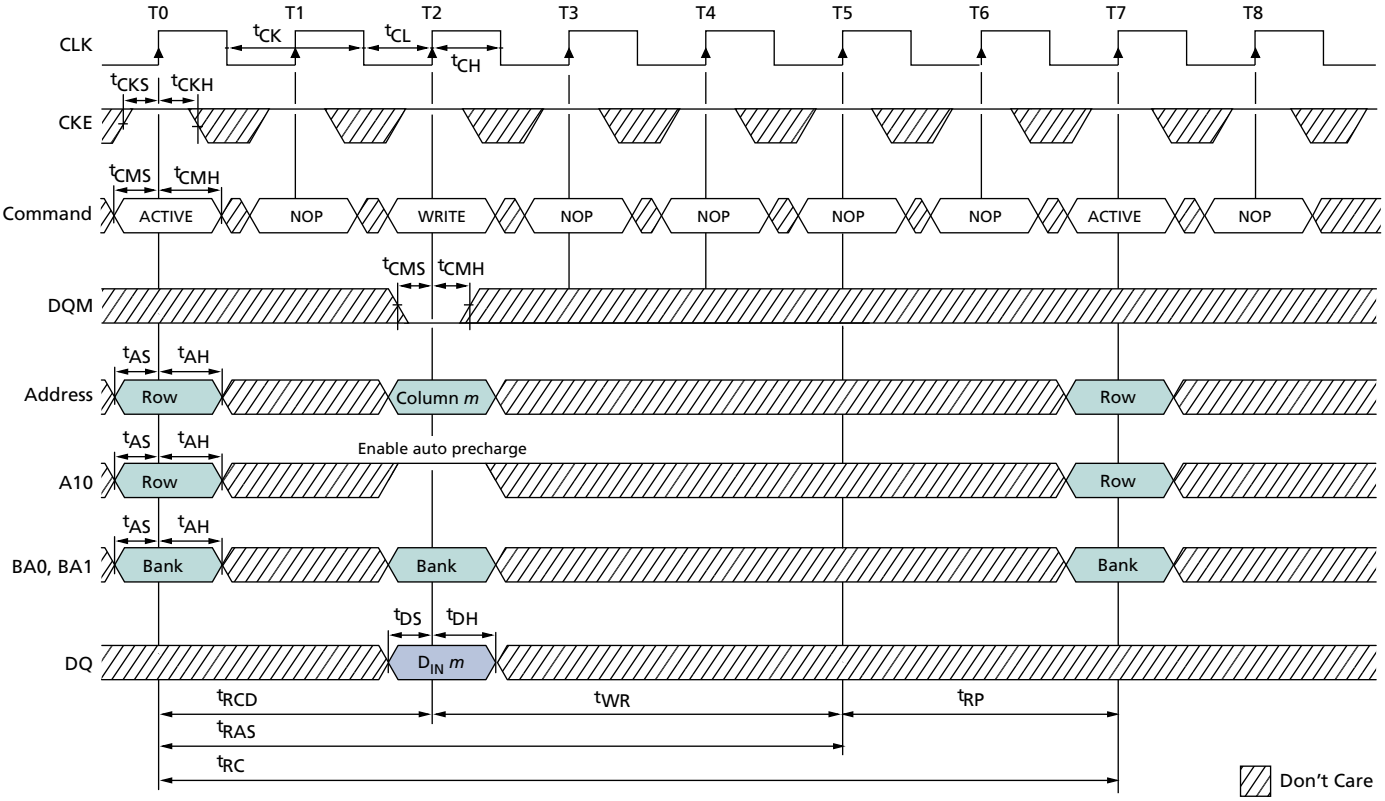
Note: 1. For this example, BL = 4.

Figure 44: WRITE Without Auto Precharge



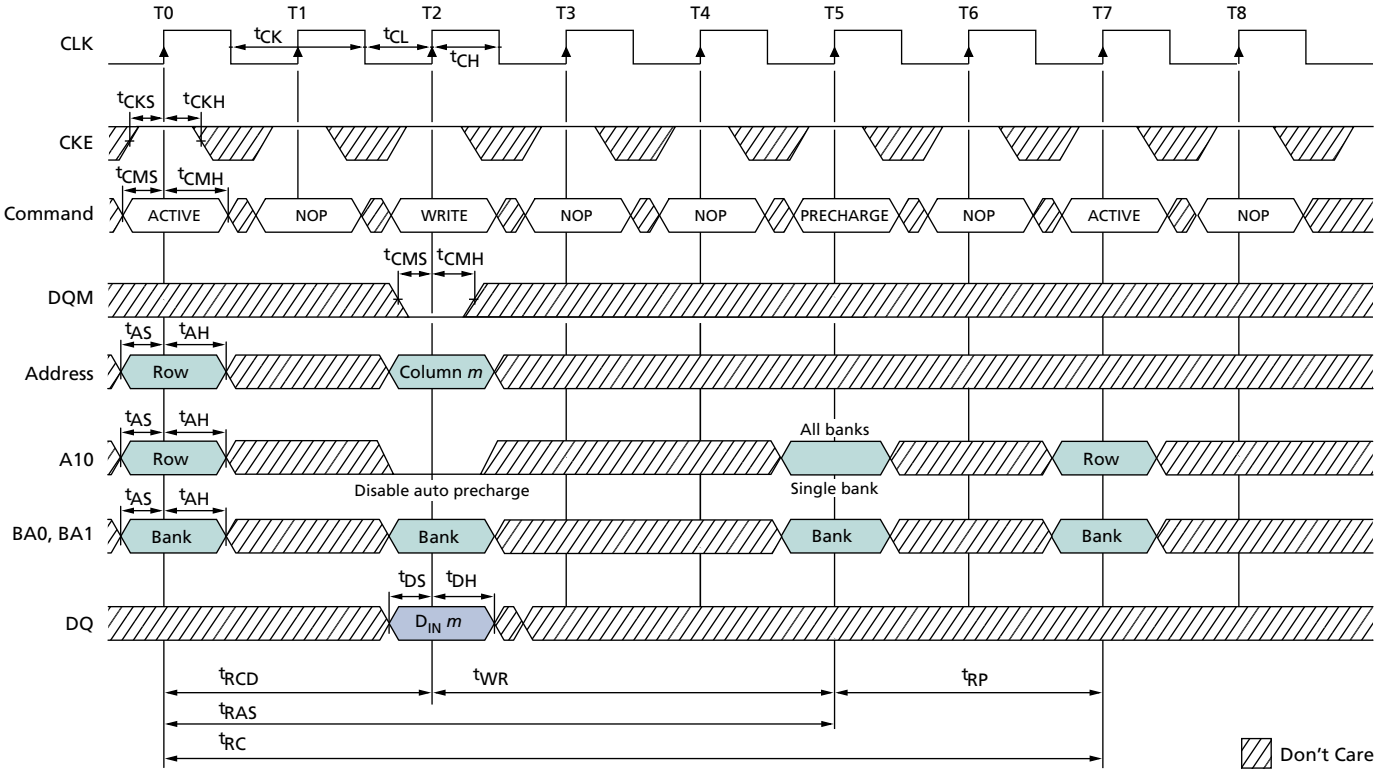
Note: 1. For this example, BL = 4 and the WRITE burst is followed by a manual PRECHARGE.

Figure 45: Single WRITE With Auto Precharge



Note: 1. For this example, BL = 1.

Figure 46: Single WRITE Without Auto Precharge



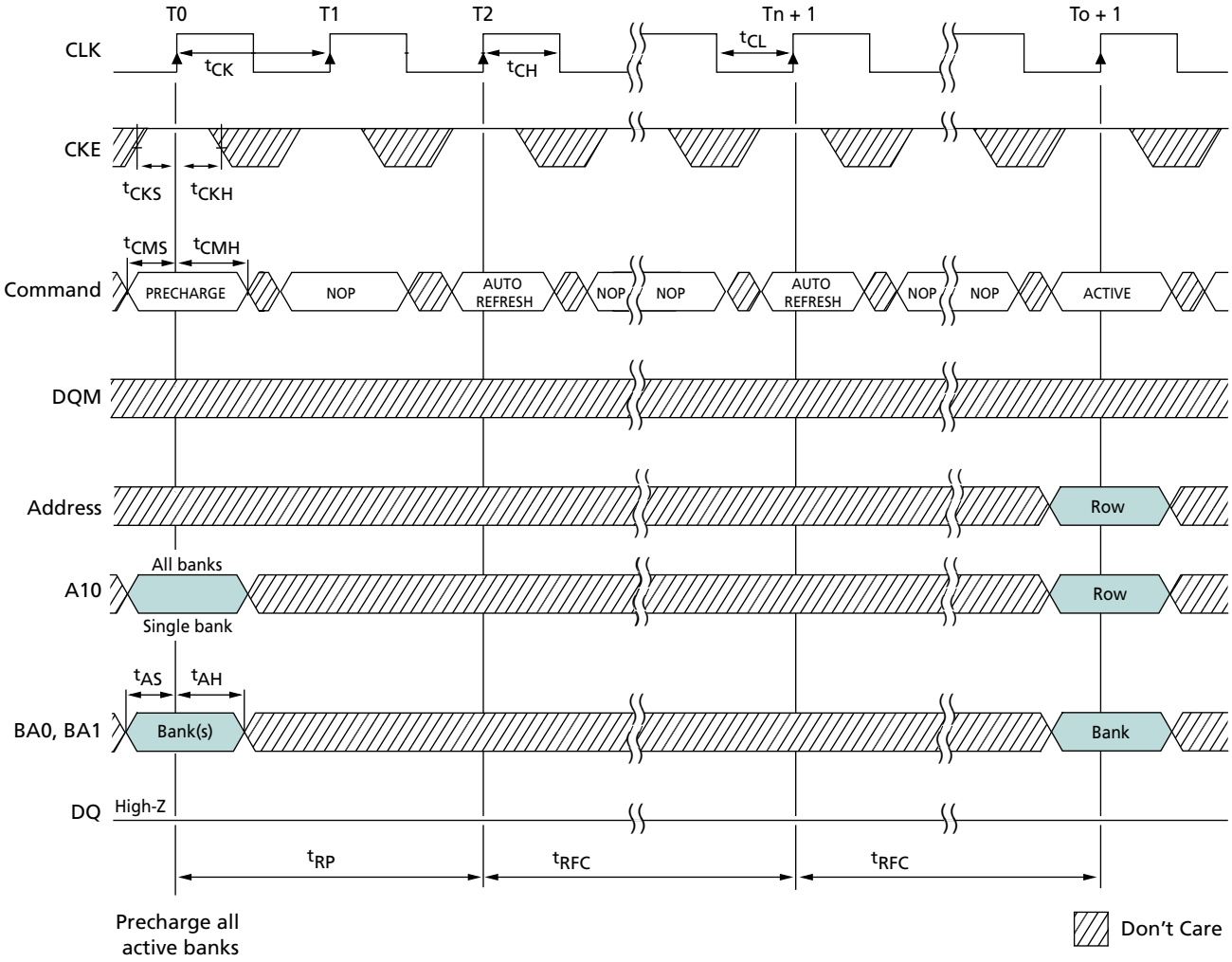
Note: 1. For this example, BL = 1 and the WRITE burst is followed by a manual PRECHARGE.

AUTO REFRESH Operation

The AUTO REFRESH command is used during normal operation of the device to refresh the contents of the array. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP is met following the PRECHARGE command. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

After the AUTO REFRESH command is initiated, it must not be interrupted by any executable command until ^{t}RFC has been met. During ^{t}RFC time, COMMAND INHIBIT or NOP commands must be issued on each positive edge of the clock. The SDRAM requires that every row be refreshed each ^{t}REF period. Providing a distributed AUTO REFRESH command—calculated by dividing the refresh period (^{t}REF) by the number of rows to be refreshed—meets the timing requirement and ensures that each row is refreshed. Alternatively, to satisfy the refresh requirement a burst refresh can be employed after every ^{t}REF period by issuing consecutive AUTO REFRESH commands for the number of rows to be refreshed at the minimum cycle rate (^{t}RFC).

Figure 47: Auto Refresh Mode



Note: 1. Back-to-back AUTO REFRESH commands are not required.

SELF REFRESH Operation

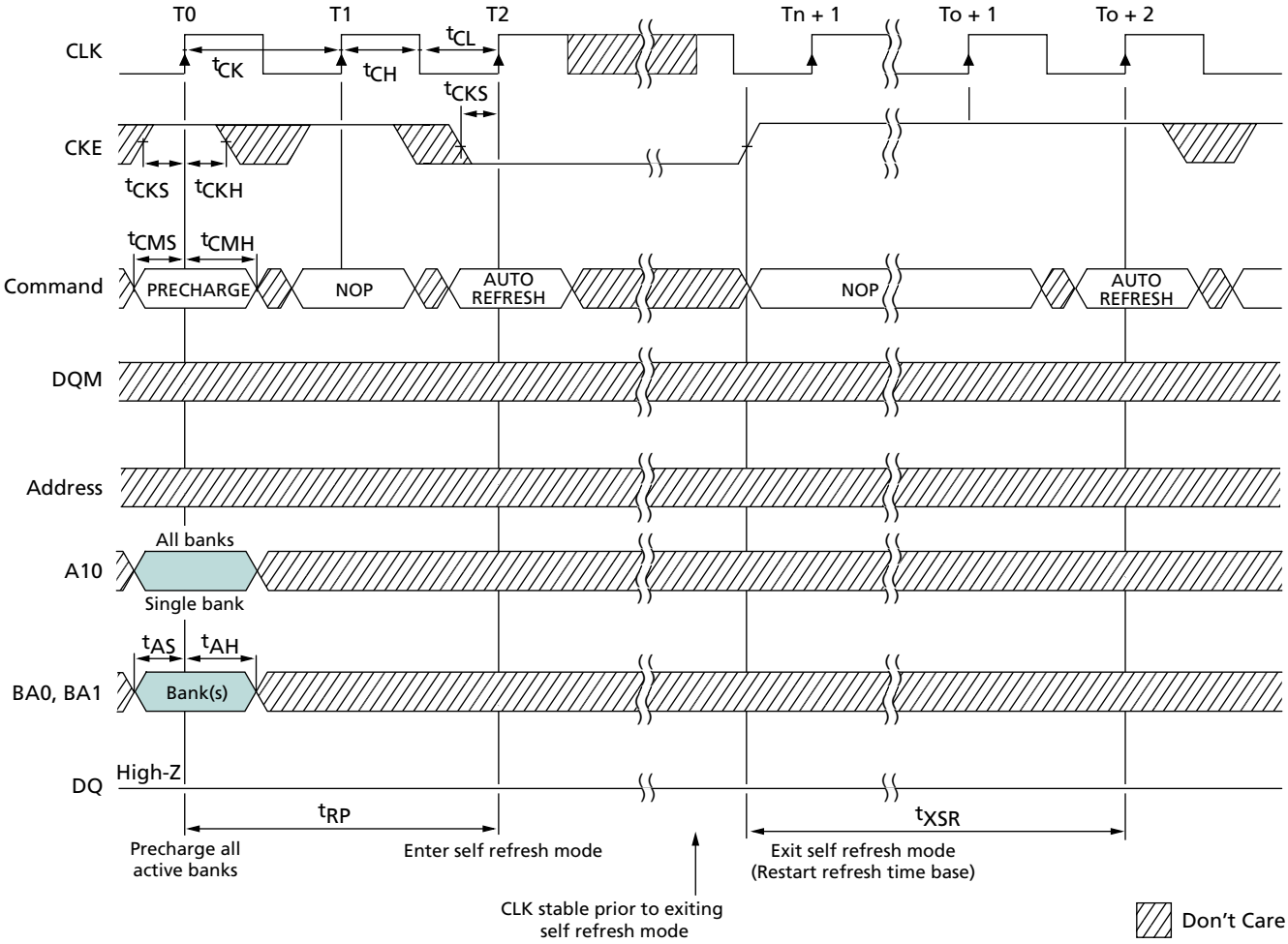
The self refresh mode can be used to retain data in the device, even when the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the device become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the device provides its own internal clocking, enabling it to perform its own AUTO REFRESH cycles. The device must remain in self refresh mode for a minimum period equal to ^{t}RAS and remains in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. (Stable clock is defined as a signal cycling within timing constraints specified for the clock ball.) After CKE is HIGH, the device must have NOP commands issued for a minimum of two clocks for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued according to the distributed refresh rate (^{t}REF/refresh row count) as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Figure 48: Self Refresh Mode



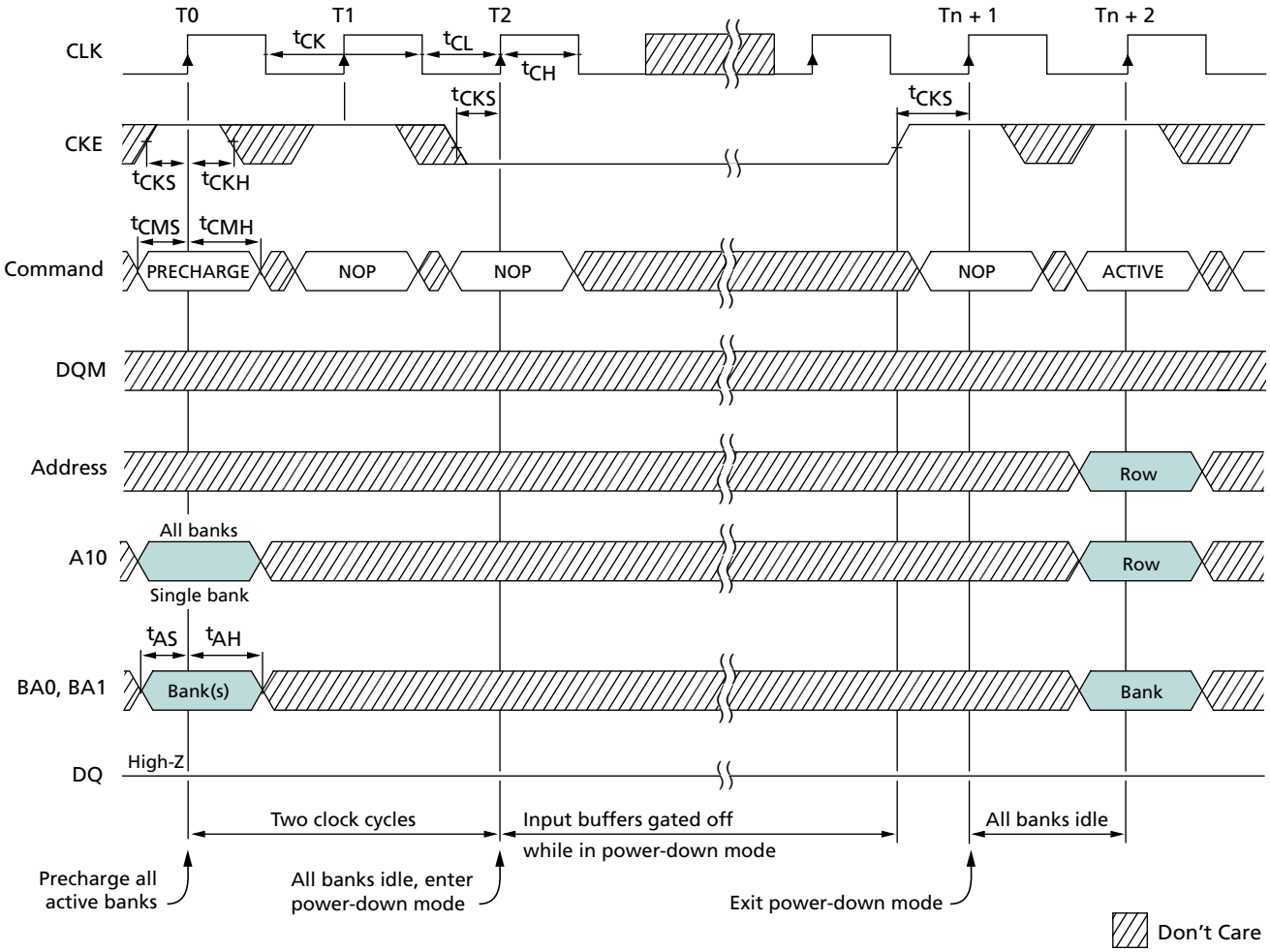
Note: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.

Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device cannot remain in the power-down state longer than the refresh period (64ms) because no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT with CKE HIGH at the desired clock edge (meeting ^{t}CKS).

Figure 49: Power-Down Mode



Note: 1. Violating refresh requirements during power-down may result in a loss of data.

Deep Power-Down

Deep power-down mode is a maximum power-saving feature achieved by shutting off the power to the entire device memory array. Data on the memory array will not be retained after deep power-down mode is executed. Deep power-down mode is entered by having all banks idle, with CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

To exit deep power-down mode, CKE must be asserted HIGH. Upon exiting deep power-down mode, a full initialization sequence is required.

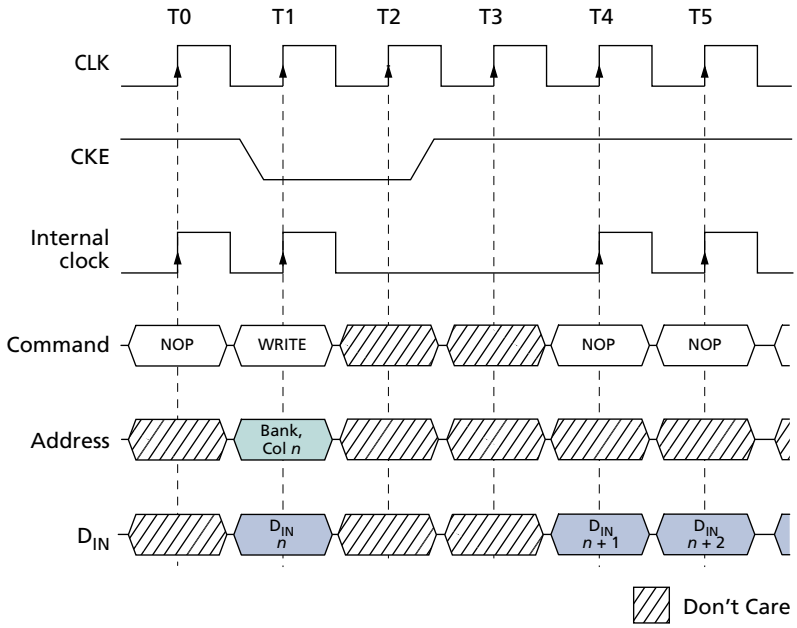
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, freezing the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls when an internal clock edge is suspended will be ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended.

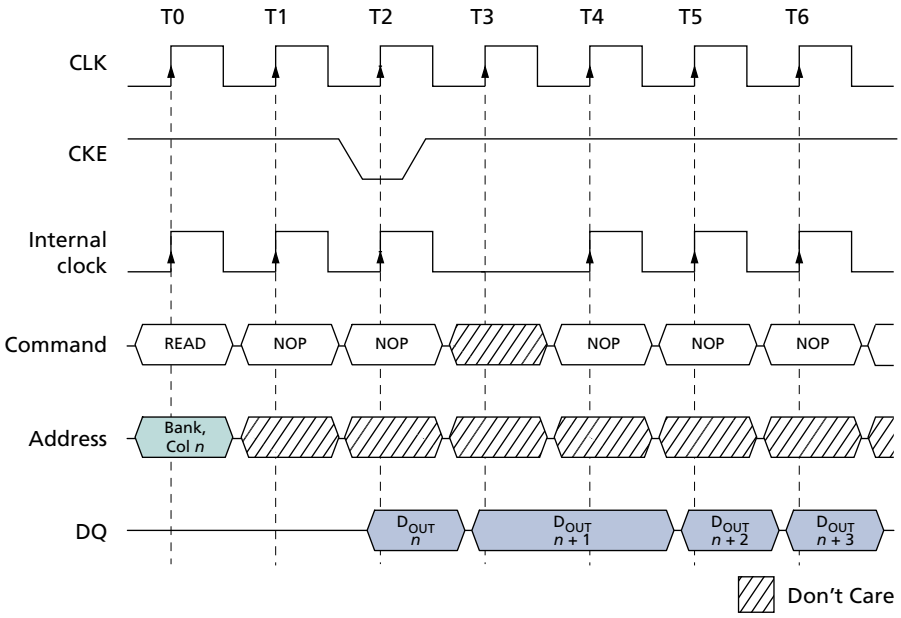
Exit clock suspend mode by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 50: Clock Suspend During WRITE Burst



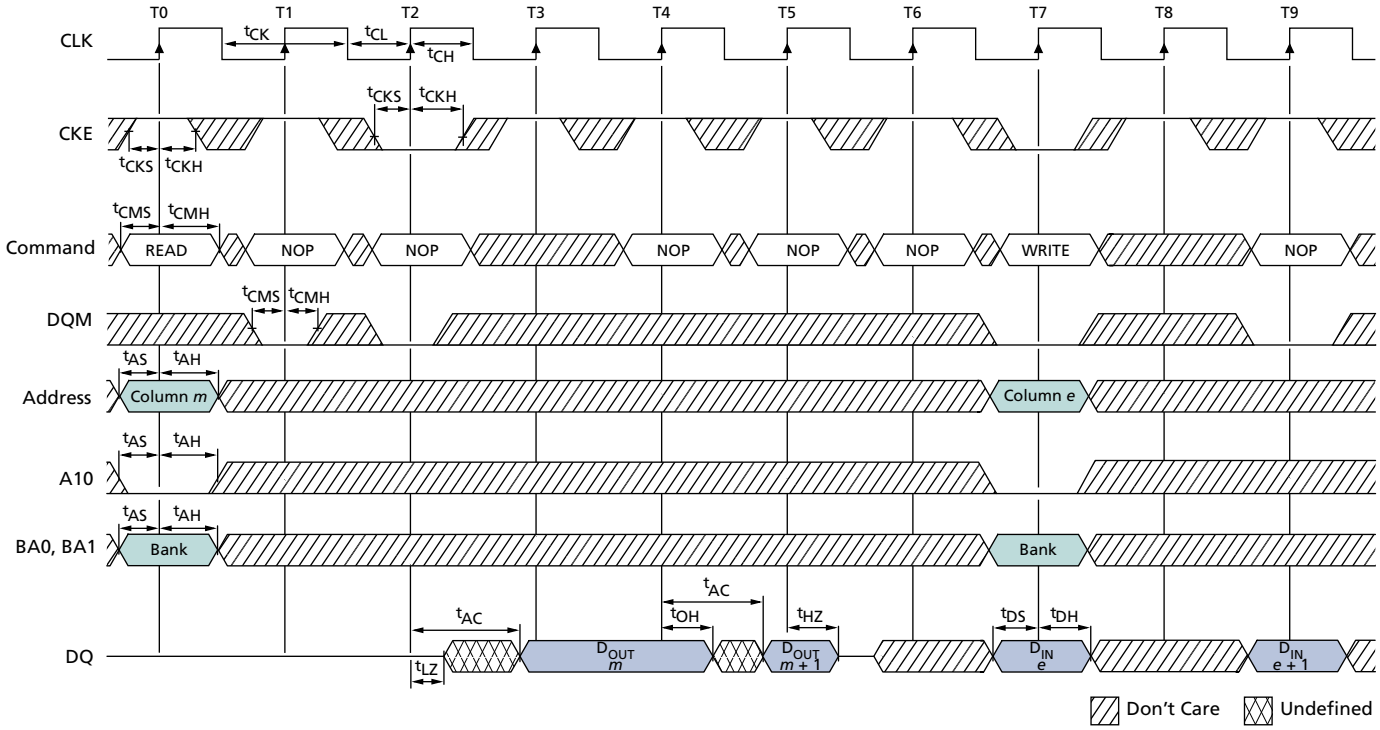
Note: 1. For this example, BL = 4 or greater, and DQM is LOW.

Figure 51: Clock Suspend During READ Burst



Note: 1. For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

Figure 52: Clock Suspend Mode



Note: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.

Revision History

Rev. J, Production – 09/10

- Select Idd limits were tightened for x16 and x32 configurations

Rev. I, Production – 11/09

- Corrected seating plane value on package dimension drawings from 0.12 to 0.1.

Rev. H, Production – 10/09

- Changed ^{t}RFC from 97.5ns to 72ns in the Electrical Specificatins and AC Operating Conditions table.

Rev. G, Production – 8/09

- Updated format.

Rev. F, Production – 6/09

- DC Electrical Characteristics and Operating Conditions table: Updated I_{OZ} to ±1.5µA.

Rev. E, Production – 4/09

- VFBGA Ball Descriptions table: Removed ball assignments columns.
- AC Functional Characteristics table: Updated note 9.

Rev. D, Production – 1/09

- Replaced the 8mm x 8mm 54-ball package drawing with an 8mm x 9mm package drawing.
- Updated the 90-ball package drawing.

Rev. C, Production – 12/08

- Changed to Production status.
- I_{DD7} Specifications and Conditions (x16 and x32) table: Updated I_{DD7} values for full array 85°C, 1/8 array 45°C, and 1/16 array 45°C.

Rev. B, Preliminary – 10/08

- Changed to Preliminary status.
- VFBGA Ball Descriptions table: Rearranged table content that was out of order.

Rev. A, Advance – 9/08

- Initial release.

Revision History for Commands, Operations, and Timing Diagrams

Update – 10/08

- Deep Power-Down: Added description for exiting DPD.

Update – 7/08

- Updated address/data range presentation to industry-standard presentation.
- Replaced MODE REGISTER SET with LMR as appropriate.
- Truth Table – Current State Bank n, Command to Bank m, note 13: Added missing "m."
- Mode Register: Corrected presentation of mode register bits.
- Partial-Array Self Refresh (PASR): Updated refresh options presentation.

Update – 5/08

- Auto Precharge: Added fourth paragraph regarding ^{t}RAS lock-out.
- Single READ With Auto Precharge: Updated figure.
- WRITE Without Auto Precharge: Updated note to BL = 4.
- Single WRITE With Auto Precharge: Updated figure.
- Single WRITE Without Auto Precharge: Updated figure.

Update – 4/08

- Added three-quarter drive strength content.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
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