CY7C194BN

256 Kb (64 K × 4) Static RAM

Features

- Fast access time: 15 ns
- Wide voltage range: 5.0 V ± 10% (4.5 V to 5.5 V)
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Transistor transistor logic (TTL) compatible inputs and outputs
- CY7C194BN is available in 24-pin DIP, 24-pin SOJ packages.

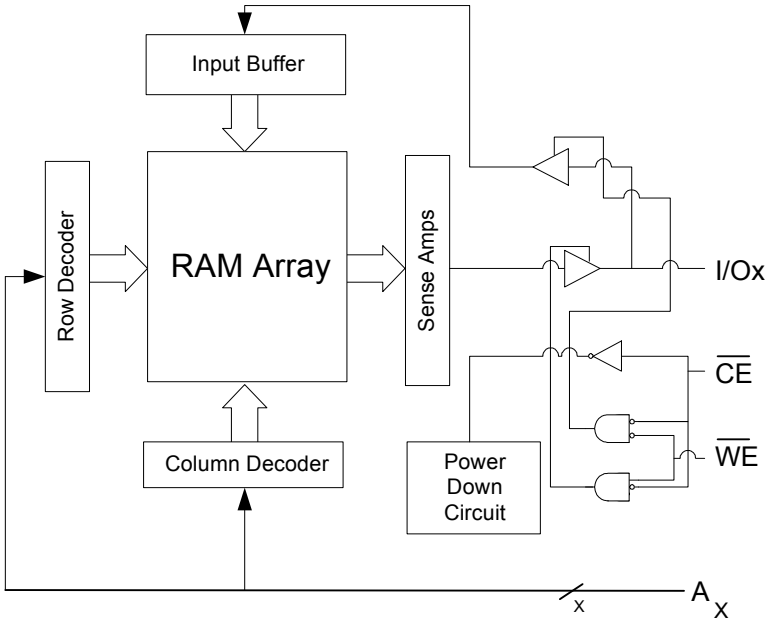
General Description

The CY7C194BN is a high-performance CMOS Asynchronous SRAM organized as 64 K × 4 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C194BN is available in 24-pin DIP, 24-pin SOJ package(s).

Logic Block Diagram



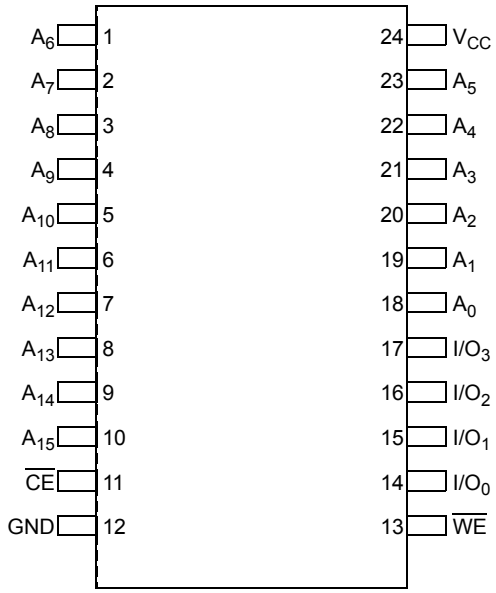
Contents

Product Portfolio

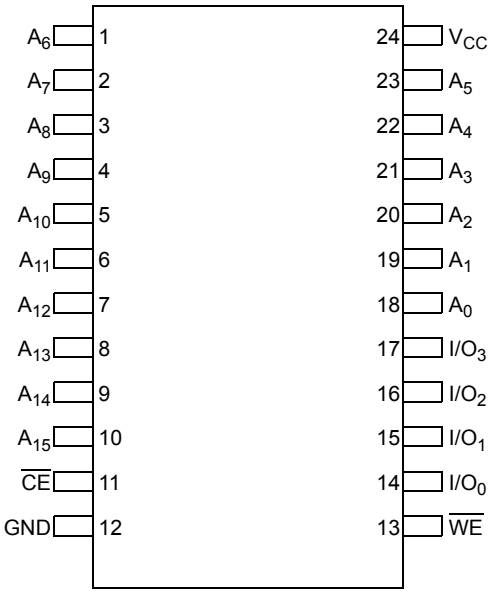
Description	-15	Unit
Maximum access time	15	ns
Maximum operating current	80	mA
Maximum CMOS standby current	10	mA

Pin Layout and Specification

CY7C194BN 24-pin SOJ (8 × 15 × 3.5 mm)



CY7C194BN 24-pin DIP (6.6 × 31.8 × 3.5 mm)



Pin Description

Pin	Type	Description	CY7C194BN	
			24-pin DIP	24-pin SOJ
A_X	Input	Address inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	Chip enable	11	11
I/O_X	Input or output	Data input/outputs	14, 15, 16, 17	14, 15, 16, 17
NC	–	No connect. pins are not internally connected to the die	–	–
V_{CC}	Supply	Power (V)	24	24
$\overline{WE}$	Control	Write enable	13	13

CY7C194BN Truth Table

$\overline{CE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	High Z	Power-down	Standby (I_{SB})
L	H	Data out	Read	Active (I_{CC})
L	L	Data in	Write	Active (I_{CC})

Maximum Ratings

Above which the useful life may be impaired. For user guidelines, not tested.

Parameter	Description	Value	Unit
T_{STG}	Storage temperature	–65 to +150	°C
T_{AMB}	Ambient temperature with power applied (i.e. case temperature)	–55 to +125	°C
V_{CC}	Core supply voltage relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC voltage applied to any pin relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output short-circuit current	20	mA
V_{ESD}	Static discharge voltage (per MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0 °C to 70 °C	5.0 V ± 10%

DC Electrical Characteristics

Parameter [1]	Description	Condition	15 ns		Unit
			Min	Max	
V_{IH}	Input HIGH voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	0.8	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = F_{MAX} = 1 / t_{RC}	–	80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down current – TTL inputs	V_{CC} = Max, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down current – CMOS inputs	V_{CC} = Max, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} > V_{CC}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0, Commercial	–	10	mA
I_{OZ}	Output leakage current	GND $\leq V_I \leq V_{CC}$, output disabled	–5	+5	µA
I_{IX}	Input load current	GND $\leq V_I \leq V_{CC}$	–5	+5	µA

Capacitance

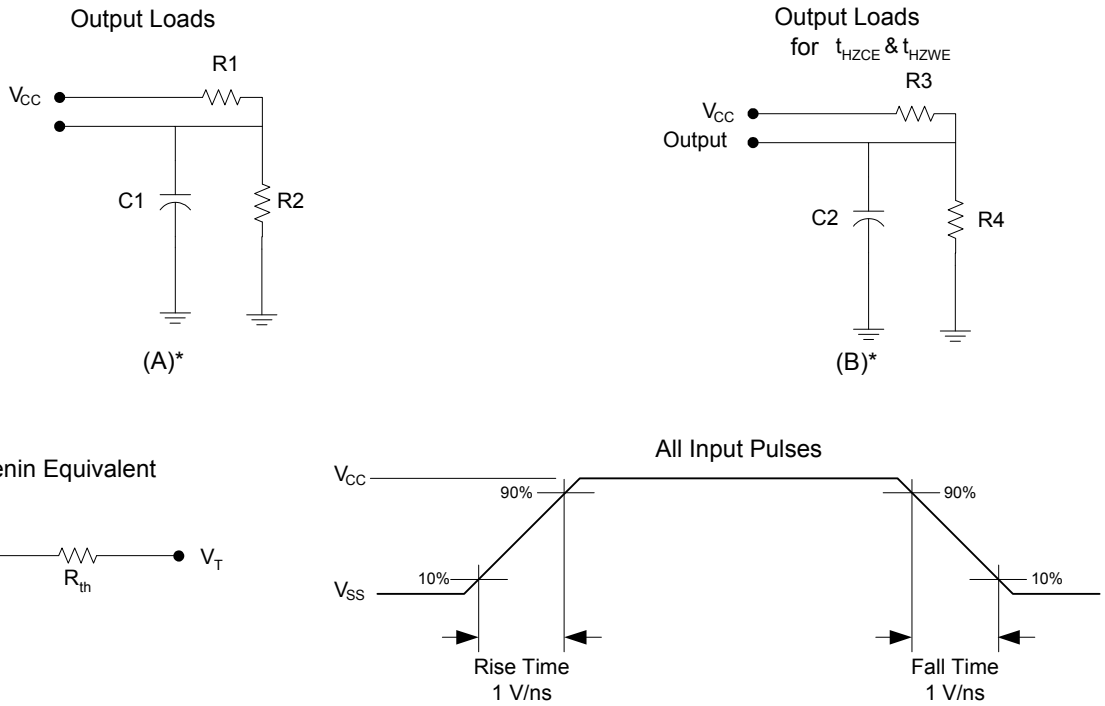
Parameter [2]	Description	Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	7	pF
C_{OUT}	Output capacitance		10	–

Thermal Resistance

Parameter [2, 3]	Description	Conditions	CY7C194BN		Unit
			24-pin DIP	24-pin SOJ	
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ_{JC}	Thermal resistance (junction to case)		33.80	37.56	

Notes
1. V_{IL}(min) = –2.0 V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process change that may affect these parameters
3. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

AC Test Loads



* including scope and jig capacitance

AC Test Conditions

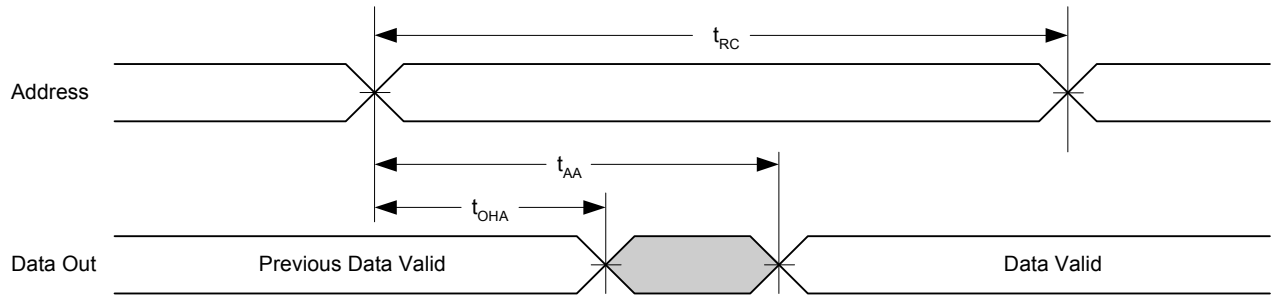
Parameter	Description	Nom	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

AC Electrical Characteristics

Parameter [4, 5, 6, 7]	Description	15 ns		Unit
		Min	Max	
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ to data valid	–	15	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	7	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	15	ns
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}$ to write end	10	–	ns
t_{AW}	Address set-up to write end	10	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	9	–	ns
t_{SD}	Data set-up to write end	8	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	ns

Timing Waveforms

Figure 1. Read Cycle No. 1 [8, 9]



Notes
4. Tested initially and after any design or process change that may affect these parameters
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
7. t_{HZCE}, t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.
8. Device is continuously selected. $\overline{CE}$ = V_{IL}.
9. $\overline{WE}$ is HIGH for Read Cycle.

Timing Waveforms *(continued)*

Figure 2. Read Cycle No. 2 [10, 11, 12]

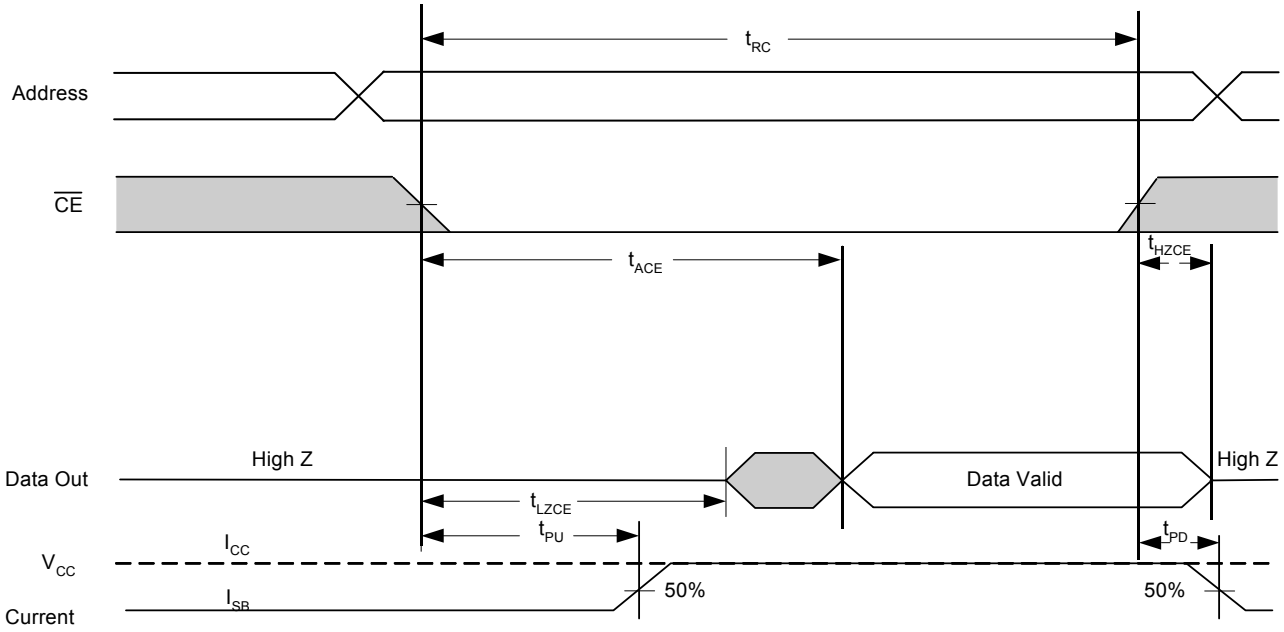
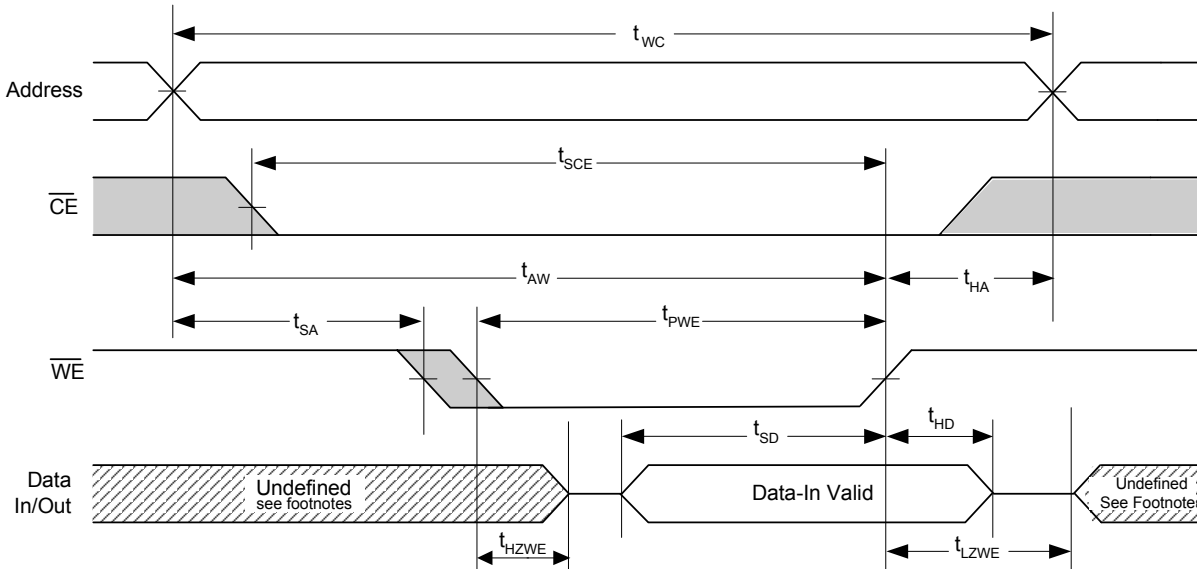


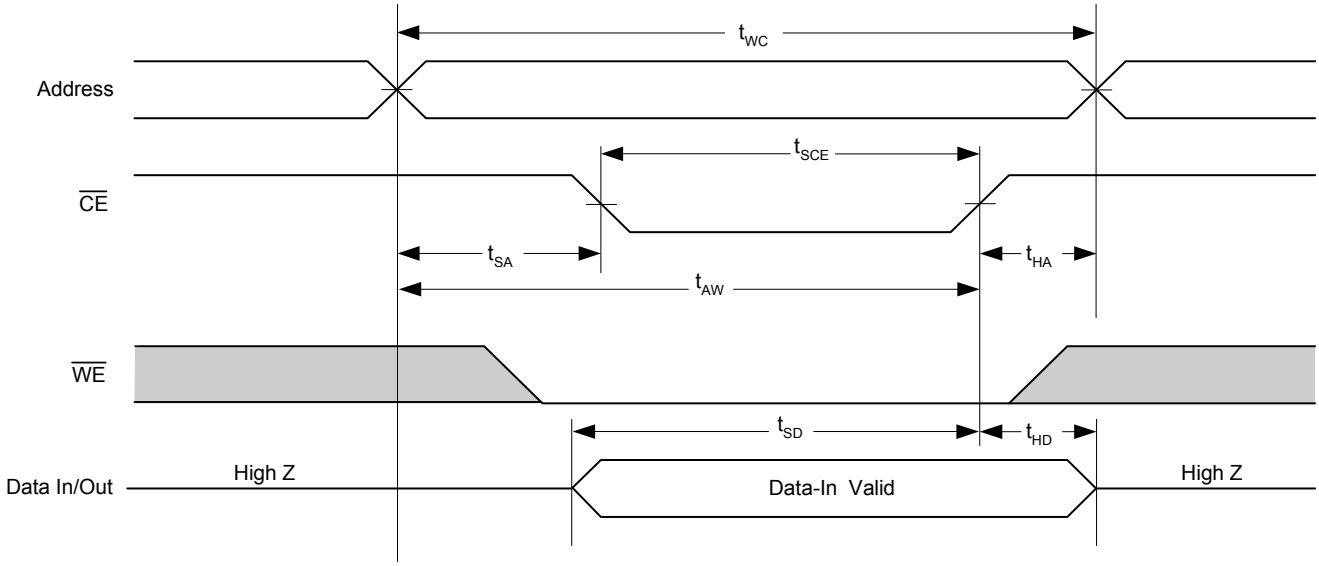
Figure 3. Write Cycle No. 1 ($\overline{WE}$ Controlled) [10, 13]



Notes
10. Tested initially and after any design or process change that may affect these parameters
11. $\overline{WE}$ is HIGH in read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Timing Waveforms *(continued)*

Figure 4. Write Cycle No. 2 ($\overline{CE}$ Controlled) [14, 15]



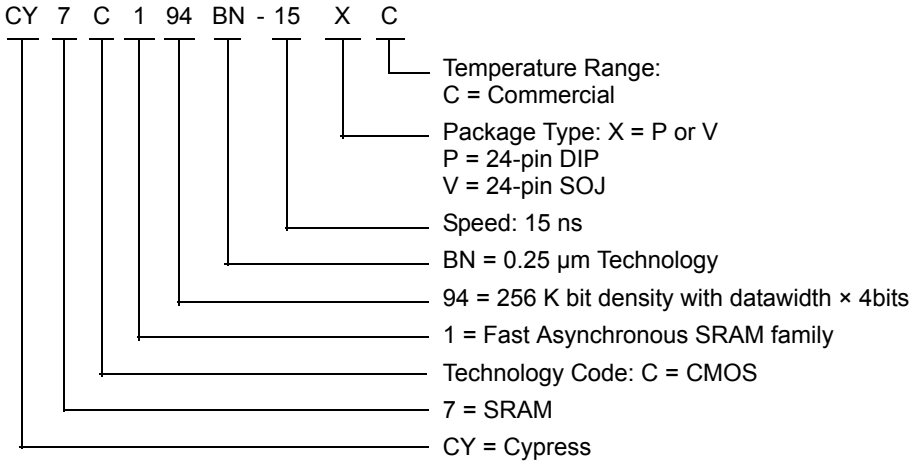
Notes
14. This cycle is $\overline{CE}$ controlled.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
15	CY7C194BN-15PC	51-85013	24-pin DIP (6.6 × 31.8 × 3.5 mm)	Standard	Commercial
	CY7C194BN-15VC	51-85030	24-pin SOJ (8 × 15 × 3.5 mm)	Standard	Commercial

Please contact local sales representative regarding availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 5. 24-pin (300-mil) SOJ V24.3/VZ24.3 (Molded SOJ V13), 51-85030

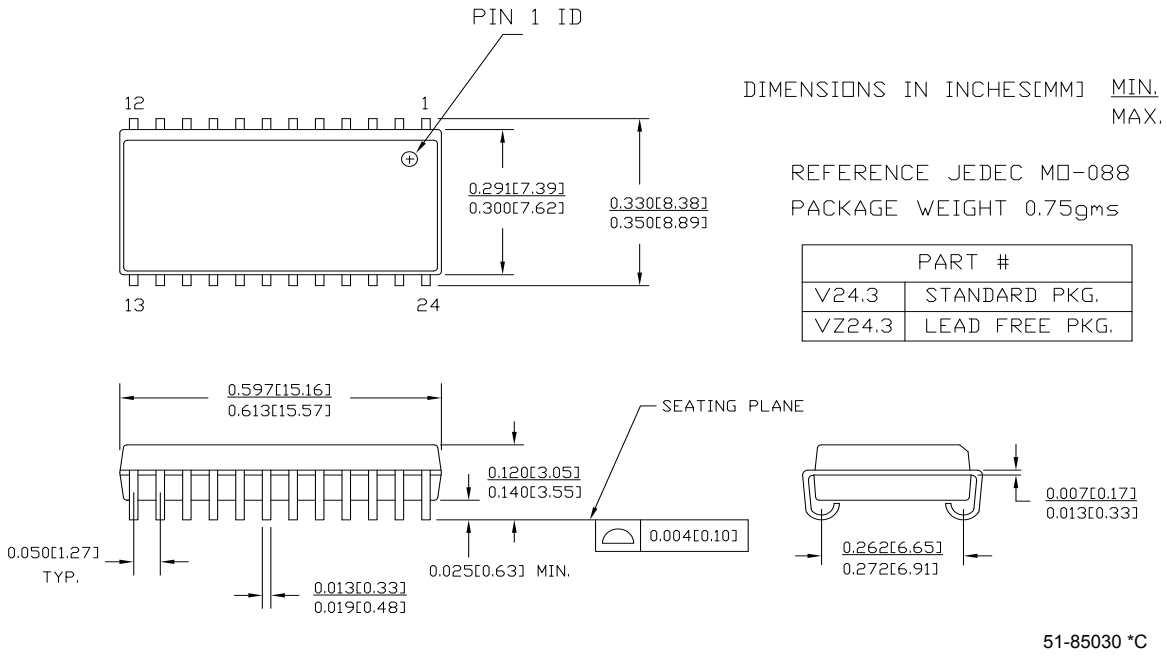
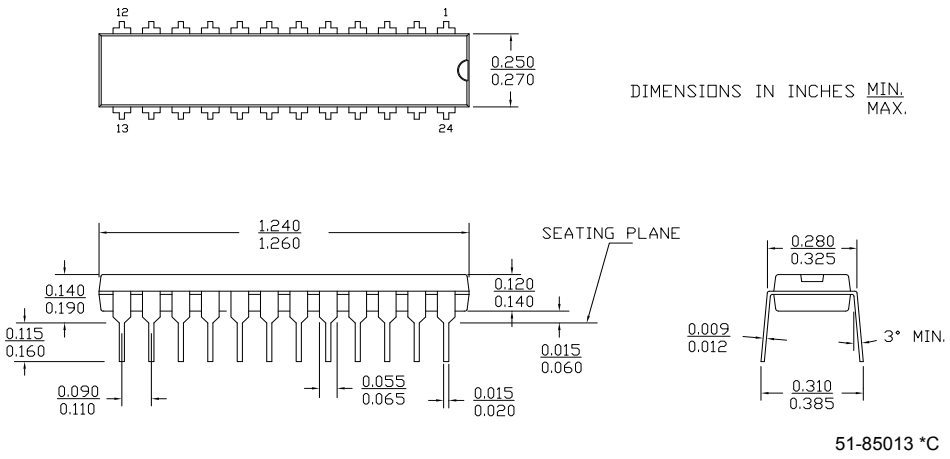


Figure 6. 24-pin PDIP (1.260 × 0.270 × 0.140 Inches) P24.3, 51-85013



Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
DIP	dual in-line package
ESD	electrostatic discharge
I/O	input/output
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
µA	micro Amperes
mA	milli Amperes
mm	milli meter
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY7C194BN, 256 Kb (64 K × 4) Static RAM Document Number: 001-06446				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	424111	See ECN	NXR	New Data Sheet
*A	2892510	03/18/2010	VKN	Removed 25ns speed bin Updated Ordering Information table Updated Package Diagram Added Sales, Solutions, and Legal Information
*B	3108898	12/13/2010	AJU	Added Ordering Code Definitions.
*C	3219087	04/18/2011	PRAS	Updated as per template Added TOC Added Acronyms and Units of Measure.
*D	3271782	06/02/2011	PRAS	Updated General Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated in new template.

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