CML Microcircuits
COMMUNICATION SEMICONDUCTORS

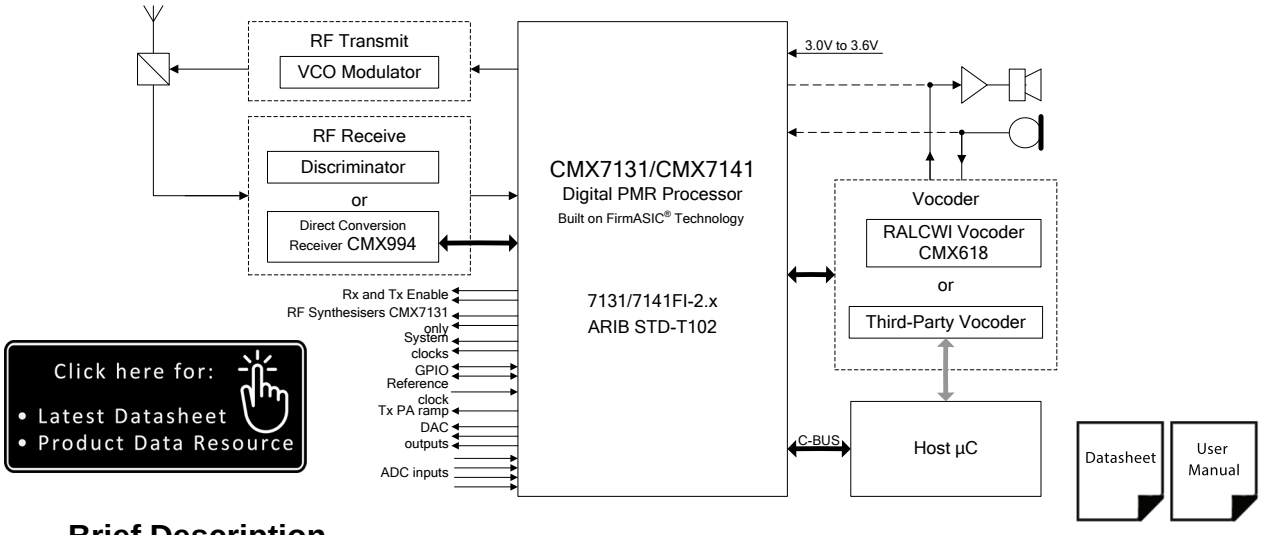
CMX7131/CMX7141
Digital PMR Processor
T102 Operation

D/7131/41_FI-6.x/7 May 2016 **DATASHEET** Advance Information

7131/7141FI-6.x: ARIB STD-T102 Baseband Data Processor with Auxiliary System Clocks, ADCs and DACs

Features

- **Digital PMR**
  - **ARIB STD-T102 Compliant**
  - **Air Interface Physical Layer (Layer 1)**
  - **Air Interface Data Link Layer (Layer 2)**
- **4FSK Modem**
  - **4.8 kbps Data Rate**
  - **Soft-decision Data Output Option**
  - **AFSD (Automated Frame Sync Detection)**
- **Tx Outputs for Two-Point or I/Q Modulation**
- **Rx Inputs for CMX994 Direct Conversion (I/Q) Receiver**
- **Two RF Synthesisers (CMX7131 only)**
- **Two Auxiliary ADCs (4 Multiplexed Inputs)**
- **Four Auxiliary DACs**
- **Two Auxiliary System Clock Outputs**
- **Flexible Powersave Modes**
- **Available in Small LQFP or VQFN Packages**
- **Low-power (3.0 to 3.6 V) Operation**
- **C-BUS Serial Interface to Host µController**
- **Vocoder Connectivity**
  - **Vocoder Management and Control (RALCWI Vocoders CMX608 and CMX618)**
  - **Vocoder Data Transport (Third-party vocoders e.g. AMBE-3000)**



1 Brief Description

The CMX7131/CMX7141 with 7131/7141FI-6.x implements a half-duplex 4FSK modem and a large proportion of the ARIB STD-T102 Air Interface, Data Link and Call Control layers. In conjunction with a suitable host and a limiter/discriminator based RF transceiver or CMX994 Direct Conversion (I/Q) Receiver, a compact, low cost, low power digital PMR radio conforming to ARIB's T102 standard can be realised. The 7131/7141FI-6.1.x has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default and is compatible with 7131/7141FI-6.0.x for conventional limiter/discriminator

receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. Dual mode, analogue/digital PMR operation can also be achieved with the CMX7131/CMX7141.

The embedded functionality of the CMX7131/CMX7141 allows managing voice and data systems autonomously including CMX6x8 Vocoder control. Host microcontroller interactions are minimised enabling the lowest operating power and therefore the longest battery life for a T102 radio. The CMX7131/CMX7141 can also provide audio codec functionality for vocoders under direct host control.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host µController over the built-in C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7131/7141FI-6.1.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). The CMX7131 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover.

The CMX7141 is identical in functionality to the CMX7131 with the exception that the two on-chip RF Synthesisers have been deleted, which enables it to be supplied in a smaller package. This document refers to both parts generically as the CMX7141, unless otherwise stated.

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

CONTENTS

Table Page

Figure Page

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.
It is recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
7	Section 6.6.10 Add Tx repeated word command ($C1=0062) Section 8.1.3: RxENA and TxENA logic level invert function added to register $A7:b1 Section 8.1.24: Entire description of register $C3 restructured to improve clarity and includes the following additions: SPI/PCM Rx voice level scaling RAMDAC scaling feature Ability to change FS error tolerance Tx symbol level adjustment Section 8.2.1: Call drop threshold, FS error tolerance, preamble length, and repeated END and HEADER frames features added to Program Block 0. Section 8.2.3: Default values added to Program Block 2 Section 8.2.4: Tx Sequencer RAMDAC scan time configuration added as Program Block P3.80 Section 9: Function Image Updates	May 2016
6	Datasheet/User Manual updated for FI-6.1, which adds support for a CMX994 I/Q Rx interface in sections 4.3 and 5.2.6. CMX994 Pass-through mode added in section 6.6.20. Updated RAMDAC, tone generator and AGC I/Q Mode descriptions, see Figure 10 and sections 5.2.8, 8.1.4 and 8.2.4. Added RSSI - signal strength graph for I/Q mode, Figure 15 and section 5.2.4. Updated data formats in Tables 10 and 11, sections 8.1.14 and 8.1.17. Expanded description of Fine Level adjustment of outputs in section 6.14, 8.1.9, 8.1.24 and 8.2.4. Various typographical and editorial changes and update to version history.	May 2013
5	Additional RAMDAC information in section 9.1.4 Corrected b3-0 order in Table 9 Added information about Abort/Reset in section 7.7.5	14th Sept 12
4	Change 618_DIS to VOC_DIS, update description in 6.2, figs 6, 7, 8 Correct RxData and TxData bit allocations	24th Oct 11
3	Corrections to SPI bus pinout in section 3	12th Sept 11
2	Clarification of BOOTEN states and corrections to RF Synthesiser specification Addition of: • Mixed TCH / FACCH1 payload frames • Selectable number of Header / End frames • Selectable whitening sequence • Another synchronisation mode Call drop-out threshold changed to match T102 standard	24th Aug 11
1	Original document, prepared for internal and customer use.	28th Jul 11

2 Block Diagram

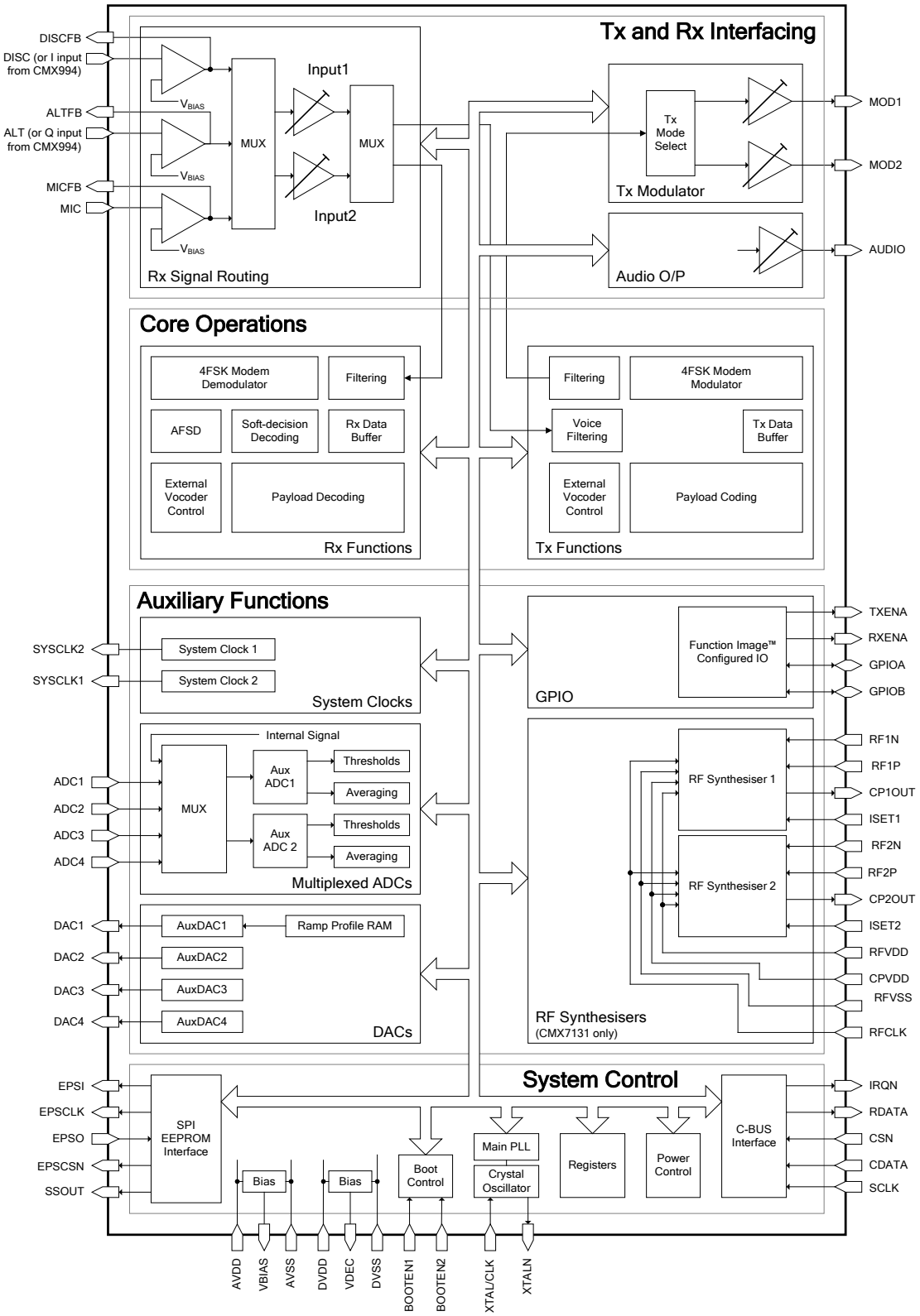


Figure 1 Block Diagram

3 Signal List

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser 1 Negative Input
3	-	RF1P	IP	RF Synthesiser 1 Positive Input
4	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 1
5	-	CP1OUT	OP	RF Synthesiser 1 Charge Pump output
6	-	ISET1	IP	RF Synthesiser 1 Charge Pump Current Set input
7	-	RFVDD	PWR	The 2.5V positive supply rail for both RF Synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser 2 Negative Input
9	-	RF2P	IP	RF Synthesiser 2 Positive Input
10	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 2
11	-	CP2OUT	OP	RF Synthesiser 2 Charge Pump output
12	-	ISET2	IP	RF Synthesiser 2 Charge Pump Current Set input
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF Synthesiser charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both RF Synthesisers)[1]
15	**11**	GPIOA	OP	General Purpose I/O pin
16	**12**	GPIOB	OP	General Purpose I/O pin
17	-	NC	NC	Reserved – do not connect this pin
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1
21	**14**	DVSS	PWR	Digital Ground
22	-	NC	NC	Reserved – do not connect this pin
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISC	IP	Discriminator inverting input or I input from CMX994
25	**17**	DISCFB	OP	Discriminator input amplifier feedback
26	**18**	ALT	IP	Alternate inverting input or Q input from CMX994

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLK input.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description	
27	**19**	ALTFB	OP	Alternate input amplifier feedback	
28	**20**	MICFB	OP	Microphone input amplifier feedback	
29	**21**	MIC	IP	Microphone inverting input	
30	**22**	AVSS	PWR	Analogue Ground	
31	**23**	MOD1	OP	Modulator 1 output	
32	**24**	MOD2	OP	Modulator 2 output	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	Audio Output in SPI-Codec mode	
35	**27**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 8.1.3 for details.
36	**28**	ADC2	IP	Auxiliary ADC input 2	
37	**29**	ADC3	IP	Auxiliary ADC input 3	
38	**30**	ADC4	IP	Auxiliary ADC input 4	
39	**31**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
41	**33**	DAC2	OP	Auxiliary DAC output 2	
42	**34**	AVSS	PWR	Analogue Ground	
43	**35**	DAC3	OP	Auxiliary DAC output 3	
44	**36**	DAC4	OP	Auxiliary DAC output 4	
-	**37**	DVSS	PWR	Digital Ground	
45	**38**	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
48	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS Command Data: Serial data input from the µC	
50	**43**	RDATA	TS OP	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	
51	-	NC	NC	Reserved – do not connect this pin	

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
53	**44**	SSOUT	OP	SPI bus Chip Select/Frame Sync (used for CMX6x8)
52	**45**	DVSS	PWR	Digital Ground
54	**46**	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	**48**	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input
57	-	NC	NC	Reserved – do not connect this pin
58	**1**	EPSI	OP	CMX994 or Serial Memory Interface: Output; SPI bus Output
59	**2**	EPSCLK	OP	CMX994 or Serial Memory Interface: Clock; SPI bus Clock
60	**3**	EPSO	IP+PD	CMX994 or Serial Memory Interface: Input; SPI bus Input
61	**4**	EPSCSN	OP	CMX994 or Serial Memory Interface: Chip Select
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
64	**7**	DVSS	PWR	Digital Ground
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AV_{SS}). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pullup/pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{DD}	RFVDD	Power supply for RF circuits
RFV_{SS}	RFVSS	Ground for RF circuits
CPV_{DD}	CPVDD	Power supply for charge pump circuits

4 External Components

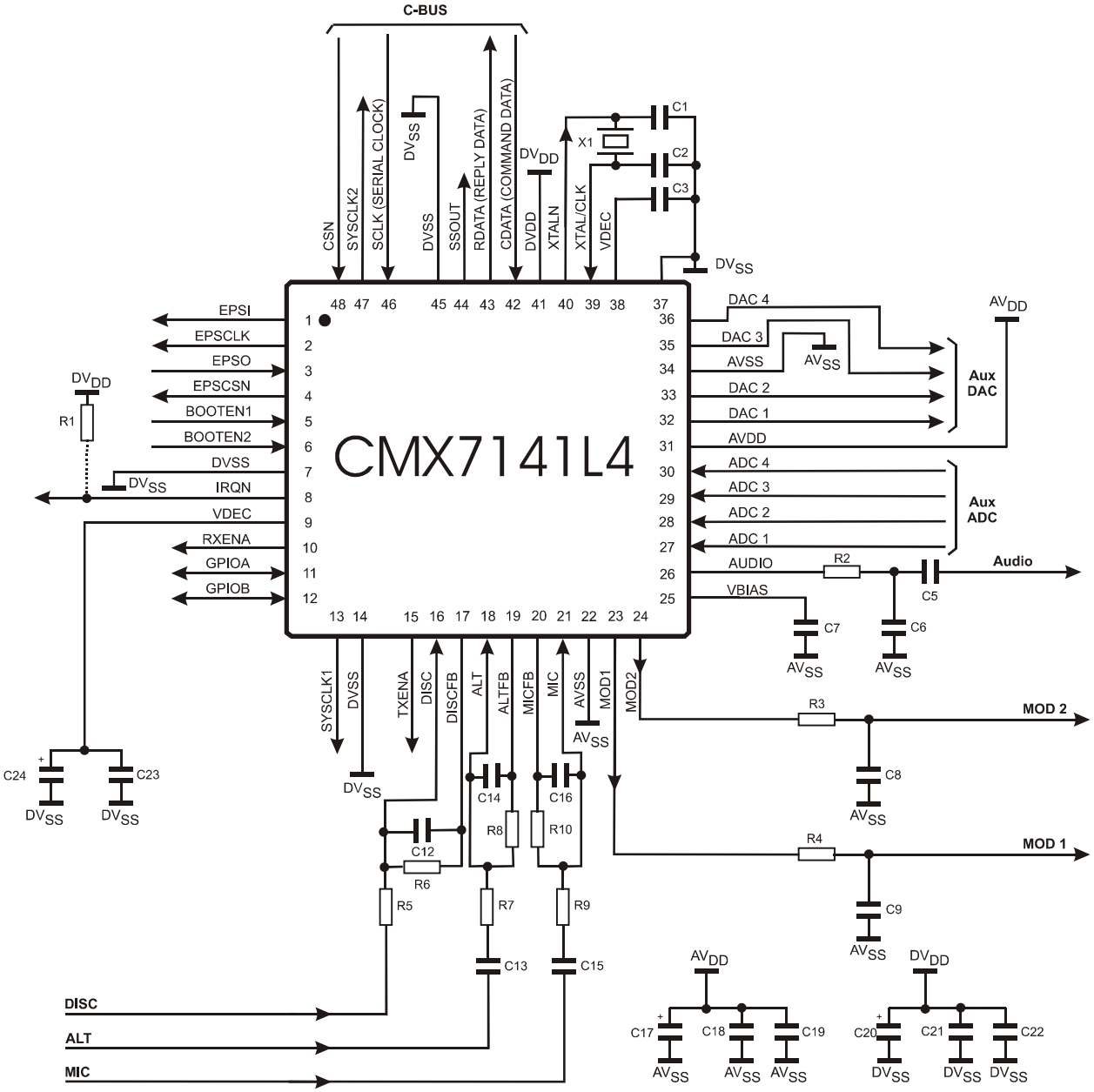


Figure 2 CMX7141 Recommended External Components

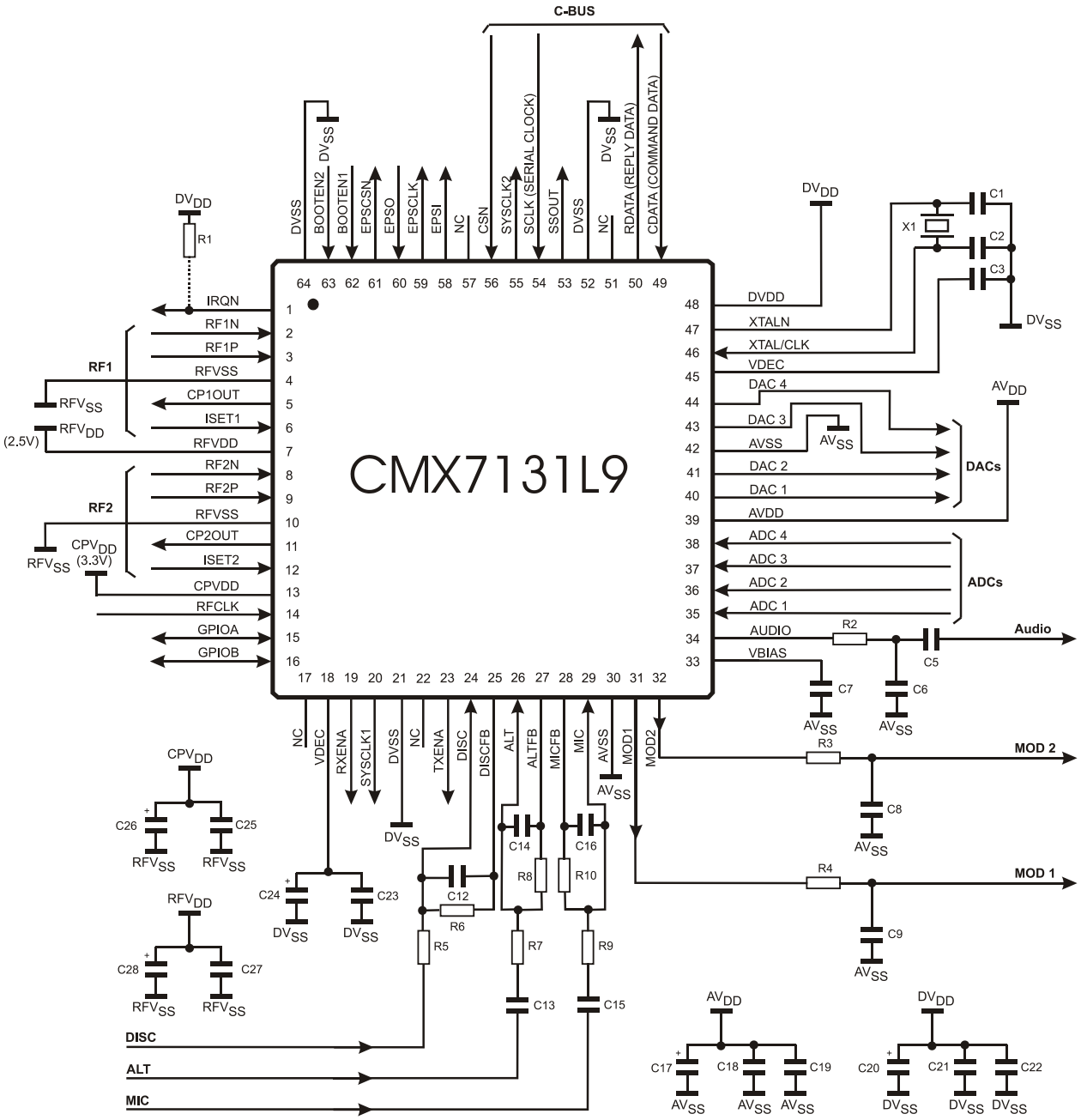


Figure 3 CMX7131 Recommended External Components

4.1 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5	C25	
R6	100kΩ	C6	100pF	C16	200pF	C26	
R7	See note 3	C7	100nF	C17	10µF	C27	
R8	100kΩ	C8	100pF	C18	10nF	C28	
R9	See note 4	C9	100pF	C19	10nF	X1	6.144MHz
R10	100kΩ	C10	*not used*	C20	10µF		See note 1

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 6.14.2. For 4FSK modulation, this signal should be DC coupled from the Limiter/ Discriminator output.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.14.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.14.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC and ALT inputs as follows:

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$
$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. AUDIO output is only used in this Function Image™ when SPI-Codec mode has been selected. It may also be used by analogue Function Images which may also be used on this device.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

4.2 PCB Layout Guidelines and Power Supply Decoupling

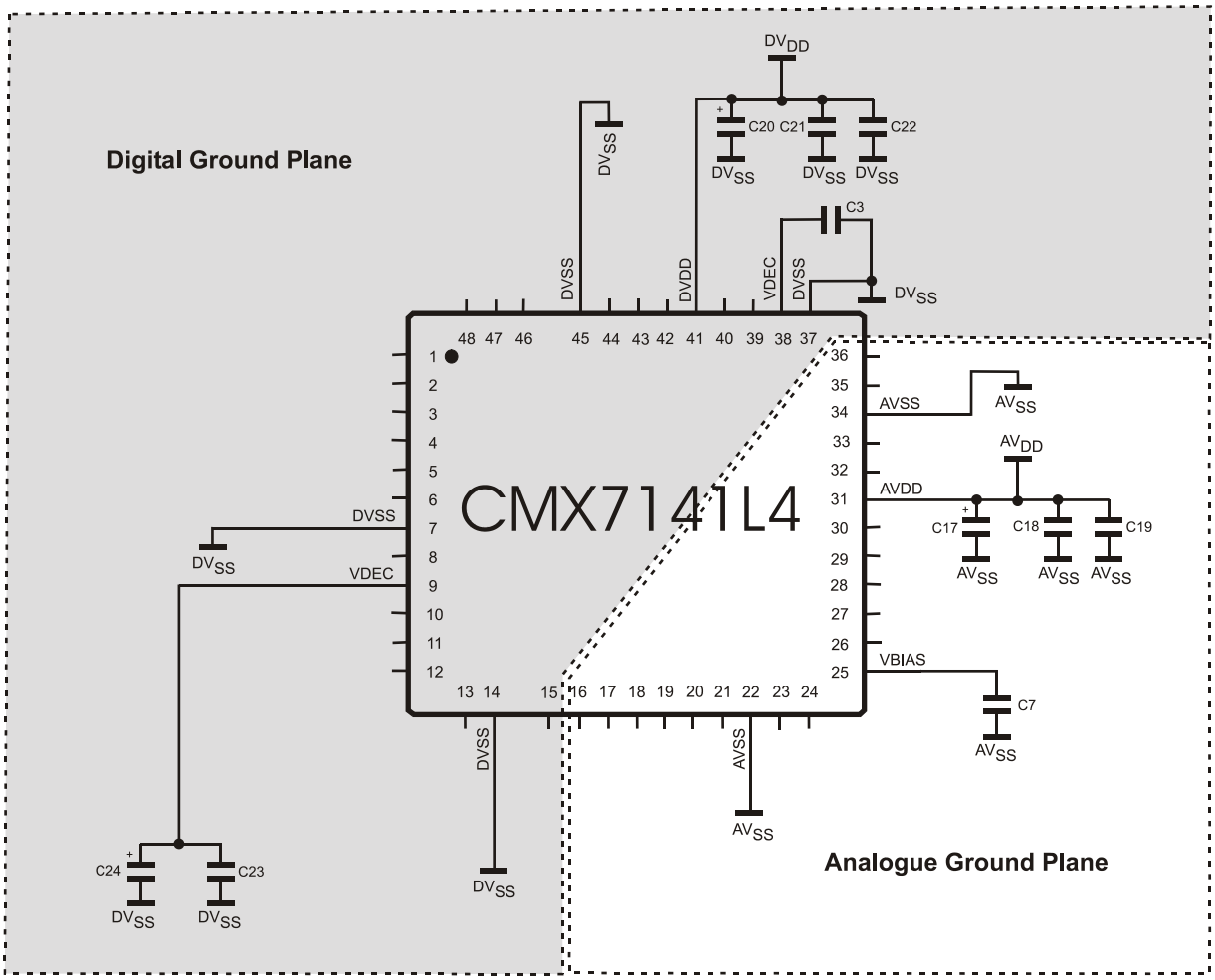


Figure 4 CMX7141 Power Supply and Decoupling

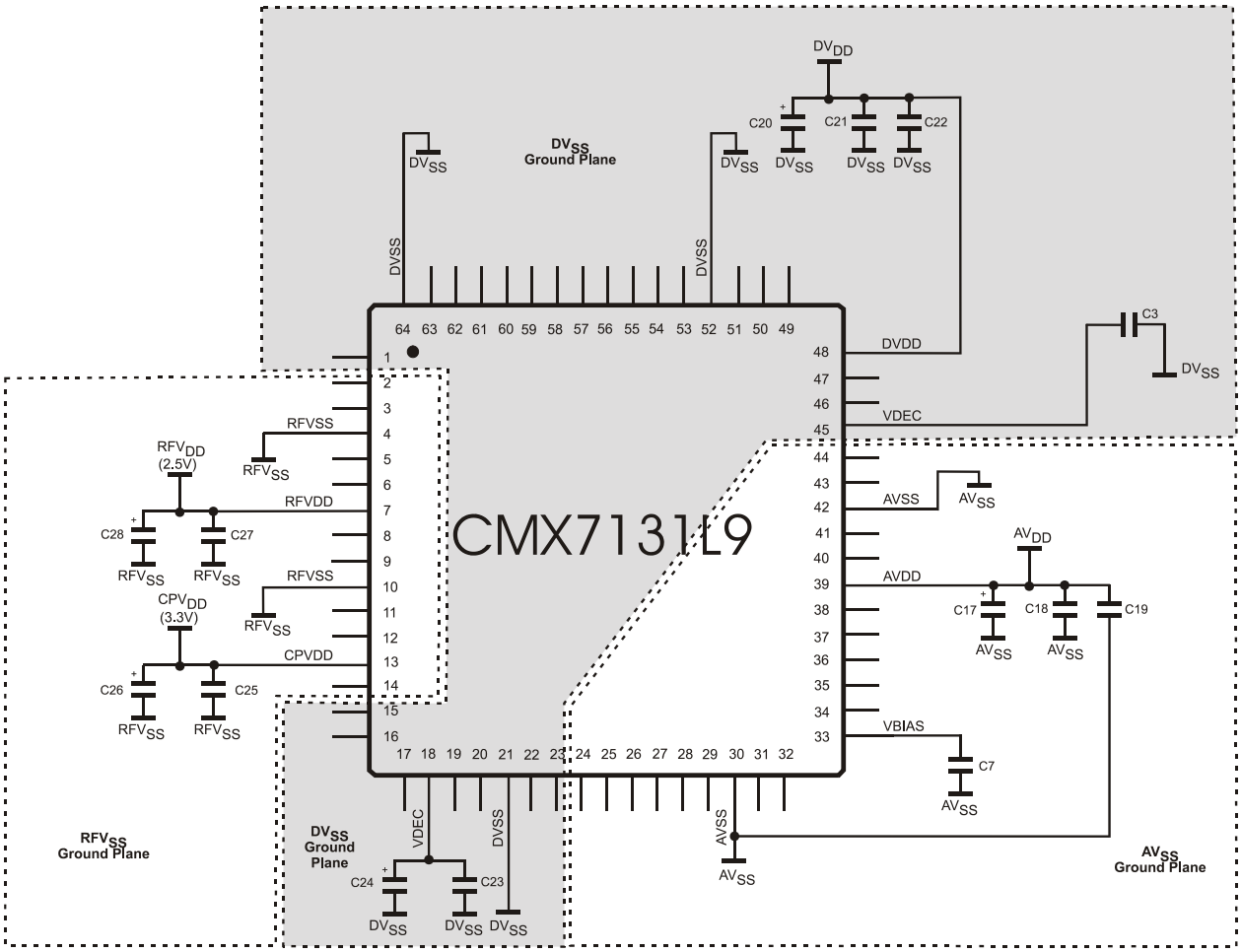


Figure 5 CMX7131 Power Supply and Decoupling

Component Values as per Figure 2

Notes:

It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the CMX7131/CMX7141 and the supply and bias decoupling capacitors. The decoupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7131/CMX7141. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7131/CMX7141, with provision to make links between them, close to the CMX7131/CMX7141. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it should be buffered with a high input-impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

4.3 CMX994 Interface

When operating the 7131/7141FI-6.1.x.x in I/Q mode the interface to the CMX994 shown in Figure 6 should be used. Component values are shown in Table 2, where values are not shown refer to the CMX994 datasheet.

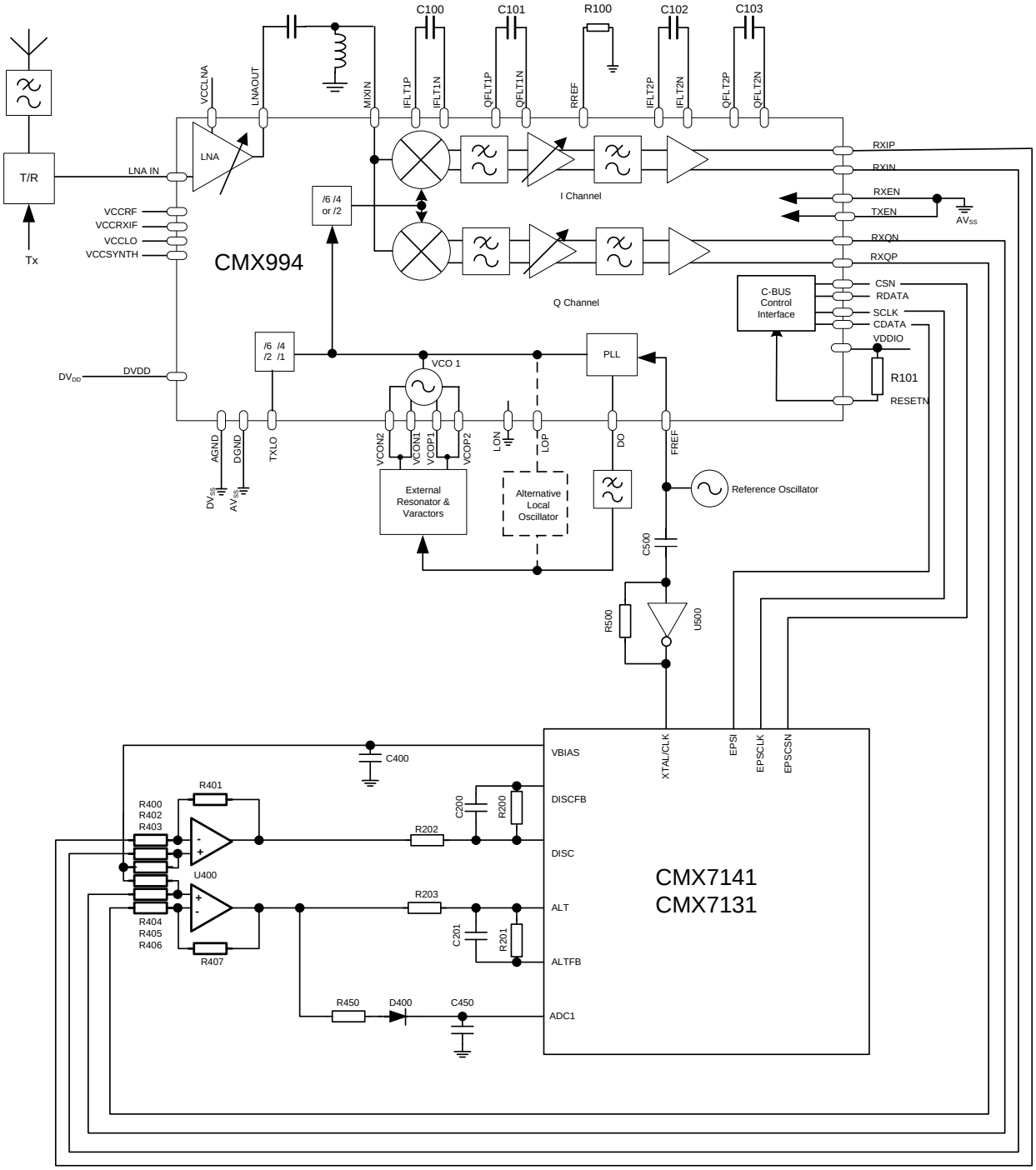


Figure 6 CMX994 Interface

Table 2 Recommended External Components when using CMX994

R100	10kΩ	C100	1.5nF	C500	1nF
R101	100kΩ	C101	1.5nF	R500	100kΩ
		C102	3.9nF	D400	MMBD1503A
R200	100kΩ	C103	3.9nF	U500	e.g. SN74AHC1G04DRL
R201	100kΩ				
R202	100kΩ	C201	100pF		
R203	100kΩ	C202	100pF		
		C450	3.3pF	U400	e.g. LM6132
R450	22kΩ	C400	100nF	R400-407	10kΩ

5 General Description

5.1 Features

7131/7141FI-6.x for the CMX7131/CMX7141 is intended for use in half-duplex digital PMR equipment using 4FSK modulation at 4800bps suitable for 6.25kHz channel systems.

Much of the ARIB STD-T102 standard air interface protocol is embedded within the CMX7131/CMX7141 operation namely:

Air Interface – Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting.

Air Interface – Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame building and synchronising
- Burst and parameter definition
- Link addressing (source and destination)
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic Own-ID detection

The 7131/7141FI-6.1 has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default and is compatible with 7131/7141FI-6.0.x for conventional limiter/discriminator receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. The transmitter can provide a conventional output suitable for 2-point modulation or for an I/Q interface.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1.

The signal processing blocks can be routed from any of the three DISC**/**ALT**/**MIC input pins.

Other Functions Include:

- Automatic Tx sequencer simplifies host control
- RAMDAC operation
- TXENA and RXENA hardware signals
- Two-point or I/Q modulation outputs
- Hard or Soft data output options.

Auxiliary Functions:

- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC
- Two RF PLLs (CMX7131 only).

Interface:

- Optimised C-BUS (4 wire high speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- C-BUS interface to CMX618/CMX608 with pass-through mode from host
- SPI bus interface for speech codec to support third-party Vocoders
- Two GPIO pins
- Serial memory boot mode
- C-BUS (host) boot mode
- Auxiliary C-BUS interface to CMX994 Direct Conversion Receiver

5.2 System Design

A number of system architectures can be supported by the device. The most highly integrated solution uses a CMX618 Vocoder under full control of the CMX7131/CMX7141, relieving the host of all vocoder management duties. In this mode audio codec functions are provided by the CMX618. The presence of the CMX618 is detected by the device automatically following power-up.

CMX618 detected	VOC_DIS	SPI-Codec	Port mode	activity
yes	0	0	C-BUS	CMX618 under automatic control. MIC and AUDIO signals routed via CMX618
yes	1	0	C-BUS	CMX618 disabled. All data passed over host C-BUS as payload data.
no	x	0	C-BUS	CMX618 disabled. All data passed over host C-BUS as payload data.

The presence of the CMX6x8 device can be verified by using the “pass-through” feature, see section 6.6.21.

Other architectures using third-party vocoders are supported using SPI-Codec mode, in which the CMX7131/CMX7141 acts as an external audio codec attached to the vocoder. In this mode, the host must issue all control commands to the vocoder and also transfer coded data packets between the vocoder and CMX7131/CMX7141. The device will automatically enable/disable the activity on the SPI-Codec port when a voice call is in progress.

In SPI-Codec mode, signed 16-bit linear PCM audio samples are transferred at 8ksps. When this mode is selected:

In Tx: the microphone input should be routed from MIC to Input2. This signal is low-passed filtered, converted to PCM data and output on the EPSI pin for the external Vocoder to process

In Rx: the Audio output should be routed from Output1. PCM data samples are read from the EPSO pin, then filtered and output via the Audio Output attenuator.

CMX618 detected	VOC_DIS	SPI-Codec	Port mode	activity
no	0	1	SPI	SPI Port enabled during Rx or Tx, PCM data from MIC/to AUDIO passed over SPI bus

The automatic enable/disable of the SPI-Codec port during Rx and Tx may be overridden by setting the VOC_DIS bit in the Modem Configuration register, $C7:b7. In this situation, the activity on the SPI-Codec port is determined by the host setting/clearing the SPI-Codec ENA, $B1:b0.

CMX618 detected	VOC_DIS	SPI-Codec	Port mode	activity
no	1	0	SPI	SPI Port disabled
no	1	1	SPI	SPI Port enabled, PCM data from MIC/to AUDIO passed over SPI bus

5.2.1 Implementation using the CMX6x8

Figure 7 shows the configuration using the CMX618 RALCWI Vocoder where all control and data is handled by the CMX7131/CMX7141 with minimal host CPU involvement:

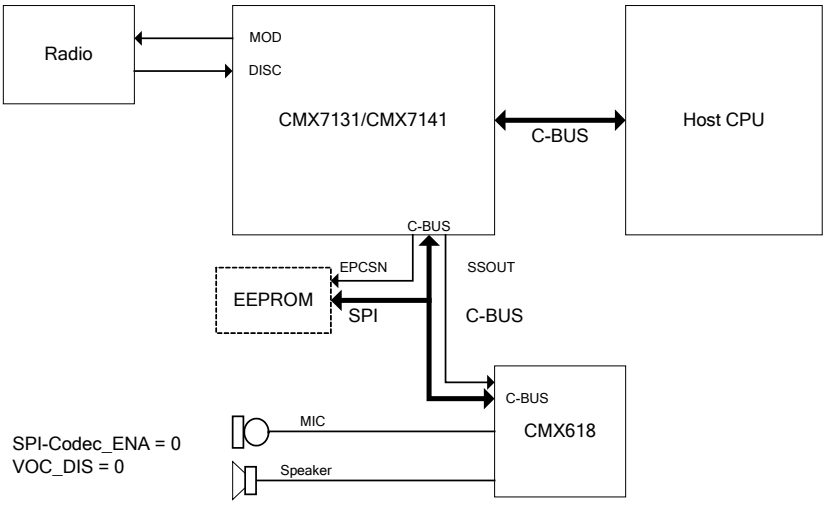


Figure 7 CMX618 Vocoder Connection

If the CMX608 is to be used, then there are two possible architectures available. If an external Audio Codec is available then the CMX7131/CMX7141 can take full control over the CMX608 as in Figure 7. Otherwise the Audio Codecs within the CMX7131/CMX7141 can be used at the expense of additional host activity. In this case, all channel data (control, addressing and payload) is transferred from the CMX7131/CMX7141 to the host over the main C-BUS interface, and the host must then transfer the Voice payload (TCH) data to the CMX608 using another C-BUS interface, as shown in Figure 8.

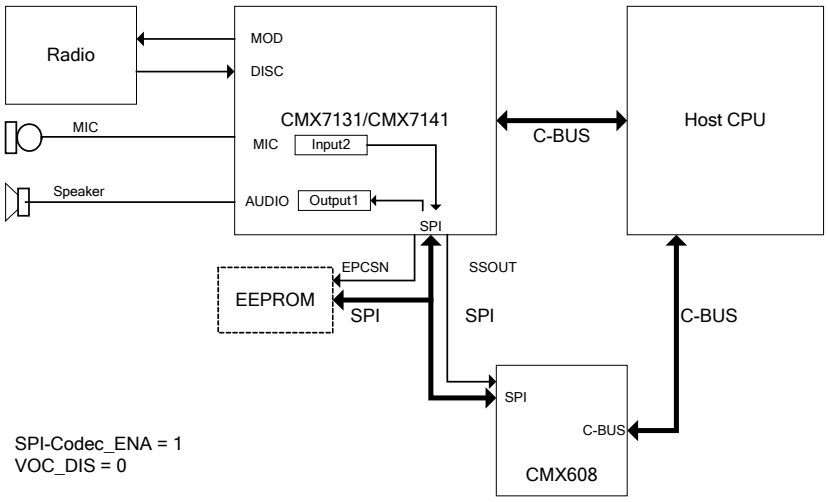


Figure 8 CMX608 Vocoder Connection

5.2.2 Implementation using Third-party Vocoders

As an alternative to the integrated architecture using the CMX618, it is possible to use a third-party Vocoders by routing all payload data (including voice traffic channel data) through the main C-BUS to the host. The host can then transfer it to/from the third party vocoder over a suitable port supported by the chosen vocoder. Typically these Vocoders do not include audio Digital-to-Analogue and Analogue-to-Digital converters, so the CMX7131/CMX7141 can be configured to use its auxiliary C-BUS as an SPI interface and use its built-in DAC/ADC's as audio converters. This architecture is shown in Figure 9.

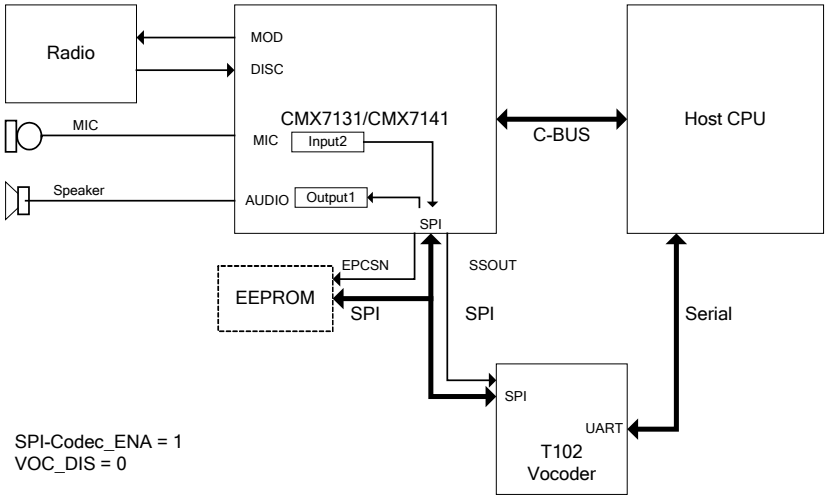
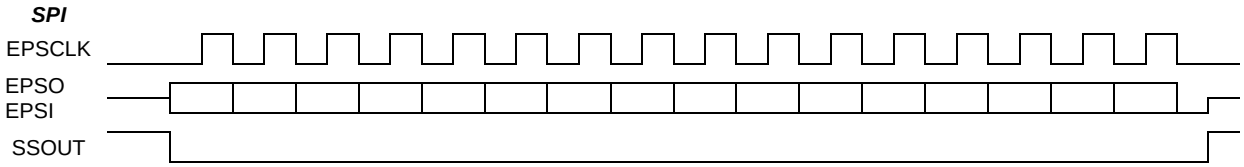


Figure 9 T102 Vocoder Connection

Table 3 SPI-Codec Format



Note: There are 16 SCLK pulses per data transfer. The default SCLK rate is 2MHz.

5.2.3 Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The CMX7131/CMX7141 can then format and transmit that data while at the same time loading in the following data blocks from the host or CMX618.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the CMX7131/CMX7141 filters, demodulates and decodes the output data before presenting it to the host or CMX618. For best performance voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format compatible with the CMX618/CMX608 and other third-party vocoders, although this mode increases the data transfer rate over C-BUS by a factor of four.

5.2.4 RSSI Measurement (LD Mode)

The AuxADC provided by the CMX7131/CMX7141 can be used to detect the Squelch or RSSI signal from the RF section while the device is in Rx or IDLE mode. This allows a significant degree of powersaving within the CMX7131/CMX7141 and avoids the need to wake the host up unnecessarily. The host programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.2.5 Serial Memory Connection (LD Mode only)

In all cases, the auxiliary C-BUS/SPI-Codec bus is shared with the serial memory bus which may be used to load the contents of the Function Image. Bus conflicts are avoided by the use of an additional chip select signal (SSOUT). If this feature is not used then the EPSCSN pin should be left un-connected. Serial Memory may not be used in I/Q interface mode.

5.2.6 CMX994 Connection (I/Q Mode only)

The CMX994 can be connected via the C-BUS connection in place of the serial memory (Table 4). This allows the CMX994 to be used along with the CMX6x8, DVSI vocoder or other third party vocoder.

Note that the data and clock connections to the CMX994 are common with the Vocoder, so the data traffic on the interface is a potential source of noise/interference in the radio.

Table 4 CMX994 Connections

CMX7131/CMX7141 Pin	CMX994 Pin
EPSCSN	CSN
EPSI	CDATA
EPSCLK	SCLK
No connection	RDATA

The operation of the CMX994 is generally automatic, however specific data may be written to CMX994 registers using the pass-through mode available using register $C8. For example if the CMX994 PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994 PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception.

5.2.7 Hardware AGC – AuxADC1 Connection

In I/Q mode, the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components, see Figure 6. This function provides a broadband signal detector which is used in the AGC process. This is required to prevent the DISC/ALT ADC inputs limiting internally in the presence of alternate channel signals, which are attenuated by the inherent filtering of the ADC.

This functionality is enabled by setting:

- Program Block P2.0:b8=1 (enable hardware AGC)
- Program Block P3.0 = $F002 (AuxADC1 averaging = 2)
- $CD = $4205 (hi threshold)
- $CD = $0200 (lo threshold)
- $A7 = $0030 (turn AuxADC1 on)

Note that threshold levels may need adjustment to suit particular hardware implementations.

5.2.8 RSSI Measurement (I/Q Mode)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 10 shows a typical response.

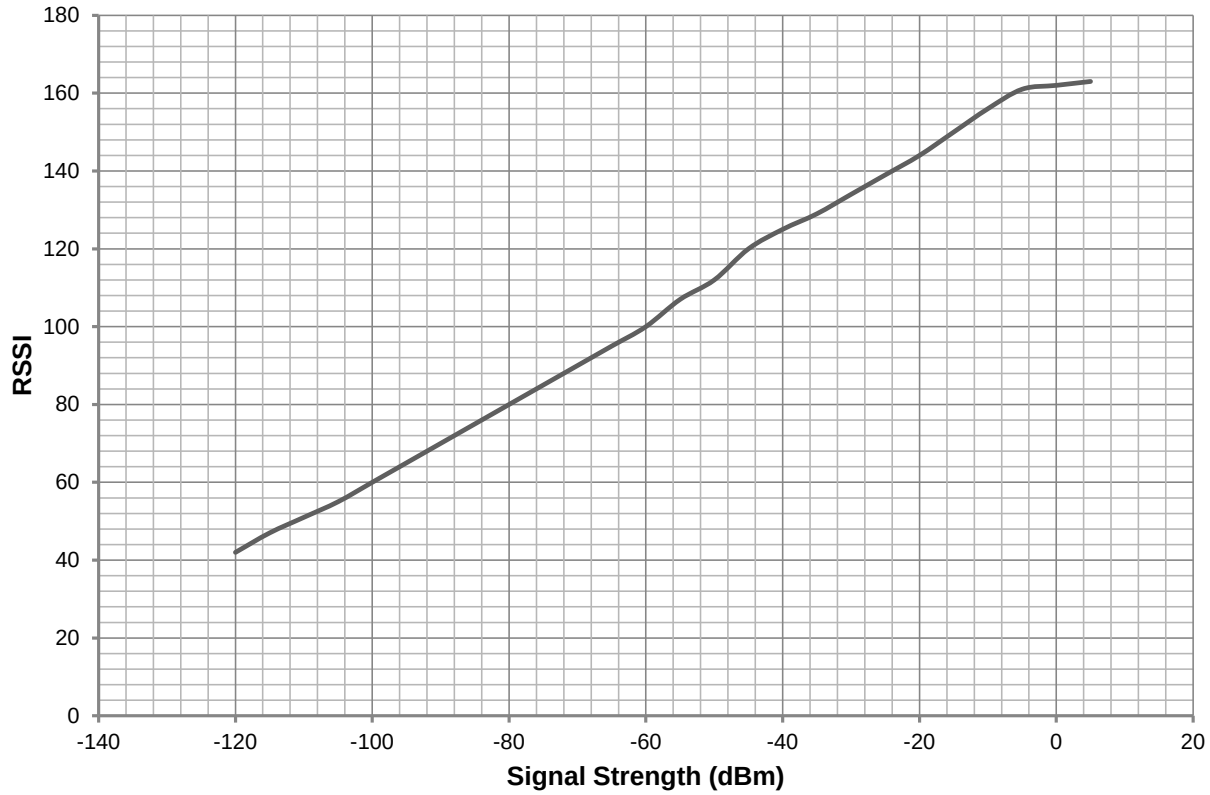


Figure 10 RSSI in I/Q Mode

5.3 Introduction

This modem runs at 4800bps occupying a 6.25kHz bandwidth RF channel. It has been designed such that, when combined with suitable RF, host controller, CMX618/CMX608 Vocoder and appropriate control software, it meets the requirements of the T102 standard.

The T102 standard specifies the AMBE Voice Coding algorithm which can be supported by transferring all payload data through the host using the main C-BUS interface. However, the CMX7131/CMX7141 also implements an automated control system for the CMX618 or CMX608 RALCWI Vocoders (also available from CML) using its auxiliary SPI/C-BUS port to issue control commands and transfer voice payload data. This substantially reduces the processing load on the host during voice calls. In the remainder of this document the CMX618 and CMX608 are referred to generically as the CMX6x8: the only significant difference is that the CMX618 provides an on-chip audio codec while the CMX608 requires an external Audio Codec.

The standard requires a 4FSK modulation scheme with an over-air bit rate of 4800bps (2400 symbols per second).

5.3.1 Modulation

The T102 4FSK modulation scheme operates in a 6.25kHz channel bandwidth with an over-air bit rate of 4800bps (2400 symbols per second). RRC filters are implemented in both Tx and Rx with a filter “alpha” of 0.2. The maximum frequency error is +/- 625Hz and the CMX7131/CMX7141 can adapt to the maximum

time-base clock drift of 2ppm over the duration of a 180-second burst. Figure 13 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

Figure 11 and Figure 12 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36k span and zero-span mode, having been 2-point modulated using a suitable RF transmitter.

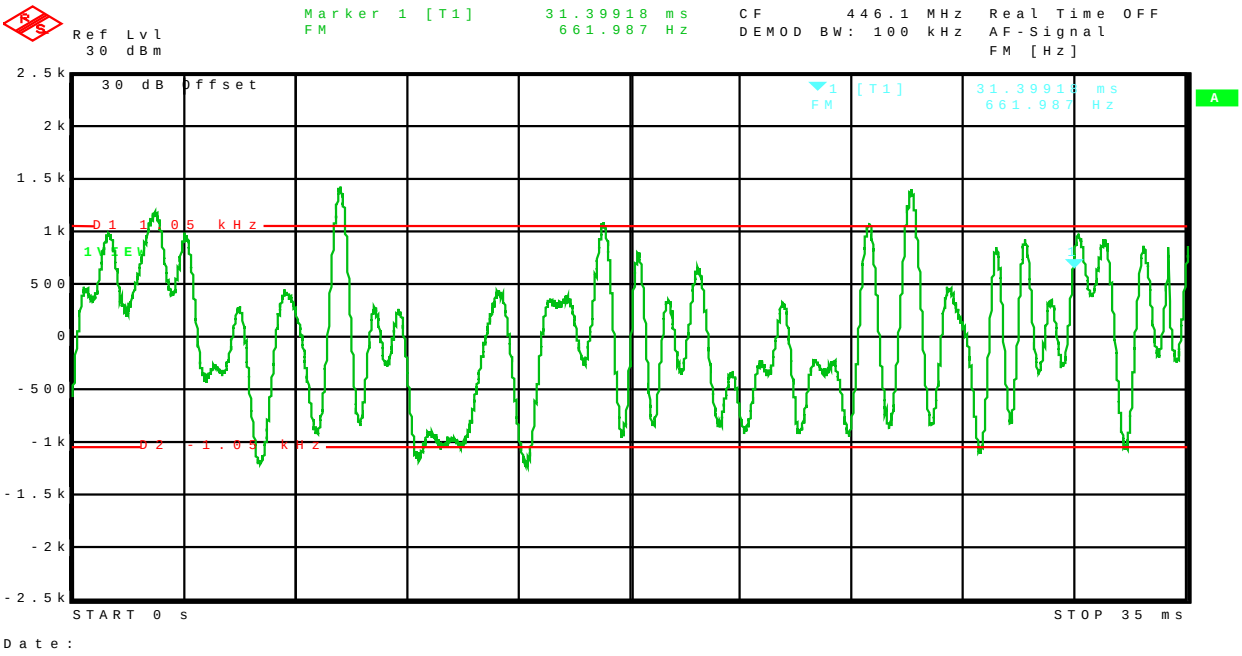


Figure 11 4FSK PRBS Waveform - Modulation

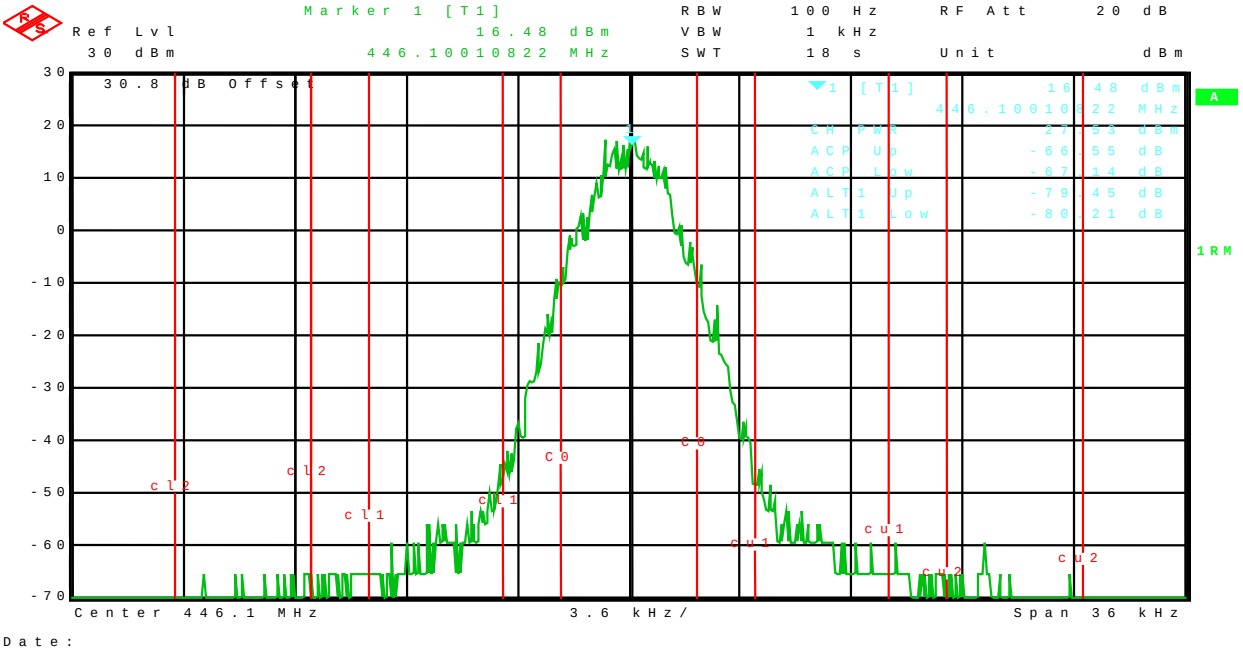
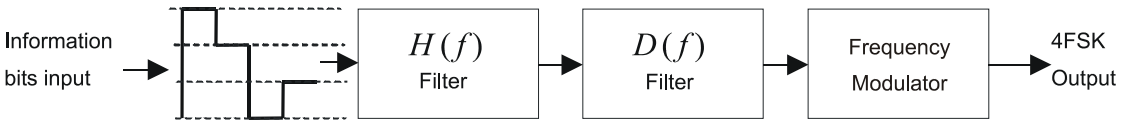


Figure 12 4FSK PRBS Waveform - Spectrum

Tx Baseband Filter



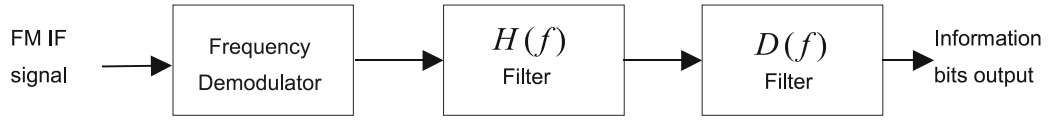
$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\sin(\pi fT)}{\pi fT}$$

4FSK Deviation		
Di-bit	Symbol	Deviation
01_2	+3	+945Hz
00_2	+1	+315Hz
10_2	-1	-315Hz
11_2	-3	-945Hz

Rx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\pi fT}{\sin(\pi fT)}$$

Figure 13 Modulation Characteristics

5.3.2 Internal Processing

The CMX7131/CMX7141 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power IDLE mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 14. Additional processing in I/Q Mode is shown in Figure 15.

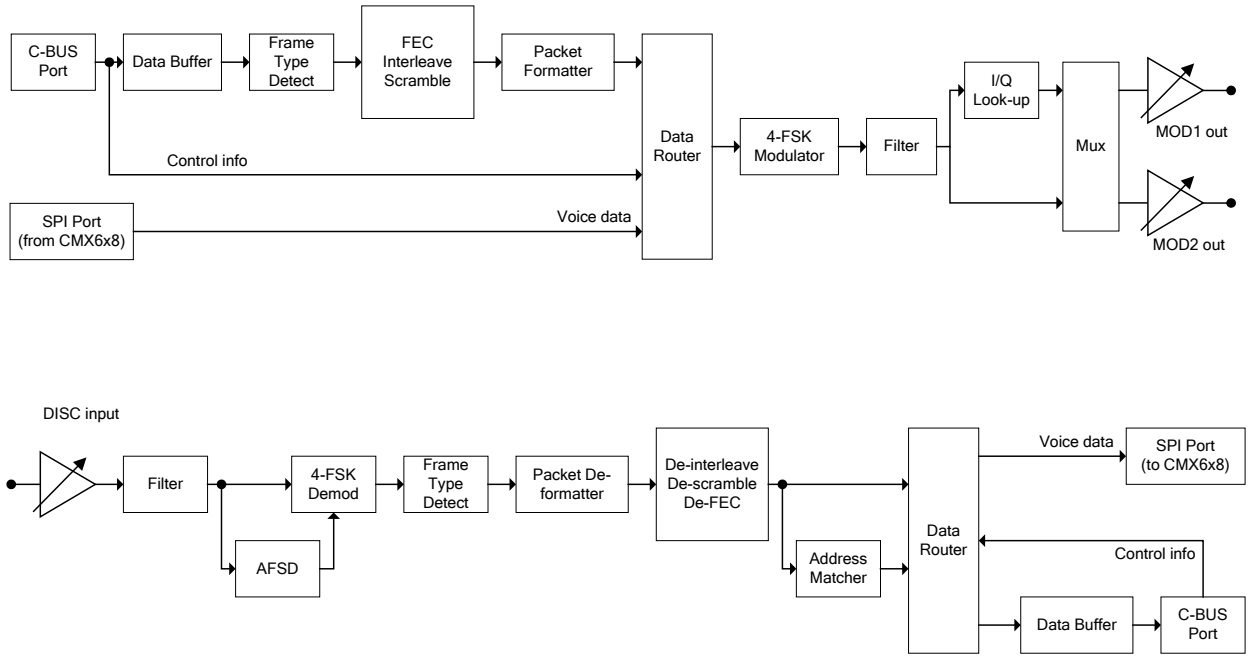


Figure 14 Internal Data Blocks (LD Mode)

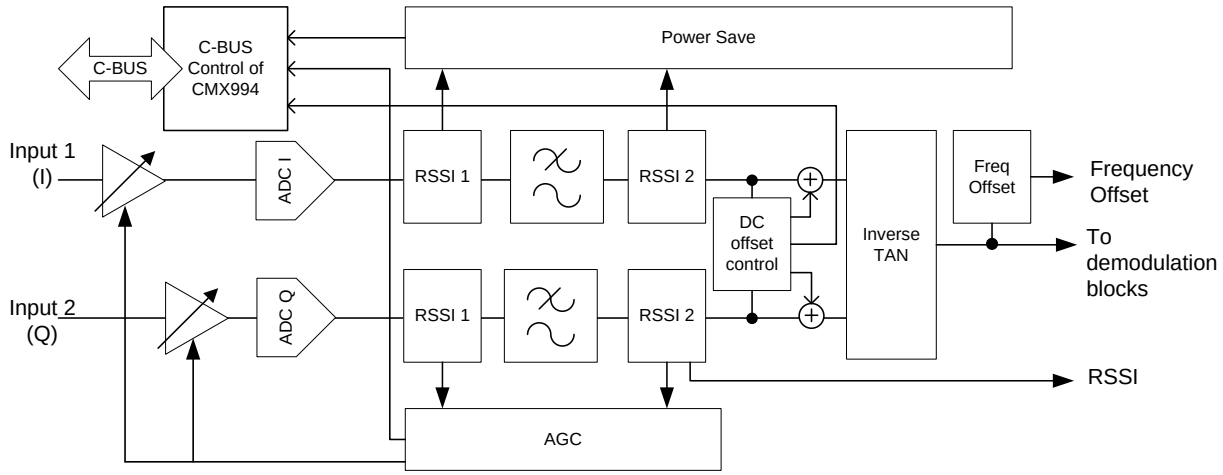


Figure 15 Additional Internal Data Processing in I/Q Mode

5.3.3 Frame Sync Detection and Demodulation

The analogue signal from the receiver may be from either a CMX994 I/Q interface or a limiter/discriminator (LD) output. The signal(s) from the RF section should be applied to the CMX7131/CMX7141 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx). The signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the CMX7131/CMX7141 Input Gain settings. In LD mode the signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the data-processing sections that follow are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. The

CMX7131/CMX7141 can detect the end of a burst by scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

In I/Q mode filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before RRC filtering, after which the signal chain is then the same as the LD case. In I/Q mode the CMX7131/CMX7141 provides measurements of frequency error and RSSI (which are not available in LD mode).

A T102 call consists of a series of 80ms frames, each starting with a 20-bit Synchronisation Word (SW). The first frame is preceded by a Preamble sequence, and the CMX7131/CMX7141 uses the last 18 bits of the Preamble together with the first Synchronisation Word to detect the start of a transmission. This is reported to the host by setting the FS1 Detect bit in the Status register.

Last 9 Symbols of Preamble: `xx11 0111 0101 1111 1101 ($375FD)`

Synchronisation Word: `1100 1101 1111 0101 1001 ($CDF59)`

The CMX7131/CMX7141 can optionally also detect the Synchronisation Word sequence in isolation to perform “late entry” into an existing call. This is reported to the host by setting the FS2 Detect bit in the Status register. The short length of the Synchronisation Word gives a high probability of false detections, so by default the CMX7131/CMX7141 will only generate an initial FS2 Detect if two successive Synchronisation Words are detected at the correct frame spacing in the received signal.

Additionally, once initial synchronisation has been achieved with an FS1 or FS2 Detect, it can later be re-established from a single Synchronisation Word received within ±2 symbols of the original frame timing. This mode slightly increases power consumption in order to maintain the symbol timer through Rx-Tx-Rx or Rx-IDLE-Rx transitions, and hence is selectable using b13 of the modem configuration register, $C7. Note that this also requires b8 of $C7 to be set in order to enable FS2 detects.

When frame synchronisation has been achieved and the 4FSK demodulator has been enabled, Frame Sync detection is switched off and any subsequent Preamble or Synchronisation Word sequences in the received data are not reported to the host.

Table 5 T102 Frame Format – Audio Communication

bits:	>24	20	16	60	144	144
	P	SW	RI	SACCH	FACCH1	FACCH1
		SW	RI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	RI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	RI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	RI	SACCH	TCH1	TCH2	TCH3	TCH4
	Repeat SCs until PTT released….							

Table 6 T102 Frame Format – Data Communication

bits:	>24	20	16	348
	P	SW	RI	UDCH1 or FACCH2

Table 7 T102 Frame Format – Data Burst Operation

bits:	>24	20	16	252	96
	P	SW	RI	UDCH2	G

P = Preamble (optional)

SW = Synchronisation Word

FS1 = 18 bits Preamble + 20 bits SW

FS2 = 20 bits SW

RI = RICH (Radio Information Channel)

SACCH = Slow Associated Control Channel

FACCH1 = Fast Associated Control Channel 1 (144 bits)

FACCH2 = Fast Associated Control Channel 2 (348bits)

TCHx = Traffic/Payload Data (72 bits)

UDCH1 = User Data Channel 1 (348 bits)

UDCH2 = User Data Channel 2 (252 bits)

G = Guard time (96 bits)

In Tx and Rx mode, the Preamble and Synchronisation Word are handled automatically and do not need to be loaded by the host.

It is possible to substitute FACCH1 blocks for TCH blocks during a call (frame stealing), in which case the vocoder should either be fed a silence frame or repeat its last data.

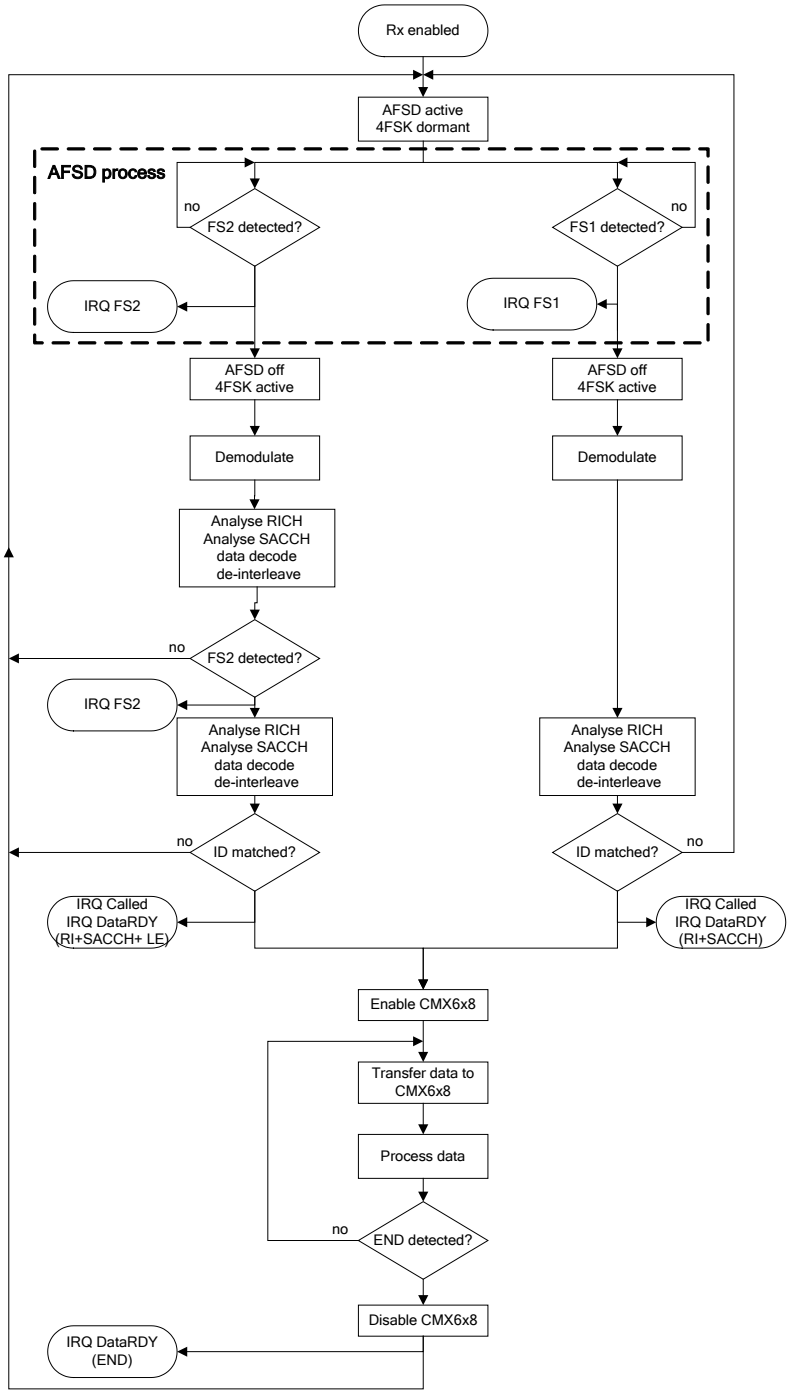


Figure 16 FS Detection

5.3.4 FEC and Coding

The CMX7131/CMX7141 implements all CRCs, convolutional codes, interleaving and scrambling required by the T102 standard. CRC failures in control channel fields and coded data blocks are indicated to the host by issuing an “Event” IRQ with a corresponding error code in the Modem Status register, $C9. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7131/CMX7141.

Table 8 Frame Types

Frame type	Un-coded data bits (C-BUS interface)	Coded data bits (over-air)	Notes:
RICH	7	16	
SACCH	8 + 18	60	User ID in the SU field
FACCH1	80	144	
FACCH2	8 + 176	348	User ID in the SU field
UDCH1	8 + 176	348	User ID in the SU field
UDCH2	252	252	No coding defined
TCHx	72	72	Coding applied by vocoder

Note: FACCH1, FACCH2, UDCH1, UDCH2 and TCHx are all regarded as payload data. If the “Softcoded” function is enabled, in Rx mode this data will be reported as a 4-bit code per data bit.

5.3.5 Voice Coding

A CML CMX618 or CMX608 RALCWI Vocoder can be used under the control of the CMX7131/CMX7141. The CMX7131/CMX7141 provides an auxiliary SPI/C-BUS port (shared with the boot serial memory) which is used to issue control commands and transfer voice payload data directly to the CMX6x8 Vocoder, minimising the loading on the host controller during voice calls.

Alternatively, the CMX7131/CMX7141 can support any third-party vocoder by routing voice payload data over the main C-BUS interface and through the host. In this mode, all vocoder control and data transfers must be managed by the host.

Voice data transferred to the CMX6x8 in Rx mode always uses soft decision (4-bit log-likelihood ratio) format. This option is also available for voice payload data routed to the host, although it increases the required data transfer rate over C-BUS by a factor of four.

5.3.6 Radio Performance Requirements

In LD mode, for optimum performance, the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.

In I/Q mode the recommended interfacing to the CMX994 should be used, see section 4.3. The CMX7131/CMX7141 includes digital filters to provide adjacent channel rejection while compensating for the in-band response of the CMX994 I/Q filters.

Further information and application notes can be found at http://www.cmlmicro.com .

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7131/CMX7141 is designed to work with an external frequency source of 19.2MHz. If this default configuration is not used, then Program Block 3 must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of common values can be found in Table 9. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24MHz can be used.

The register values in Table 9 are shown in hex, the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 9 Xtal/Clock Frequency Settings for Program Block 3

Program Block			External frequency source (MHz)							
			3.579	6.144	9.216	12.0	12.8	16.368	16.8	**19.2**
P3.2	IDLE	GP Timer	*$017*	$018	$018	$019	$019	*$018*	$019	**$018**
P3.3	IDLE	VCO output and AUX clk divide	*$085*	$088	$08C	*$10F*	*$110*	*$095*	*$115*	**$099**
P3.4	Rx or Tx	Ref clk divide	*$043*	$040	$060	$07D	$0C8	$155	$15E	**$0C8**
P3.5	Rx or Tx	PLL clk divide	*$398*	$200	$200	$200	$300	$400	$400	**$200**
P3.6	Rx or Tx	VCO output and AUX clk divide	*$140*	$140	$140	$140	$140	$140	$140	**$140**
P3.7	Rx or Tx	Internal ADC/DAC clk divide	*$008*	$008	$008	$008	$008	$008	$008	**$008**

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7131/CMX7141 and the host µC; this interface is compatible with Microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.6.2.

The CMX7131/CMX7141 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

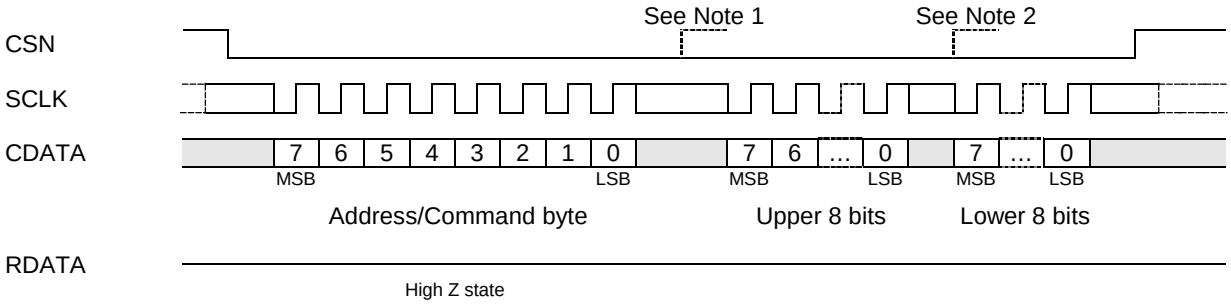
6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7131/CMX7141's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7131/CMX7141's write only Registers, or one or more data byte(s) read out from one of the CMX7131/CMX7141's read only Registers, as shown in Figure 17.

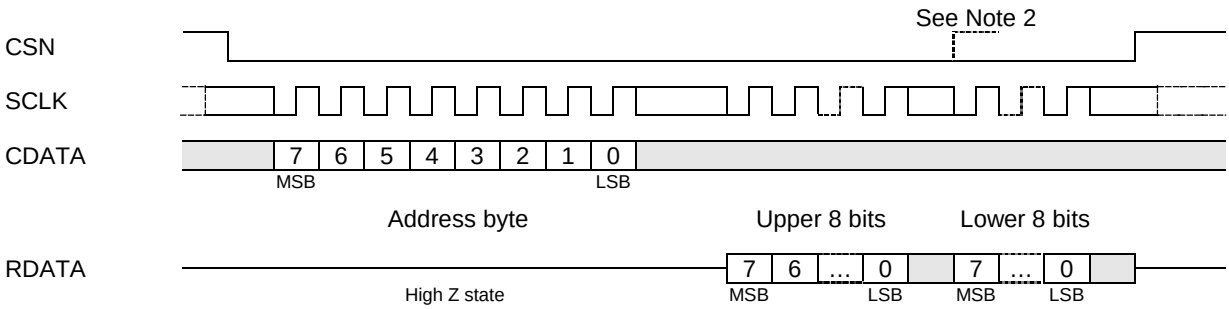
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7131/CMX7141 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7131/CMX7141 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 17 C-BUS Transactions

Notes:

1. For Command byte transfers, only the first 8 bits are transferred ($01 = General Reset)
2. For single byte data transfers, only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer
4. The SCLK input can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

***NOTE**:FI loading from serial memory is not supported when FI-6.1 is used in I/Q mode because the serial memory interface is used for CMX994 control.*

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The maximum possible size of Function Image™ is 46kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable

throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7131/CMX7141 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220kΩ resistor (see Table 10).

For serial memory load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the serial memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 10). The serial memory interface is shared with the Auxiliary C-BUS port which controls the CMX6x8 Vocoder using a separate chip select (SSOUT) pin. During boot operations, the SSOUT will be disabled. Once the boot operation has completed, the serial memory chip select (EPSCSN) will be disabled and the SSOUT will become operational.

Once the FI has been loaded, the CMX7131/CMX7141 performs these actions:

(1) The product identification code ($7141 or $7131) is reported in C-BUS register $C5
(2) The FI version code is reported in C-BUS register $C9
(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) Once activated, the device initialises fully, enters IDLE mode and becomes ready for use, and the Programming flag (bit 0 of the Status register) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 10 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
reserved	1	0
Serial Memory load	0	1
No FI load	0	0

Note: Following a General reset, reloading of the Function Image is strongly recommended.

6.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7131/CMX7141 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7131/CMX7141 powered up and placed into Program mode, the data can then be sent directly over the C-BUS to the CMX7131/CMX7141.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.

Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to the Programming register has been accepted. The PRG flag state can be determined by polling the Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete (host dependent).

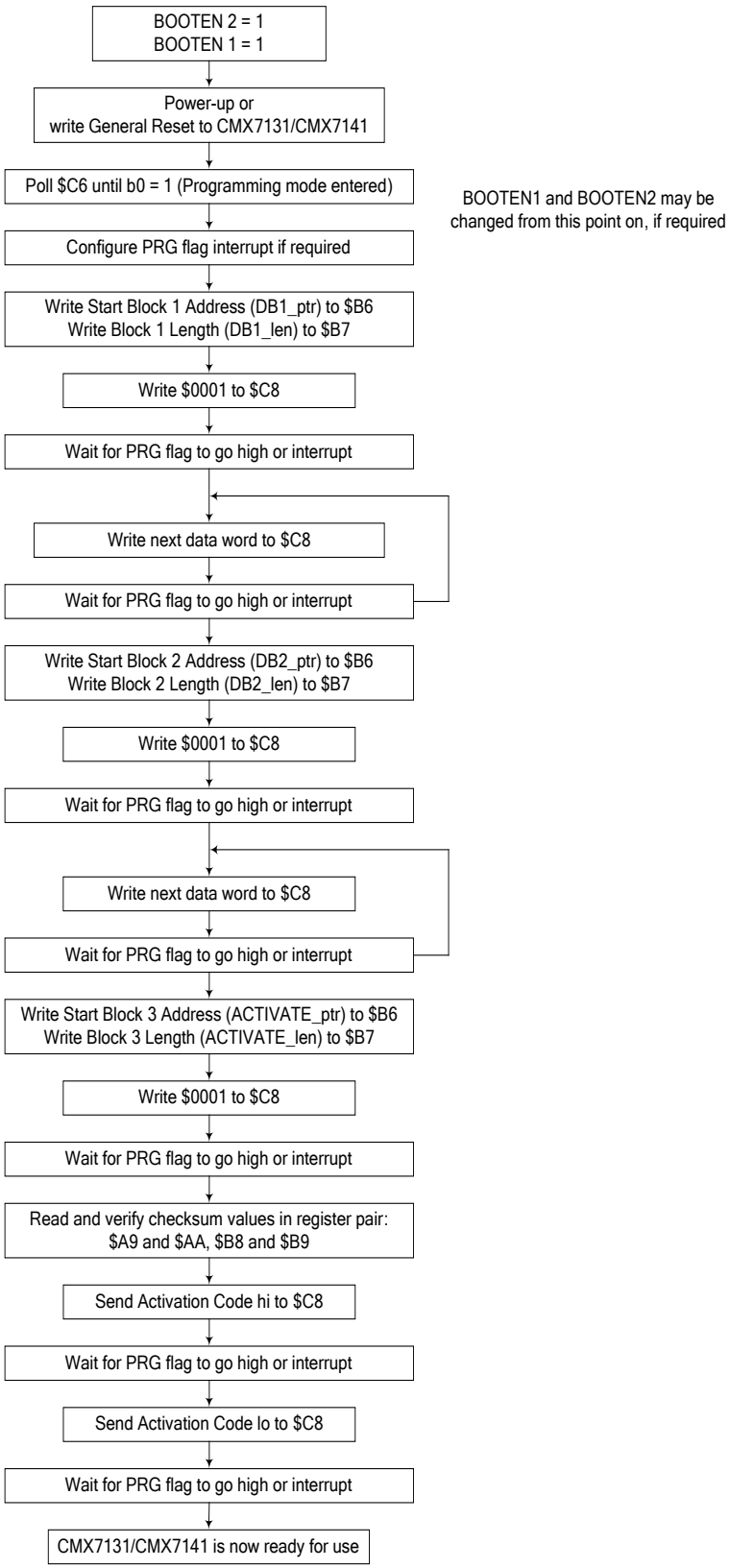


Figure 18 FI Loading from Host

6.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The CMX7131/CMX7141 needs to have the BOOTEN pins set to serial memory load, and then, on power-on, or following a C-BUS General Reset, the CMX7131/CMX7141 will automatically load the data from the serial memory without intervention from the host controller.

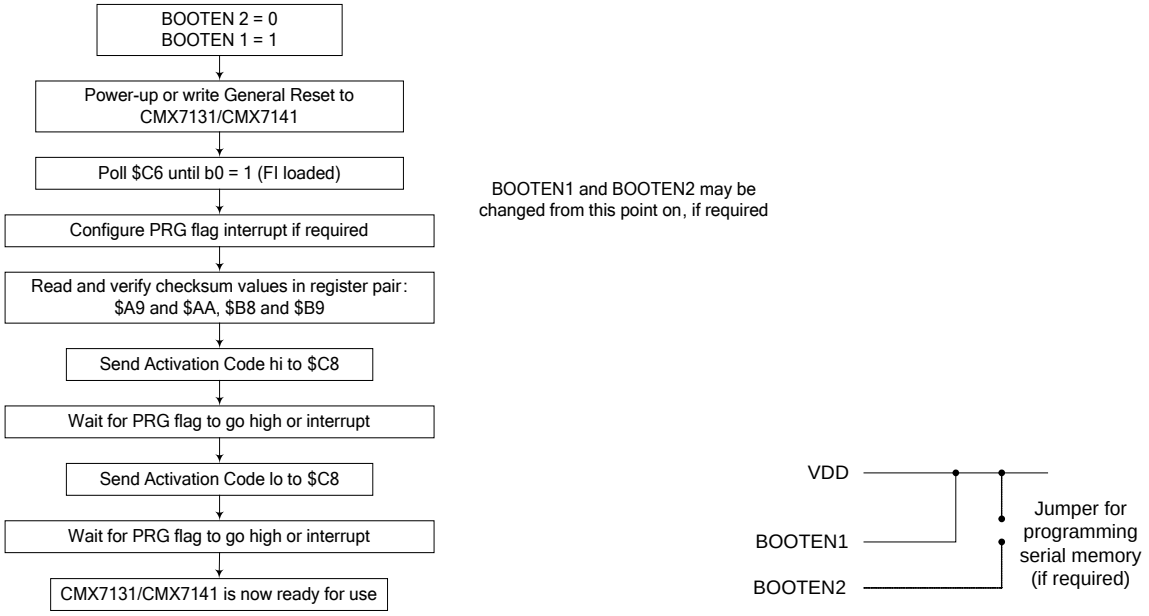


Figure 19 FI Loading from Serial Memory

The CMX7131/CMX7141 has been designed to function with the Atmel AT25HP512 serial EEPROM and the AT25F512 flash EEPROM devices[2], however other manufacturers' parts may also be suitable. The time taken to load the FI is dependent on the Xtal frequency; with a 6.144MHz Xtal, it should load in less than 1 second.

***NOTE**:FI loading from serial memory is not supported when FI-6.1 is used in I/Q mode.*

[2] Note that these two memory devices have slightly different addressing schemes. FI-6.x is compatible with both schemes.

6.4 CMX618/CMX608 C-BUS Interface

An auxiliary SPI/C-BUS interface is provided which allows the CMX6x8 vocoder to be directly controlled by the CMX7131/CMX7141 without the need for the host to intervene. This is accomplished by multiplexing the serial memory SPI interface with the additional chip select pin SSOUT. The serial memory Data Out pin MUST NOT drive the CMX7131/CMX7141 EPSO pin when the serial memory is disabled, otherwise the CMX6x8 will not be able to return its data to the CMX7131/CMX7141. The CMX7131/CMX7141 Auxiliary SPI/C-BUS interface bus should be connected to the C-BUS interface on the CMX6x8 using the SSOUT pin as the CSN signal for the CMX6x8 running in C-BUS mode (this is the default setting of the SPI-Codec ENA pin, $B1 bit 0). Following receipt of the Activation Codes at power-on, the Function Image™ will automatically select C-BUS mode and poll the interface to see if a CMX6x8 is connected on its C-BUS port. The default settings of the Vocoder 1 Enable Program registers (P1.11 and P1.12) are set for the RALCWI coding format.

The initialisation and operational settings of the CMX6x8 should be programmed by the host into the CMX7131/CMX7141 Program Block 1 on power-up. These values will be written to the defined registers in the CMX6x8 at:

- Initialisation
- IDLE mode
- Rx mode
- Tx mode.

Mic Gain and Speaker Gain commands may be sent to the CMX6x8 whenever the CMX7131/CMX7141 is in Rx or Tx mode.

DTMF mode 2, DTX, and VAD modes of the CMX6x8 are not supported in this FI. DTMF Mode 1 (transparent) is supported.

The default settings for the CMX6x8 are:

- 4-frame packet (80ms) with FEC no STD, no DTMF
- 2400bps with FEC
- Internal Sync
- Throttle = 1
- Internal Codec
- IRQ disabled
- Soft Coded data bits.

The connections for the CMX6x8 Vocoder are shown Table 11.

Table 11 CMX6x8 Vocoder Connections

CMX7131/CMX7141 Pin	CMX6x8 Pin
SSOUT	CSN
EPSI	CDATA
EPSO	RDATA
EPSCLK	CLK
No connection	IRQN (tied to V_{DD} via 100kΩ resistor).

Figure 20 shows one possible implementation of the CMX7141 combined with a CMX618, a host µController and suitable RF sections to provide a digital PMR radio. The bold lines show the active signal paths in Rx and Tx respectively.

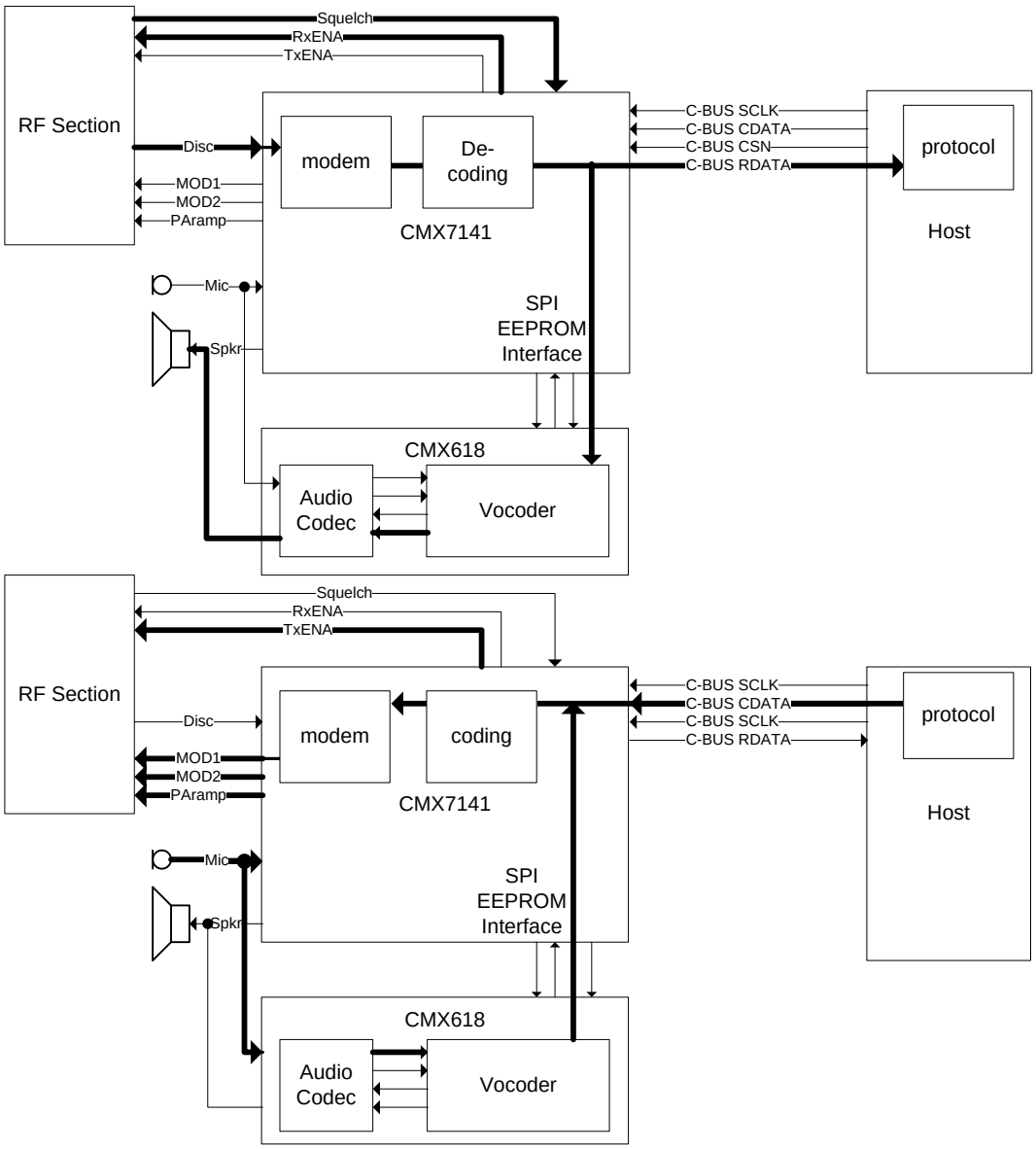


Figure 20 Digital Voice Rx and Tx Blocks

The paralleling of the microphone and speaker connections between the CMX618 and the CMX7131/CMX7141 is only required if the CMX7131/CMX7141 is also to provide analogue PMR functionality. Otherwise, the microphone and speaker should be connected to the CMX618 only. The CMX618 RALCWI Vocoder provides an on-chip audio and voice codec, but alternatively a CMX608 device could be used along with an external audio codec. Voice payload data is transferred directly from and to the CMX618 by the CMX7131/CMX7141. Note that the CMX618 Audio output does not have a high impedance mode, therefore an external analogue switch is required if the Analogue FI-2.x is to be used on the device to isolate it.

6.5 T102 Standard Vocoder Interface

If the T102 standard vocoder (or other a third-party vocoder) is used all radio channel data will need to be transferred over the main C-BUS through the host. In this case the Vocoder 1 Enable Program registers (P1.11 and P1.12) should be set appropriately and the SPI-Codec ENA bit ($B1 bit 0) should be set to 1.

To speed the power-on process, the automatic presence check for the CMX6x8 may be skipped by setting the SPI-Codec ENA bit BEFORE the activation codes are loaded during the power-on sequence.

The connections for the T102 standard vocoder are shown in Table 12.

Table 12 T102 Standard Vocoder Connections

CMX7131/CMX7141 Pin	Standard Vocoder Pin
SSOUT	SPI_STE
EPSI	SPI_RX_DATA
EPSO	SPI_TX_DATA
EPSCLK	SPI_CLK and SPI_CLK_IN.

6.5.1 Support for I²S Mode

The device can support I²S interfaces in mono, 16-bit mode only, for transmitting and receiving audio codec data using the SPI bus. This mode is selected in Program Block 1 of the Programming register (see section 8.2.2). Figure 21 shows typical transmit waveforms.

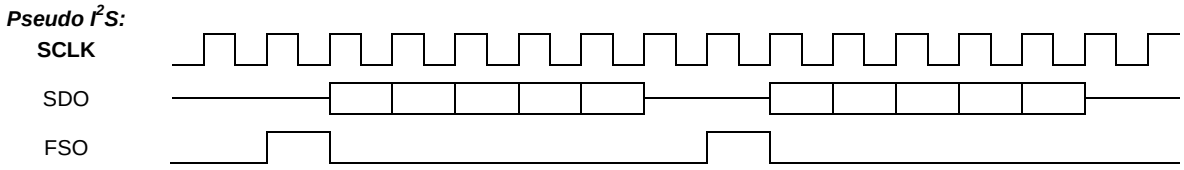


Figure 21 I²S Mode Support

6.6 Device Control

The CMX7131/CMX7141 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required Signal Routing and Gain

(4) Use the Modem Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into IDLE mode. This will also command the CMX6x8 to enter a power saving mode as well. Additional power savings can be achieved by disabling any unused hardware blocks but care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the input or output blocks to function.

See:

- Power Down Control - $C0 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

6.6.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Modem Control - $C1 write
- Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- TxAuxData - $C2 write
- CMX6x8 Analogue Gain- $C3 write.

Setting the Modem Mode to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the CMX6x8 out of its powersave mode, whilst setting the Modem Mode to IDLE Mode will automatically return the internal clock to a lower (powersaving) speed. To access the Program blocks (through the Programming register, $C8) the device MUST be in IDLE mode.

Under normal circumstances the CMX7131/CMX7141 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

6.6.2 Interrupt Operation

The CMX7131/CMX7141 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) of the Interrupt Mask register are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the PRG flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The PRG flag is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- Status - $C6 read
- Interrupt Mask - $CE write.

Continuous polling of the Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host I/O pin and poll this pin instead.

6.6.3 Signal Routing

The CMX7131/CMX7141 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.

See:

- Input Gain and Signal Routing - $B1 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

The analogue gain/attenuation of each input and output can be set individually, with additional fine attenuation control available via the Program Blocks in the CMX7131/CMX7141. The Mic and Speaker gains are set by the CMX6x8, which is controlled through the CMX6x8 Analogue Gain- $C3 write of the CMX7131/CMX7141.

See:

- Analogue Output Gain - $B0 write (Tx MOD 1 and 2)
- Input Gain and Signal Routing - $B1 write (Rx DISC input, Tx MOD 1 and 2)
- CMX6x8 Analogue Gain- $C3 write (CMX6x8 Mic and Speaker).

In common with other FIs developed for the CMX7131/CMX7141, this device is equipped with two signal processing paths; in this implementation of the FI, Input2 is only used in SPI-Codec mode for the Tx audio

signal. Input1 should be routed to one of the three input sources (ALT, DISC or MIC) which should be connected to the radio's discriminator output. The internal signals Output 1 and 2 are used to provide either 2-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required. In I/Q mode input 1 should be routed to the DISC input source for the I channel input and input 2 should be routed to the ALT input source for the Q channel input.

It is important to correctly attach the signal from the CMX994 I/Q outputs to the CMX7141 DISC and ALT inputs. Crossing these connections will cause the CMX7141 dc offset calibration to fail, as attempted corrections to the I signal will be made to the Q signal and vice versa. Crossed connections can be swapped using the Input Gain and Signal Routing register ($B1:b5-2). Likewise, it is important that the sense of connection is correct between the CMX994 and CMX7141. If the input signals are inverted then attempts by the CMX7141 to remove the dc offset will, in fact, increase the dc offset. The inputs may be inverted by using the 'Input Invert' bit in the Analogue Output Gain register ($B0:b7). When demodulating the received signal (internally to the CMX7141), it is possible that the signal could be inverted, resulting in no framesync detection and, in effect, inverted data. Often this can be corrected by swapping the I and Q signals (changing the signal that leads in phase to the one that lags). However, the relationship between I/Q outputs of the CMX994 and the CMX7141 DISC and ALT inputs must be maintained as described above. Therefore the demodulated signal can be inverted using Programming Register block 0, P0.10 bit1 (IFD).

In T102 formatted modes, the microphone and speaker functions can be automatically routed using the CMX6x8 Vocoder as appropriate. This is controlled by the SACCH "Information Type" field which indicates whether the payload is speech data, and the CMX6x8 Disable bit in the Modem Configuration - $C7 write register.

6.6.4 Modem Control

The CMX7131/CMX7141 operates in one of these operational modes:

- IDLE
- Rx
- Tx
- CMX6x8/CMX994 Pass-through
- Rx with CMX994 I/Q Cal.
- Rx with Powersave.

At power-on or following a reset the device will automatically enter IDLE mode, which allows maximum powersaving whilst still allowing the AuxADC inputs to be monitored (if enabled). It is only possible to write to the Programming register whilst in IDLE mode.

See:

- Modem Control - $C1 write.

RXENA and TXENA pins (GPIO1 and GPIO2) reflect bits 0 and 1 of the Modem Control register, as shown in Table 13. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 13 Modem Mode Selection

Modem Control ($C1) b3-0	Modem Mode	GPIO2 - TxENA	GPIO1 - RxENA
0000	IDLE – low power mode	1	1
0001	Rx mode	1	0
0010	Tx mode	0	1
0011	*reserved*	x	x
0100	CMX6x8/CMX994 Pass-through	1	1
0101	Rx with CMX994 I/Q cal (I/Q mode only)	1	0
1001	Rx with Powersave (I/Q mode only)	1	0
others	*reserved*	x	x

The CMX6x8/CMX994 Pass-through mode is used to control and monitor the CMX6x8 or CMX994 directly. This cannot be accessed if the CMX7131/CMX7141 is in Rx or Tx modes. This mode will transfer data to/from the TxData0/RxData0 register to the CMX6x8 C-BUS register address specified in the Programming register ($C8). See section 8.1.28. The Modem Control bits are ignored in this mode.

Table 14 Modem Control Selection

4FSK Modem Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx T102 Formatted	Tx T102 Formatted
0010	Rx T102 Raw	*reserved*
0011	Rx 4FSK EYE	Tx 4FSK PRBS
0100	Rx Pass-through Mode	Tx 4FSK Preamble
0101	*reserved*	Tx 4FSK Mod setup
0110	Sync	Tx 4FSK Repeated Word
0111	Reset/abort	Reset/abort
others	*reserved*	*reserved*

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

6.6.5 Tx Mode T102 Formatted

In Tx mode, the CMX7131/CMX7141 operates in T102 formatted mode. In both cases the first block of control channel or payload data should be loaded into the C-BUS TxData registers before executing the mode change. A “DataReady” IRQ will be asserted when the registers have been read by the CMX7131/CMX7141 and the host can then supply further blocks of payload data. When all payload has been transmitted the CMX7131/CMX7141 will issue a “TxDone” IRQ and the host can then reset the Mode bits to either Rx or IDLE as required.

6.6.6 Tx Mode

In Tx mode operation ($C1, Modem Control = $0012), the Preamble sequence is automatically transmitted first, unless disabled by setting $C7:b11. The SW sequence is then automatically transmitted for each frame, followed by control channel and payload data from the TxData registers or CMX6x8 Vocoder. This continues until a data underflow condition occurs, the “End” frame is detected or the Mode is changed back to Rx or IDLE. RICH/SACCH blocks for the first frame should be loaded into the TxData registers before executing the Modem Mode change to Tx. The CMX7131/CMX7141 performs all necessary scrambling, interleaving and FEC coding functions for the control channel and payload fields. In speech calls the CMX7131/CMX7141 will automatically enable the CMX6x8 Vocoder when required and transfer the received TCH speech data blocks from it without host intervention.

As soon as each control channel or payload data block has been read from the C-BUS TxData registers, the “DataReady” IRQ will be asserted and the next block of data may then be loaded. Note that payload data is always transmitted msb (most significant bit) first.

At the end of the call, the host should load control channel fields for the final frame with the SACCH “Message Classification” field set to “Idle”, and the FACCH1 “Message Classification” field set to “Clearing”. The CMX7131/CMX7141 will issue a “TxDone” IRQ when the frame has been sent and the host can then safely place the device into IDLE mode ($C1, Modem Control = $0000).

A typical host Tx sequence is:

1. Load TxData registers with RICH (7 bits) and SACCH (26 bits) for “Idle”
2. Set Modem Control = TxFormat, Modem Mode = Tx

   (Device will start transmission of Preamble and SW followed by contents of TxData registers)
3. Wait for DataReady IRQ
4. Load TxData registers with first part of FACCH1 (40 bits)
5. Wait for DataReady IRQ
6. Load TxData registers with second part of FACCH1 (40 bits)
7. Wait for DataReady IRQ
8. Load TxData registers with first part of FACCH1 (40 bits)
9. Wait for DataReady IRQ
10. Load TxData registers with second part of FACCH1 (40 bits)
11. Wait for DataReady IRQ
12. Load TxData registers with RICH (7 bits) and SACCH (26 bits) for “Audio”
13. Wait for DataReady IRQ
14. Load TxData registers with TCH data (72 bits)
15. Wait for DataReady IRQ
16. Load TxData registers with TCH data (72 bits)
17. Wait for DataReady IRQ
18. Load TxData registers with TCH data (72 bits)
19. Wait for DataReady IRQ
20. Load TxData registers with TCH data (72 bits)
21. Wait for DataReady IRQ
22. …repeat from 12 with the SACCH data set appropriately
23. Load TxData registers with RICH (7 bits) and SACCH (26 bits) for “Clearing”

24. Wait for DataReady IRQ
25. Load TxData registers with FACCH1 data (40 bits)
26. Wait for DataReady IRQ
27. Load TxData registers with FACCH1 data (40 bits)
28. Wait for DataReady IRQ.
29. Load TxData registers with FACCH1 data (40 bits)
30. Wait for DataReady IRQ
31. Load TxData registers with FACCH1 data (40 bits)
32. Wait for DataReady IRQ.

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

A typical host Tx sequence for Data Communications is:

1. Load TxData registers with RICH (7 bits) for “10 01 11 0”
2. Set Modem Control = TxFormat, Modem Mode = Tx
3. (Device will start transmission of Preamble and SW followed by contents of TxData registers)
4. Wait for DataReady IRQ
5. Load TxData registers with first part of UDCH1 (72 bits) – this includes the SU field
6. Wait for DataReady IRQ
7. Load TxData registers with second part of UDCH1 (72 bits)
8. Wait for DataReady IRQ
9. Load TxData registers with third part of UDCH1 (40 bits)
10. Wait for DataReady IRQ
11. Load TxData registers with RICH (7 bits) for “10 01 11 0”
12. …repeat from 4
13. Load TxData registers with RICH (7 bits) for “10 01 01 0”
14. Wait for DataReady IRQ
15. Load TxData registers with FACCH2 data (72 bits)
16. Wait for DataReady IRQ
17. Load TxData registers with FACCH2 data (72 bits)
18. Wait for DataReady IRQ.
19. Load TxData registers with FACCH2 data (40 bits)
20. Wait for DataReady IRQ

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

A typical host Tx sequence for Data Burst is:

1. Load TxData registers with RICH (7 bits) for “10 11 11 0”

2. Set Modem Control = TxFormat, Modem Mode = Tx
3. (Device will start transmission of Preamble and SW followed by contents of TxData registers)
4. Wait for DataReady IRQ
5. Load TxData registers with first part of UDCH2 (72 bits) – this includes the SU field
6. Wait for DataReady IRQ
7. Load TxData registers with second part of UDCH2 (72 bits)
8. Wait for DataReady IRQ
9. Load TxData registers with third part of UDCH1 (72 bits)
10. Wait for DataReady IRQ
11. Load TxData registers with fourth part of UDCH2 data (36 bits + 4 bits padding)
12. Wait for DataReady IRQ

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

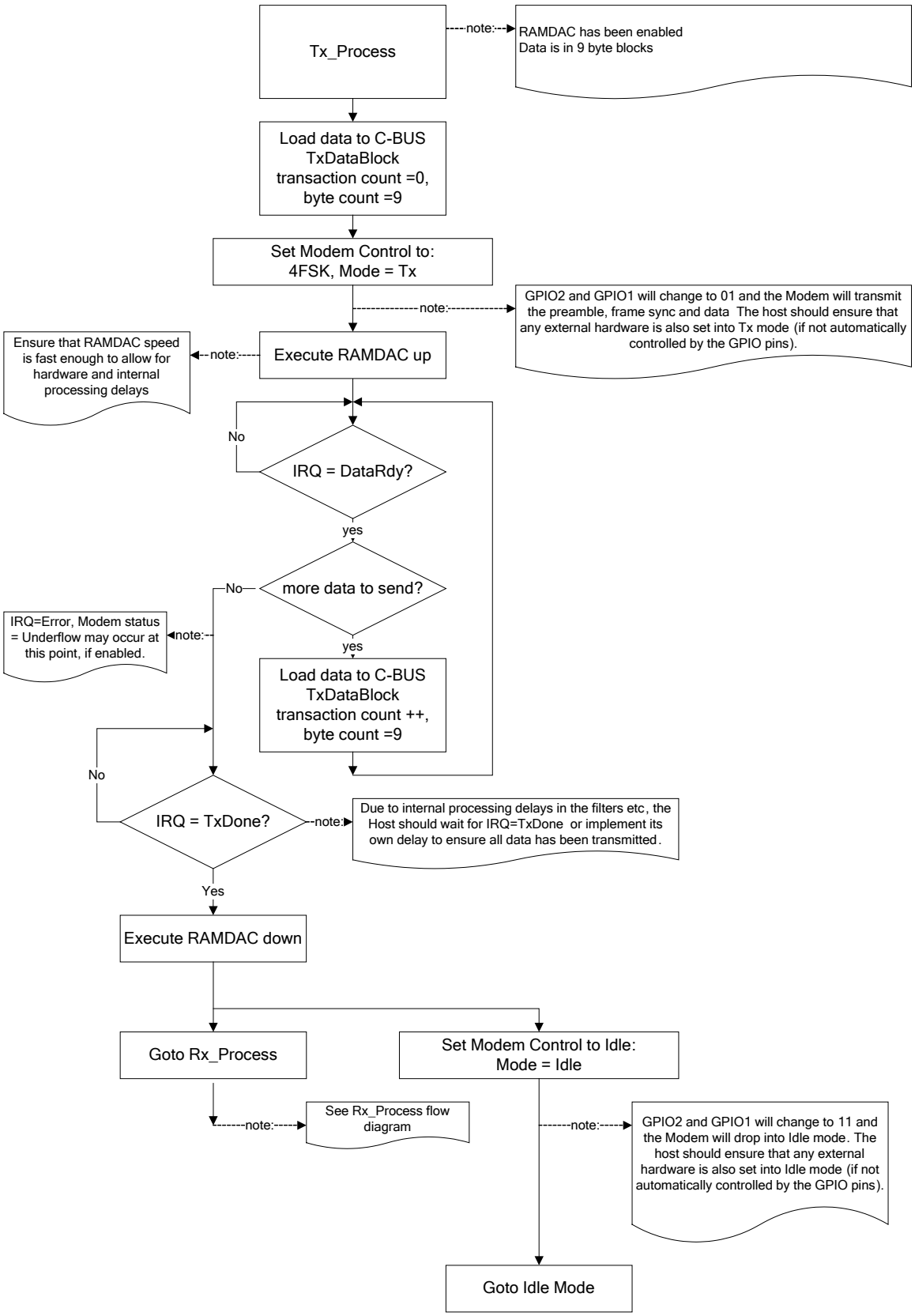


Figure 22 Tx Data Flow

6.6.7 Tx Mode PRBS

In PRBS mode ($C1, Modem Control = $0032) the preamble and frame sync are transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para. 2.1) giving a 511-bit repeating sequence.

6.6.8 Tx Mode Preamble

In Preamble mode ($C1, Modem Control = $0042) the preamble sequence [+3 +3 -3 -3] is sent continually. This can be used to set up and adjust the RF hardware.

6.6.9 Tx Mode Mod Set-up

In Mod Set-up mode ($C1 = $0052) the output depends on the selected Tx modulation type. In two-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols is sent, and in I/Q mode a continuous sequence of +3 symbols is sent. This can be used to set up and adjust the RF hardware.

6.6.10 Tx Mode Repeated Word

In Repeated Word mode ($C1 = $0062) the output depends on the data loaded into the TxData04 register ($CB). This can be used to set up and adjust the RF hardware.

6.6.11 Tx Sequencer

If enabled, the Tx Sequencer will automatically start executing its sequence of transmit actions when the CMX7131/CMX7141 is placed in Tx mode. The timing values for each action can be set in P3.75 to P3.80 and are defined in increments of 250µs.

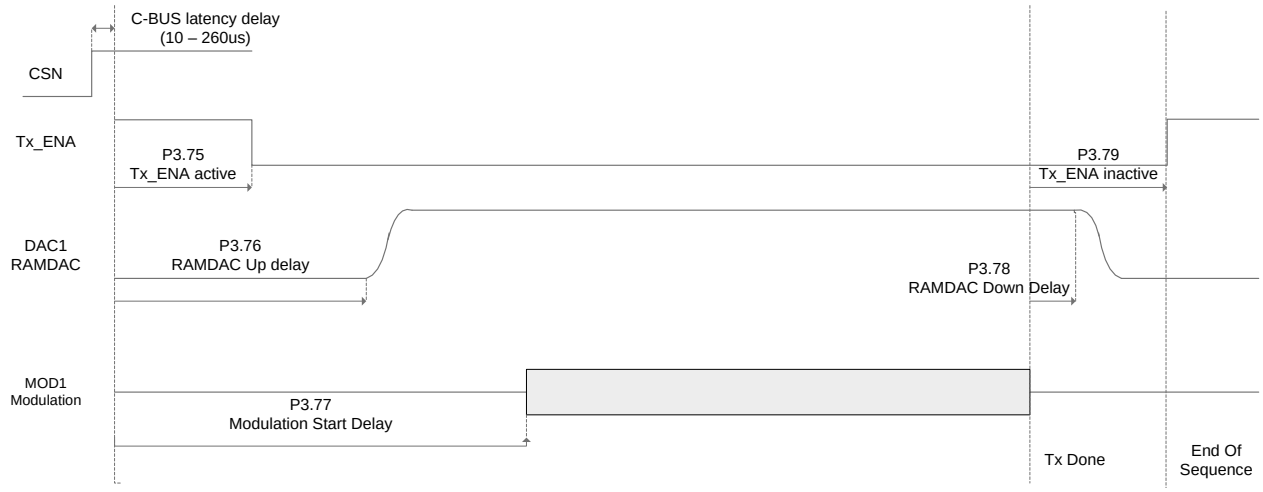


Figure 23 Automatic Tx Sequencer

6.6.12 Rx Mode T102 Formatted

In Rx mode the received signal should be routed through Input1. In T102 Raw and Formatted modes the CMX7131/CMX7141 will first search for frame synchronisation, and when this has been achieved the following data is demodulated and supplied to the host through the RxData registers. A “DataReady” IRQ indicates when each new block becomes available. In T102 Raw mode the CMX7131/CMX7141 will continue demodulating the input signal until the host resets the Mode bits to Tx or IDLE, but in T102 Formatted mode the modem can detect the end of a call and restart framesync search automatically.

6.6.13 Rx Mode Raw

Rx Mode Raw is included in this FI to facilitate BER measurements in I/Q mode. In this mode ($C1, Modem Control = $0021), once a valid Frame Sync has been detected, all following data received is loaded directly into the C-BUS RxData registers. This continues until the end of the burst (even if there is no valid signal at the input). On exiting Rx Mode Raw, there may be a DataRdy IRQ pending which should be cleared by the host. Note that Raw Mode operation always requires the incoming data to be preceded with a valid Preamble and Frame Sync pattern in order to derive timing information for the demodulator. The device will update the C-BUS RxData registers with Rx payload data as it becomes available. The host MUST respond to the DataRDY IRQ before the RxData registers are over-written by subsequent data from the modem.

6.6.14 Rx Mode Eye

In Rx 4FSK EYE mode ($C1 = $0031), the filtered received signal is output at the MOD1 pin as an ‘eye’ diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal. In I/Q mode, this includes I/Q dc calculation in RXDATA0, RXDATA1 and computed Powersave Levels 1,2,3 in RXDATA2-4.

6.6.15 Rx Pass-through Mode

Rx Pass-through mode ($C1 = $0041) is very similar to Rx Mode Eye as described in section 6.6.14. However the output at the MOD1 pin is the flat, unfiltered signal. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

Table 15 Frequency Response for Rx Pass-through Mode

300Hz	-0.6dB
1kHz	0dB (reference)
2kHz	-0.7dB
2.5kHz	-1.4dB
3kHz	-2.4dB
4kHz	-4.9dB
6kHz	-12.2dB

6.6.16 Rx Mode with CMX994 AGC (I/Q Mode only)

By default, when receiving in I/Q Mode the CMX7131/CMX7141 will control its internal analogue gain and the gain of the CMX994 in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P2.0 (I/Q AGC function), in which case any setup that the host has made of the CMX994 will determine its gain, with the input gain of the CMX7131/CMX7141 being controlled using the Input Gain and Signal Routing - $B1 write register.

It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994 as described in section 6.6.17.

6.6.17 Rx Mode with CMX994 I/Q Cal (I/Q Mode only)

When receiving, the CMX7131/CMX7141 will estimate and remove the dc error present in the I/Q signals from a CMX994 receiver. However, it is necessary to calibrate the CMX994 so that the magnitude of the

dc offsets present is as small as possible. Selecting Rx mode with CMX994 I/Q Cal ($C1, Modem Control b3-0 = $5) causes the CMX7131/CMX7141 to measure the dc offset on the DISC and ALT input pins and to control the CMX994 receiver to minimise the dc offsets. The CMX7131/CMX7141 will then begin to receive normally – correcting the remaining dc offset internally.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994 is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Having calibrated the CMX994, the value written to the CMX994 dc offset correction register is available to read using the Aux Data and Status ($A9, $AA) registers so that having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time.

6.6.18 Rx Mode with Powersave (I/Q Mode only)

Selecting powersave mode ($C1, Modem Control b3-0 = $9) will cause the CMX7131/CMX7141 to control the CMX994, switching it into a low-power state for a short period of time. Once the powersave timer has expired then the CMX994 and the internal circuits of the CMX7131/CMX7141 will be powered-up, ready to receive.

On entering the powered-up state, the CMX7131/CMX7141 will monitor the received I/Q signals for energy in its sampled bandwidth and if there is no signal present it will return to the powersave state, powering down the CMX994. If sampled energy is found then the signal is passed through a channel filter and the resulting signal measured. If no signal is found the powersave state is selected once more. Finally, a squelch measurement is taken, by FM demodulating the received signal and measuring the energy above the expected signal bandwidth. If squelch indicates that the signal is a good FM modulated signal powersave mode is ended, leaving the CMX994 and CMX7131/CMX7141 on and in receive, until the mode register is written to.

Throughout the time that the receiver is on, the CMX7131/CMX7141 will search for a frame sync and start receiving the data following that frame sync, if found. However, dependent on the powersave period, it is possible that the frame sync at the start of a burst may be missed, in which case ‘late entry’ is possible.

Thresholds for comparison and timings for powersave mode may be adjusted, potentially improving powersaving by being powered down for a greater period of time, but at the expense of a slower reaction to a received signal. See the Aux Config - $CD write register.

6.6.19 Reset/Abort

From each Rx or Tx mode, a Reset/Abort aborts the current state machine and drops into the corresponding (Rx or Tx) Idle mode. The only difference between this and going directly into the corresponding Idle mode is that all of the buffers and filters are flushed out first with Reset/Abort.

6.6.20 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred. If a data transfer does not consist of an integer number of bytes, then the final byte transfer should be padded with zero’s up to the byte boundary (as is the case with UDCH2, which uses 252 bits).

Table 16 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 and info	$B8	Rx data 0-7 and info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

The Block ID is ignored in Raw Data mode, but should be set to 01 (payload) for consistency with T102 formatted mode (see User Manual section 8.1.17).

Bits 7 and 6 hold the Transaction Counter, which is incremented modulo 4 on every read/write of the Data Block to allow detection of data underflow and overflow conditions. In Tx mode the host must increment the counter on every write to the TxData block, and if the CMX7131/CMX7141 identifies that a block has been written out of sequence, the Event bit (C-BUS register $C6, b14) will be asserted and an IRQ raised, if enabled. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (i.e. it should be the last register the host writes to in any block transfer). In Rx mode, the CMX7131/CMX7141 will automatically increment the counter every time it writes to the RxData block. If the host identifies that a block has been written out of sequence, then it is likely that a data overrun condition has occurred and some data has been lost. If a CRC failure has been detected when decoding the data block, an 'Event' IRQ is issued concurrently with the 'Data Ready' IRQ along with a status code in the Modem Status register ($C9).

6.6.21 CMX6x8/CMX994 Pass-through Mode

To allow the host to communicate directly with the CMX6x8 or CMX994 for test and configuration purposes, a pass-through mode is available which allows any CMX994 C-BUS register to be written or any CMX6x8 C-BUS register to be read or written (as appropriate). This mode uses the TxData0, RxData0 and Programming registers on the CMX7131/CMX7141.

To write to the CMX6x8:

- Set the CMX7131/CMX7141 to CMX6x8/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8 data value to the TxData0 register ($B5)
- Write the CMX6x8 C-BUS address to the Programming register ($C8) with b15-13=$010_2$
- Wait for the Program Flag to be set ($C6 b0).

To read from the CMX6x8:

- Set the CMX7131/CMX7141 to CMX6x8/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8 C-BUS address to the Programming register ($C8) with b15-13=$110_2$
- Wait for the Program Flag to be set ($C6 b0)
- Read the CMX6x8 data value from the RxData0 register ($B8).

CMX6x8 C-BUS addresses are all 8 bits long and should be written to bits 0-7 of the Programming Register. Bit 15 is the read/write flag (0 = read, 1 = write) and bit 14 is the register-size flag (0 = 16-bit, 1 = 8-bit). Unused bits should be cleared to zero. When an 8-bit register is read or written, the data occupies the lower 8 bits of the appropriate data register (TxData0 or RxData0).

To write to the CMX994:

- Set the CMX7131/CMX7141 to CMX6x8/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994 data value to the TxData0 register ($B5)
- Write the CMX994 C-BUS address to the Programming register ($C8) with b15-13=$011_2$
- Wait for the Program Flag to be set ($C6 b0).

6.7 T102 Mode Operation

The CMX7131/CMX7141 performs all frame building/splitting and FEC coding/decoding, which relieves the host controller of a significant processing load. During voice calls the CMX7131/CMX7141 can automatically enable and control the CMX6x8, and transfer voice payload data from/to it, without host intervention. In Rx mode the CMX7131/CMX7141 monitors the incoming control channel fields and will only accept calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or “sleep” state until it is really necessary to wake up, enhancing the battery life of the final product design.

6.7.1 Frame Format

T102 calls contain an optional preamble sequence (controlled by $C7:b11) followed by a continuous stream of 384-bit (80ms) frames. Three frame formats are defined by the standard: “Audio Communications Format”, “Data Communications Format” and “Data Communications Burst Format”.

All frames start with a 20-bit Sync Word followed by a 16-bit Radio Information Channel (RICH) block. The RICH fields indicate the frame format and payload type, and the CMX7131/CMX7141 uses this information to determine how to process each frame in both Tx and Rx. The “Communications mode identification” field sets the frame format and the “Option” field sets the payload field type (TCH, FACCH1, FACCH2, UDCH1, UDCH2).

In an “Audio Communications Format” call the 60-bit Slow Associated Control Channel (SACCH) block is present in all frames. The “Start” and “End” frames carry two 144-bit “Fast Associated Control Channel 1” (FACCH1) blocks in the payload fields instead of Traffic Channel (TCH) data. The CMX7131/CMX7141 scans the “SU” and “Message Classification” fields contained in the SACCH and FACCH1 blocks and uses these to perform address matching (in Rx mode) and to decide whether to route the following TCH data via the host or directly to/from the CMX6x8 Vocoder, or to enable audio sample routing when in SPI-CODEC mode. The CMX7131/CMX7141 also checks the “Message Classification” field for the “Clearing” value which indicates an “End” frame. When this is found the CMX7131/CMX7141 terminates call processing and disables the CMX6x8 Vocoder (if necessary).

During a call, while TCH data is being routed directly to/from the CMX6x8, the RICH and SACCH fields continue to be transferred to/from the host using the C-BUS data transfer registers in the usual way.

Note that in an “Audio Communications Format” call the TCH bearing frames are grouped into superframes, in which the information contained in SACCH may be split across four consecutive frames. Dis-assembly and re-assembly of the contents must be done by the transmitting and receiving hosts; this function is not performed by the CMX7131/CMX7141.

Note that all block sizes given above refer to “over-air” bits, some of which are FEC coded. Because the CMX7131/CMX7141 performs all FEC coding functions, the block sizes of data transfers between the CMX7131/CMX7141 and host are smaller in most cases except for uncoded TCH blocks.

Table 17 RxData 0/TxData 0 Block ID settings

RxData 0 TxData 0 b5-4	Block ID
00	*reserved*
01	Payload Data
10	RICH
11	SACCH and RICH

RICH Data:
The TxData block is interpreted in the following manner:

TxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RICH0-6							Count		1	0	0	0	0	1
1	Not used															
2	Not used															
3	Not used															
4	Not used															

	6	5	4	3	2	1	0
RICH	F		M		O		D

F	Format
00	*reserved*
01	*reserved*
10	**Direct Communication**
11	*reserved*

D	Direction
0	**Uplink or MS - MS**
1	Downlink

M	O	Mode	Payload content
00	**00**	Audio Communication, non-superframe SACCH follows	**FACCH1 / FACCH1**
00	01		*reserved*
00	10		*reserved*
00	11		*reserved*
01	**00**	Data Communication	**FACCH2**
01	01		*reserved*
01	10		*reserved*
01	**11**		**UDCH1**
10	00	Audio Communication, superframe SACCH follows	FACCH1 / FACCH1
10	01		FACCH1 / TCH
10	10		TCH / FACCH1
10	**11**		**TCH / TCH**
11	00	Data Burst	*reserved*
11	01		*reserved*
11	10		*reserved*
11	**11**		**UDCH2**

Examples:

Start frame:	10 00 00 0	Audio with FACCH1 (single frame)
TCH frame:	10 10 11 0	Audio with TCH payload (super-frame)
Clearing frame:	10 00 00 0	Audio with FACCH1 (single frame)

RICH and SACCH Data:
The TxData/RxData block is interpreted in the following manner:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RICH 0-6							Count		1	1	0	1	0	1
1	SACCH 0-7								SACCH 8-15							
2	SACCH 16-23								0	0	0	0	0	0	SACCH 24-25	
3	Not used															
4	Not used															

TCH Payload Data:
See Table 17 and User Manual section 8.1.14.

6.7.2 Addressing

The T102 standard allows individual or group addressing systems to be implemented using the 6-bit “User Code” field in the SACCH block. The host can load six user codes into Program Block 1 as “Own-IDs” and the CMX7131/CMX7141 will only accept an incoming call if one of these is matched or if the “All-Call” User Code (all-zeros) is received. The CMX7131/CMX7141 can also be programmed to accept or reject calls depending on the value of the SACCH “Message Classification” field, using the Manufacturer ID in Program Block 1.

6.7.3 Rx Mode

In Rx mode ($C1, Modem Control = $0011), the CMX7131/CMX7141 automatically starts searching for frame synchronisation. When a valid framesync sequence is detected, an “FS1 Detect” or “FS2 Detect” IRQ is asserted and the data demodulator is enabled. The CMX7131/CMX7141 then processes the first frame to extract control channel data and decide whether to accept the call. The CMX7131/CMX7141 performs all the necessary de-scrambling, de-interleaving and FEC decoding functions for control channel and payload data blocks. If the RICH or SACCH control channel blocks in the first frame fail their CRC or parity-bit checks, the CMX7131/CMX7141 will continue scanning incoming frames until valid control channel information is received.

The SACCH/FACCH1 “User Code” in the “SU” field is then checked and accepted if either (a) it is the all-zeros “All-Call” User Code, or (b) it matches one of the device’s “Own-IDs” programmed by the host into Program Block P1.0 to P1.5. If this check fails, and the “Open Rx” bit is clear, the call is rejected and the CMX7131/CMX7141 restarts framesync search automatically without host intervention.

Otherwise, the call is accepted, a “Called” IRQ is issued to the host and the User Code and ID match-type (exact match or All-Call) are reported in the AuxData register ($CC), and the CMX7131/CMX7141 then begins transferring data blocks to the host and enables the CMX6x8 if necessary.

Control channel fields and payload data blocks are transferred via the RxData registers. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The host MUST respond to each “DataReady” IRQ before the RxData registers are overwritten by subsequent data blocks. If “soft” data mode has been selected, uncoded payload data is transferred in 4-bit log-likelihood-ratio (LLR) format and in this mode the host must be able to service the “DataReady” IRQs and RxData registers at four times the normal rate to avoid loss of data.

When a CRC or parity-bit failure has been detected in a control channel or payload data block, an additional “Event” IRQ is issued to the host at the same time as the “DataReady” IRQ, with a corresponding error code in the Modem Status register, $C9.

In speech calls the CMX7131/CMX7141 will automatically enable the CMX6x8 Vocoder when required and transfer all received TCH speech data blocks to it without host intervention. Speech data routed to the CMX6x8 always uses 4-bit LLR format. Control channel fields are always transferred to the host regardless of speech data routing.

Received frames are processed continually until an “End” frame is detected, the Call Drop Threshold is exceeded (P0.0) or the Mode is changed back to IDLE. The CMX7131/CMX7141 will then automatically disable the CMX6x8, transfer the contents of the final frame to the host, and restart framesync search automatically unless switched to IDLE.

See:

- RxData 0 - $B8 read
- RxAuxData - $CC read.

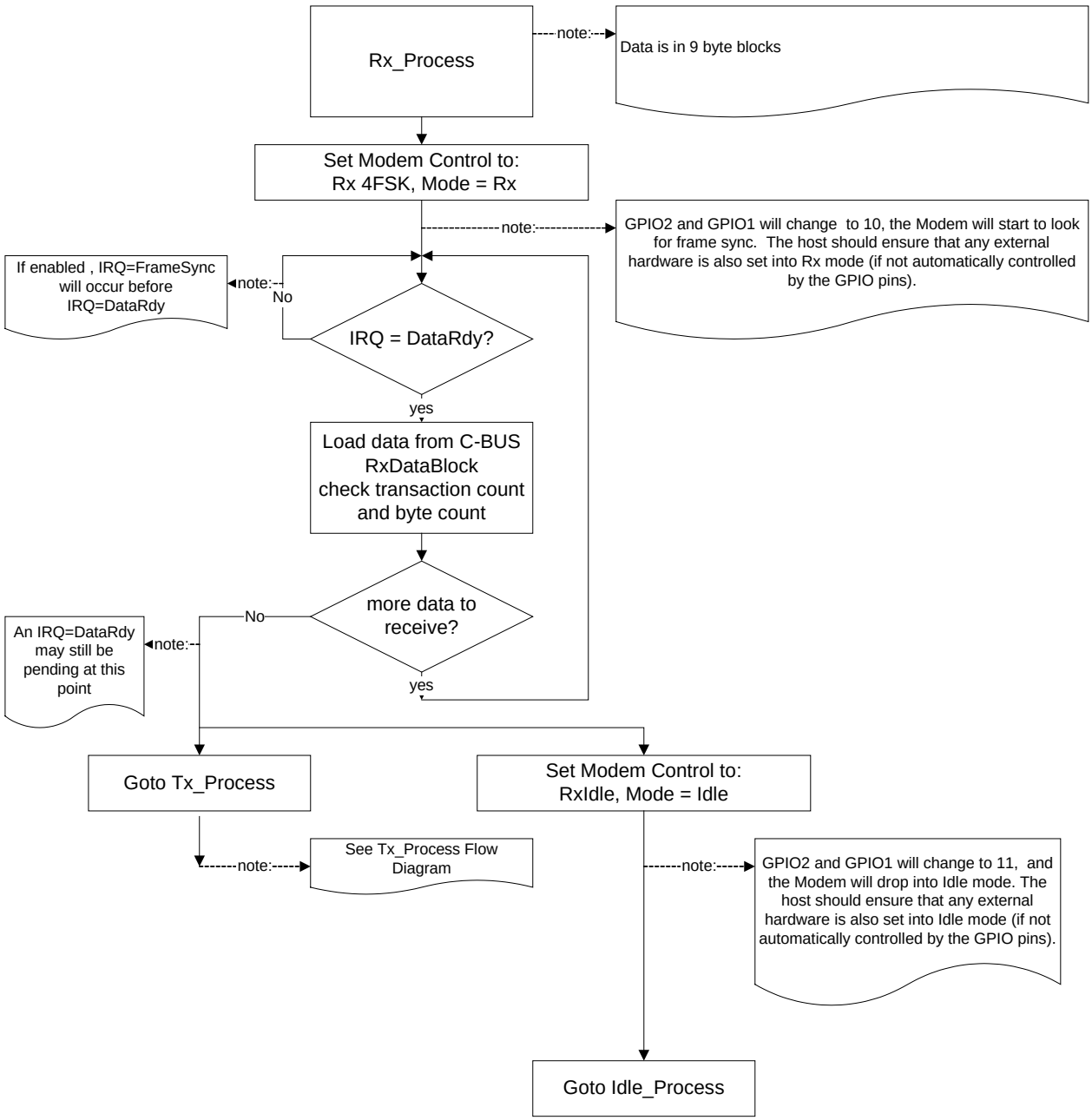


Figure 24 Rx Data Flow

6.8 Squelch Operation

Many limiter/discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital Squelch signal, which can be routed directly to one of the CMX7131/CMX7141's GPIO pins or to the host. However with the CMX7131/CMX7141, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.

See:

- Status - $C6 read
- AuxADC Configuration - $A7 write.

Note: This functionality is not necessary in I/Q mode as squelch detection is within CMX7131/CMX7141 signal processing however the AuxADC functionality remains available.

6.9 GPIO Pin Operation

The CMX7131/CMX7141 provides four GPIO pins: GPIO1, GPIO2, GPIOA and GPIOB. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:

- Modem Control - $C1 write

Note that RxENA and TxENA will not change state until the relevant Mode change has been executed by the CMX7131/CMX7141. This is to allow the host sufficient time to load the relevant data buffers and the CMX7131/CMX7141 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins.

During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is input, with a weak pullup resistor. When set for input, the values can be read back using the Modem Status register, $C9.

6.10 Auxiliary ADC Operation

The inputs to the two AuxADCs can be independently routed from any of the signal input pins under control of the Signal Routing register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to "off". Register $C0, b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the AuxADC readings by selecting the relevant bits in the AuxADC configuration register, $A7, the length of the averaging is determined by the value in the Program Block (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value

1 = 25% of the current value will be added to 75% of the last average value

2 = 12.5% etc.

The maximum useful value of this field is 9.

High and low thresholds may be independently applied to both AuxADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 25. The thresholds are programmed via the Aux Config register, $CD. See Figure 25.

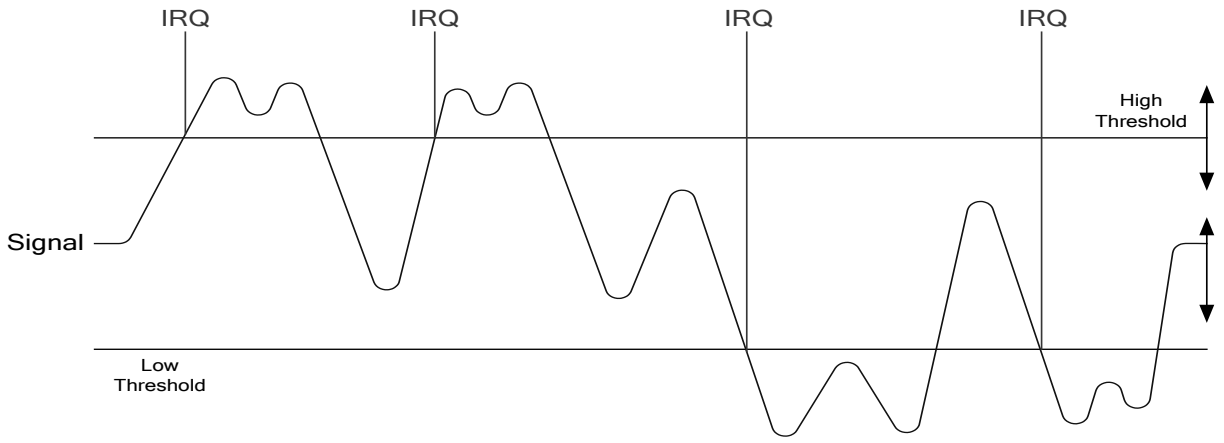


Figure 25 AuxADC IRQ Operation

AuxADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:
- o AuxADC Configuration - $A7 write
- o AuxADC1 Data and Threshold Status- $A9 read
- o AuxADC2 Data and Threshold Status- $AA read
- o Aux Config - $CD write.

6.11 Auxiliary DAC/RAMDAC Operation

The four AuxDAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 22), but this may be over-written with a user-defined profile by writing to Program Block P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

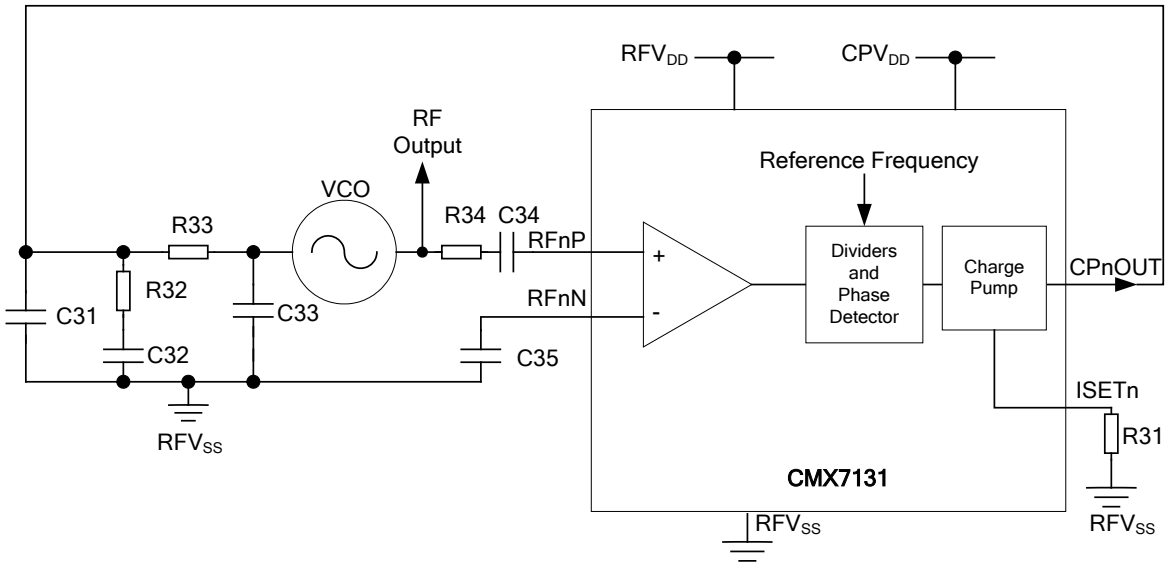
See:
- o AuxDAC Data/Control - $A8 write.

6.12 RF Synthesiser (CMX7131 only)

The CMX7131 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- o RF Synthesiser Data (CMX7131 only) - $B2 write
- o RF Synthesiser Control (CMX7131 only) - $B3 write
- o RF Synthesiser Status (CMX7131 only) - $B4 8-bit read.

External RF components are needed to complete the synthesiser circuit. A typical schematic for a 446MHz synthesiser (3.125kHz comparison frequency) is shown in Figure 26.



Note: n = 1 or 2 for Synthesiser 1 or 2

Figure 26 Example RF Synthesiser Components

R31	0Ω	C31	22nF
R32	5.6kΩ	C32	470nF
R33	10kΩ	C33	10nF
R34	100Ω	C34	1nF
		C35	1nF

Notes: Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7131 is kept as short as possible. The loop filter components should be placed close to the VCO.

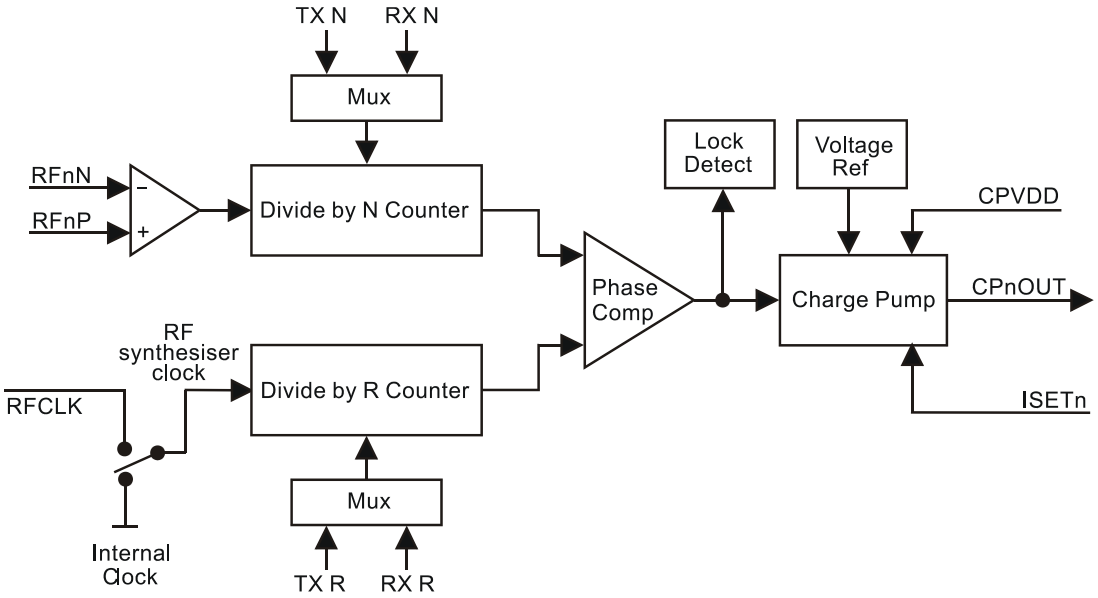


Figure 27 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 27 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL/CLK input or the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both channels. The charge pump supply pin CPVDD and the RF synthesiser power supply pins RFVSS and RFVDD are also common to both channels. The remaining pins are designated with a 1 or 2 to indicate to which RF synthesiser block they belong. The N and R values for Tx and Rx modes are channel specific and can be set from the host µC via the C-BUS. Various channel specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 26.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFV_{SS}. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

Gain bit set to 1: R31 (in Ω) = (24/Icp) – 9600.
Gain bit cleared to 0: R31 (in Ω) = (6/Icp) – 9600.
Where Icp is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The ‘gain bit’ refers to either bit 3 or bit 11 in the RF Channel Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency.

Other parameters for the synthesisers are the charge pump setting (high or low).

Since the set-up for the PLLs takes 4 x "RF Channel Data register" writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the "RF Channel Data register" on a PLL that is disabled, powersaved or selected to work from the alternate register set ("Tx" and "Rx" are alternate register sets). There are no interlocks to enforce this intention. The names "Tx" and "Rx" are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control (CMX7131 only) - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (RFClock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Channel Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a 4-cycle tolerance is for the case where a high frequency reference oscillator would not tolerate a small phase error.

RF Inputs

The RF inputs are differential and self-biased (when not powersaved). They are intended to be capacitively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the "N" and "P" inputs capacitively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitive and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14 V/µs minimum
- The RF synthesiser 2.5V digital supply can be powered from the VDEC output pin
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating
- It is recommended that the RF synthesisers are operated with maximum gain (ie. ISET1/2 tied to RFV_{SS})
- The loop filter components should be optimised for each VCO.

6.13 Digital System Clock Generators

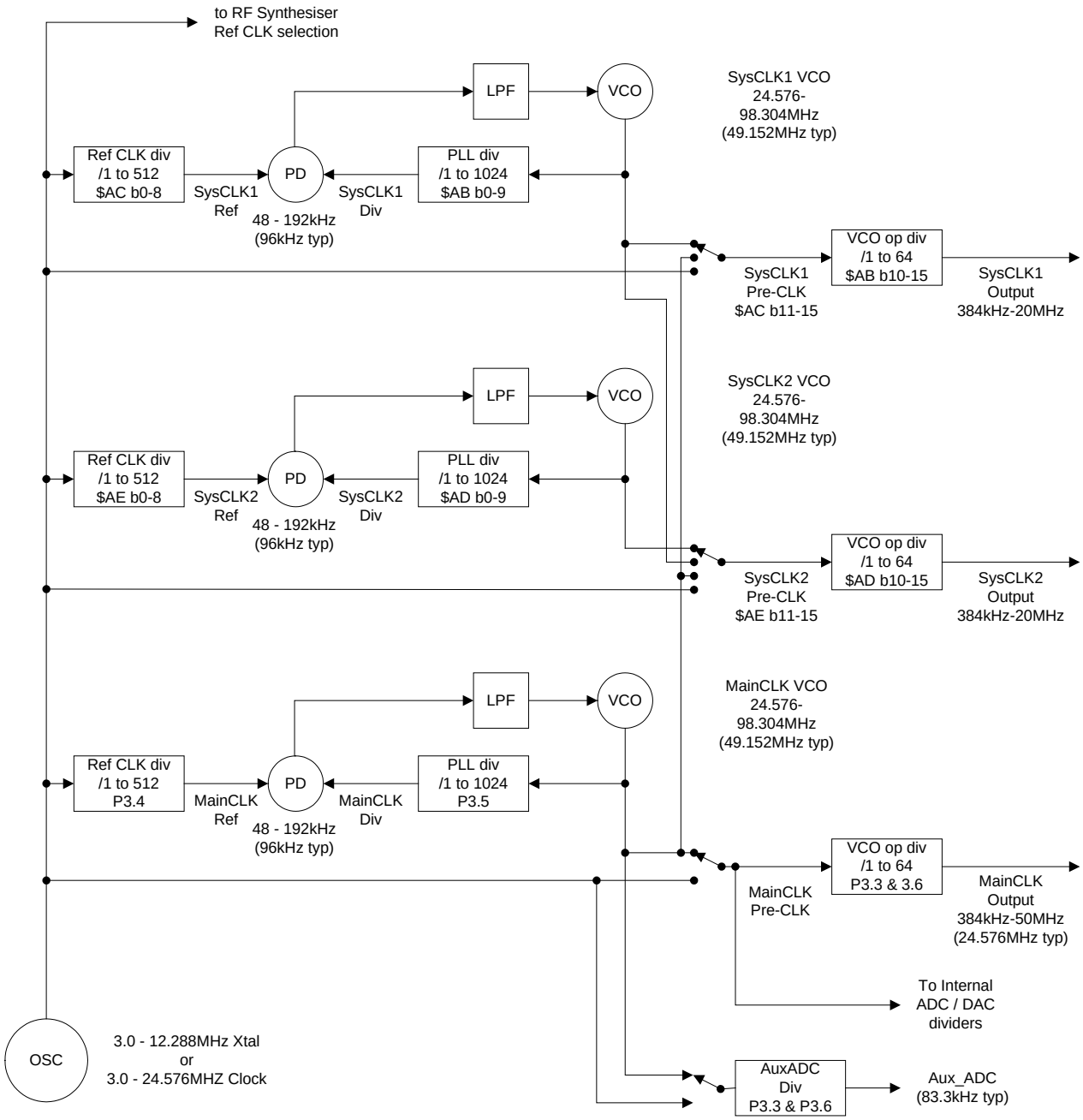


Figure 28 Digital Clock Generation Schemes

The CMX7131/CMX7141 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Section 4.2, or the XTAL/CLK input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7131/CMX7141.

6.13.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7131/CMX7141. At the same time, other internal clocks are generated by division of either the XTAL or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer and the signal processing block. In particular, it should be noted that in IDLE mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7131/CMX7141 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block P3.2 to P3.6 will need to be programmed appropriately at power-on. This flexibility allows the device to share an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 9.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control.

6.13.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a nominal reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 28. Note that at power-on, these pins are disabled.

See:

- SYSCLK1 and SYSCLK2 PLL Data - $AB, $AD write
- SYSCLK1 and SYSCLK2 REF - $AC and $AE write.

6.14 Signal Level Optimisation

The internal signal processing of the CMX7131/CMX7141 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts p-p = 838mV rms, assuming a sine-wave signal. This should not be exceeded at any stage.

6.14.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB. The Fine Output adjustment ($C3) has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to 12.0dB and no gain.

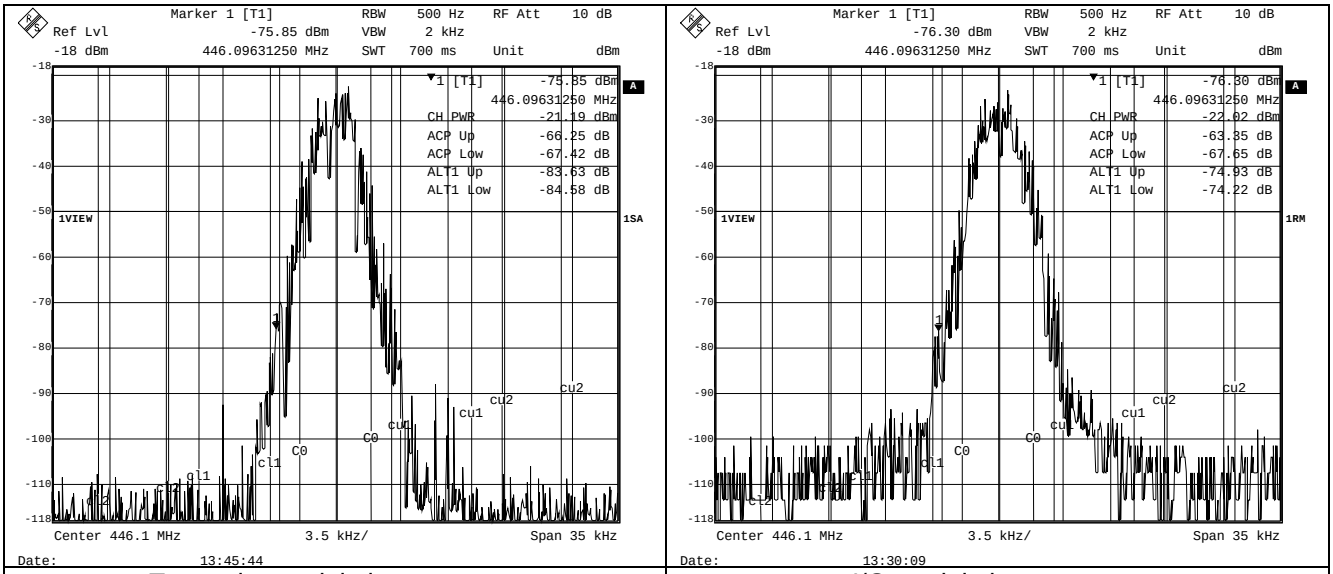
6.14.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4dB and no attenuation. In LD mode, with the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mVrms. This signal level is an absolute maximum, which should not be exceeded.

In I/Q mode CMX7131/CMX7141 automatically manages the gain control settings to optimise signal levels.

6.15 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX7131/CMX7141 internal PRBS generator. Note that the I/Q mode is sensitive to variations in dc offset in the modulation path and these must be minimised.



Two-point modulation spectrum	I/Q modulation spectrum

Figure 29 Tx Modulation Spectra - 4800bps

6.16 C-BUS Register Summary

Table 18 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data/Control	16
$A9	R	AuxADC1 Data and Threshold Status/Checksum 2 hi	16
$AA	R	AuxADC2 Data and Threshold Status/Checksum 2 lo	16
$AB	W	System Clk 1 PLL Data	16
$AC	W	System Clk 1 REF	16
$AD	W	System Clk 2 PLL Data	16
$AE	W	System Clk 2 REF	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power-Down Control	16
$C1	W	Modem Control	16
$C2	W	TxAuxData	16
$C3	W	CMX6x8 Analogue Gain	16
$C4		*reserved*	
$C5	R	Rx Data 4	16
$C6	R	Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	RxAuxData	16
$CD	W	Aux Config	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD} - DV_{SS}	–0.3	4.5	V
AV_{DD} - AV_{SS}	–0.3	4.5	V
RFV_{DD} - RFV_{SS} (CMX7131 only)	–0.3	4.5	V
CPV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS, CPVDD, RFVDD or RFVSS	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD} (CMX7131 only)	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS} (CMX7131)	0	50	mV
AV_{SS} and RFV_{SS} (CMX7131 only)	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$ (CMX7131 only)		3.0	3.6	V
$RFV_{DD} – DV_{SS}$ (CMX7131 only)	3	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using a Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes:
1 Nominal XTAL/CLK frequency is 19.2MHz.
2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.
3 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2
Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} (CMX7131) = 3.0V to 3.6V; RFV_{DD} (CMX7131) = 2.25V to 2.75V.
V_{DEC} = 2.5V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with 7131/7141FI-6.x only. The use of other Function Images, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
IDLE Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode	22				
DI_{DD} (4800bps – search for FS)		–	4.7	–	mA
DI_{DD} (4800bps – FS found)		–	2.8	–	mA
AI_{DD}		–	1.6	–	mA
Tx Mode	22				
DI_{DD} (4800bps – Two-point)		–	4.3	–	mA
DI_{DD} (4800bps – I/Q)		–	5.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.0	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
Additional Current for each RF Synthesiser	24				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA

Notes:

21 T_{AMB} = 25°C, Not including any current drawn from the device pins by external circuitry.

22 System clocks, auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

24 When using the external components shown in Figure 26 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
RDATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} <1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:
25 Characteristics when driving the XTAL/CLK pin with an external clock source.
26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2 and Figure 3.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal start up (from powersave)			–	20	–	ms
System Clock 1/2 Outputs						
XTAL/CLK input to SysClk1/2 timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (p-p)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz Xtal fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at dc.

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB

37 Design value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD1, MOD2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the Xtal and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AUXADC1/4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10-Bit ADCs (AuxADC1/2)					
Resolution		–	10	–	Bits
Maximum Input Level (p-p)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10-Bit DACs (AuxDAC1/2)					
Resolution		–	10	–	Bits
Maximum Output Level (p-p), no load	54	80%	–	–	AV_{DD}
Zero error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 AuxADC output.

56 Output offset from a $0200 DAC input, measured with respect to a nominal V_{BIAS} output.

57 Measured at dc.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic '1'	62	70%	–	–	RFV_{DD}
Input Logic '0'	62	–	–	30%	RFV_{DD}
Frequency	64, 66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level (at 600MHz)		−15	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink to source match		–	5%	–	of ISET

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET1/2 resistor (R31 in Figure 26) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. At lower frequencies slew rate needs to be considered.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:

Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (e.g. RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (e.g. IF LO).

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with 7131/7141FI-6.x only. The use of other Function Images can modify the parametric performance of the device.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2400	–	4800	sym s^{-1}
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, Two-point)	70	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	70	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, PRBS)	71, 73	-60	–	–	dB
Rx Sensitivity (BER 4800 symbols/s)	72	–	TBD	–	dBm
Rx Co-channel Rejection	71, 73	15	12	–	dB
Rx System Adjacent Channel Rejection (I/Q Mode)	74	–	63		dB
Rx Input Level		–	–	838	mVrms
Rx Input dc Offset		0.5	–	AV_{DD} - 0.5	V

Notes:

70	Transmitting continuous default preamble.
71	See data sheet section 6.15.
72	Measured at base-band – radio design will affect ultimate product performance.
73	For a 6.25kHz/4800bps channel.
74	Combined performance of CMX7131/CMX7141 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201; measurement method from EN 301 166.

7.2 C-BUS Timing

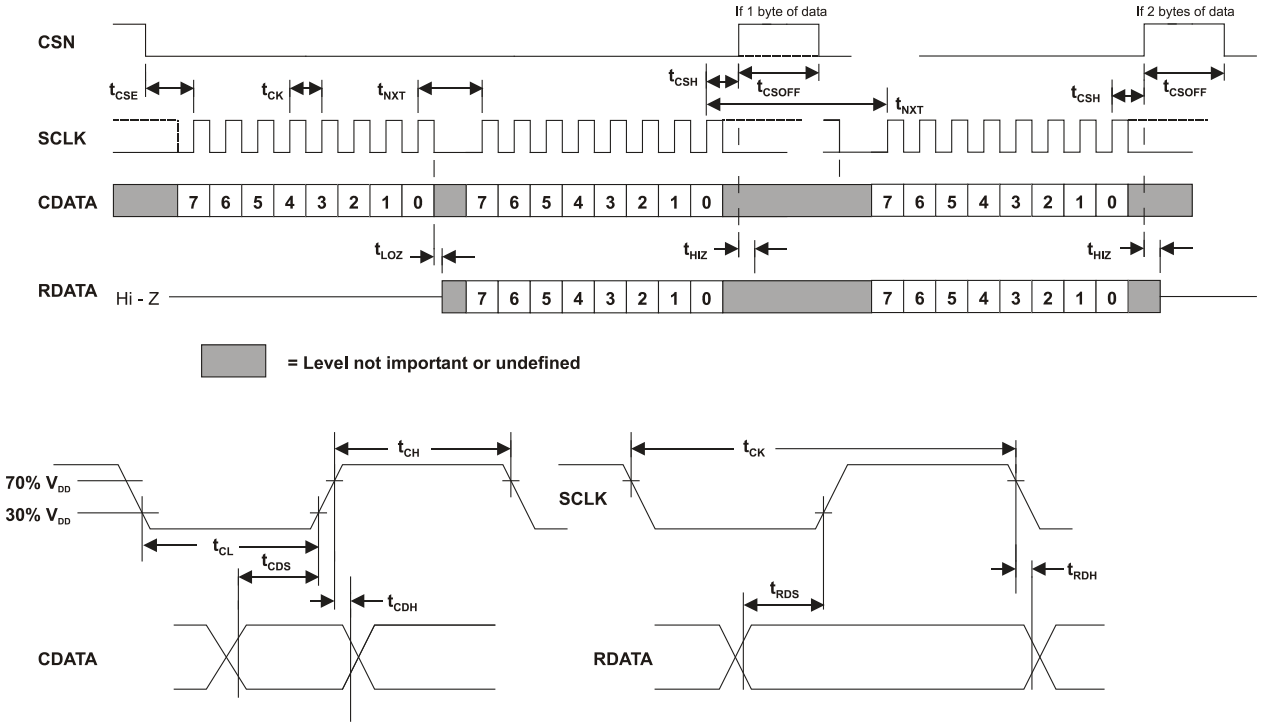


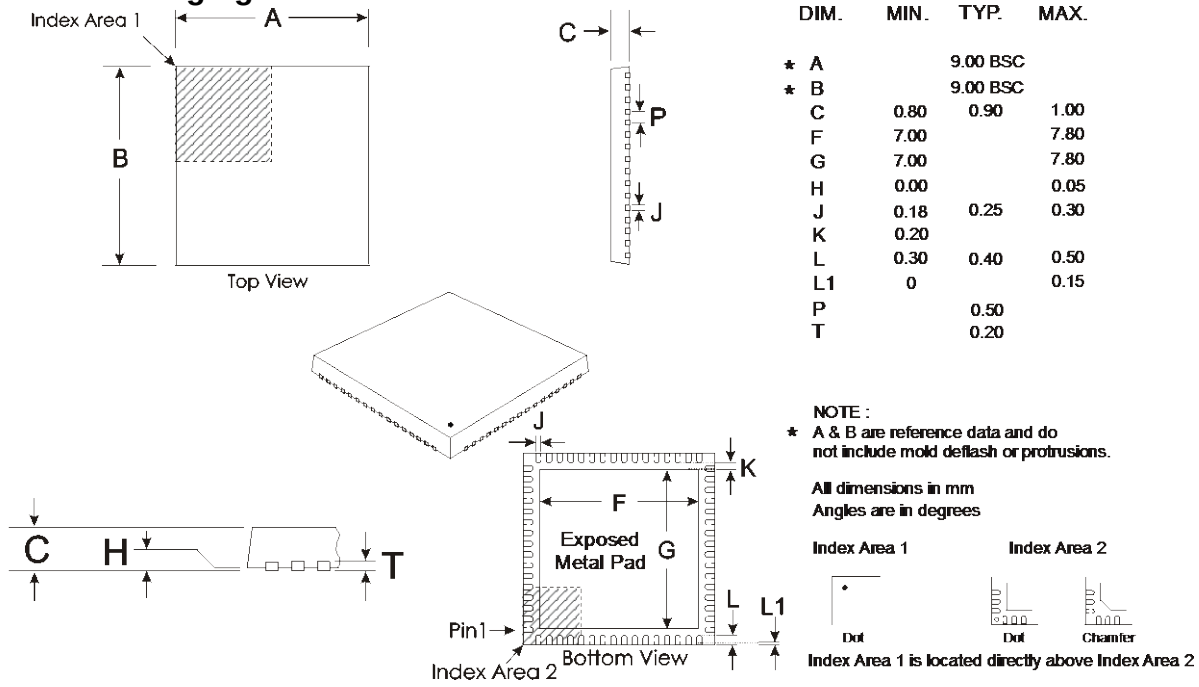
Figure 30 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7131/CMX7141 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

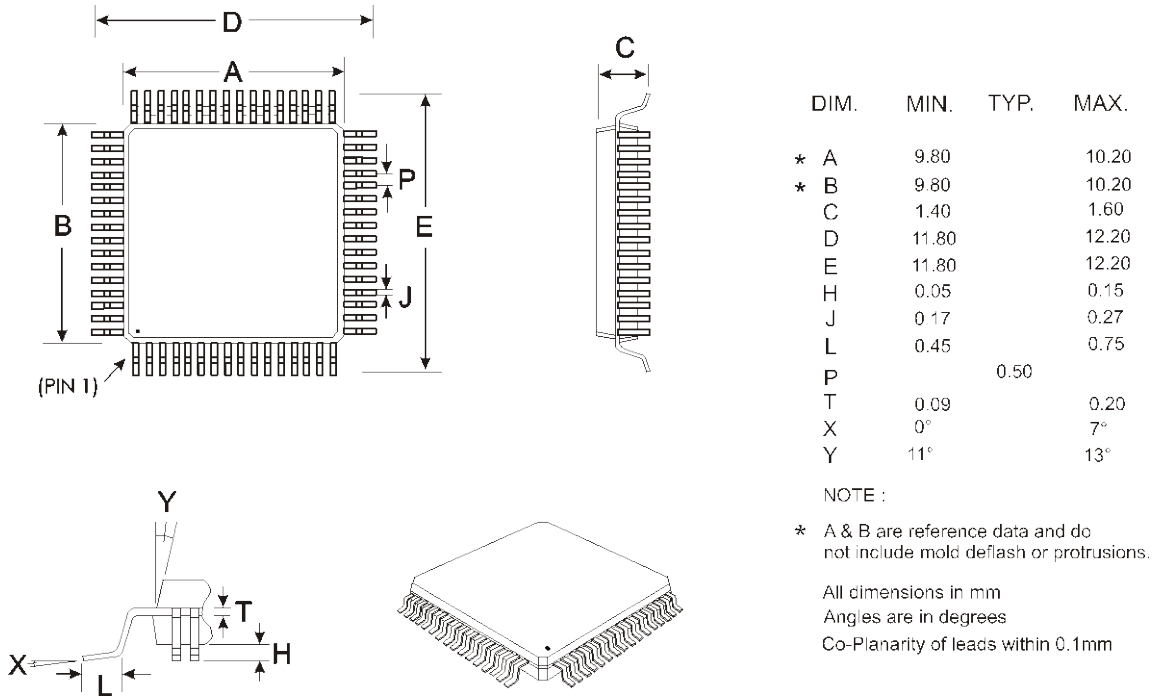
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 31 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7131Q1



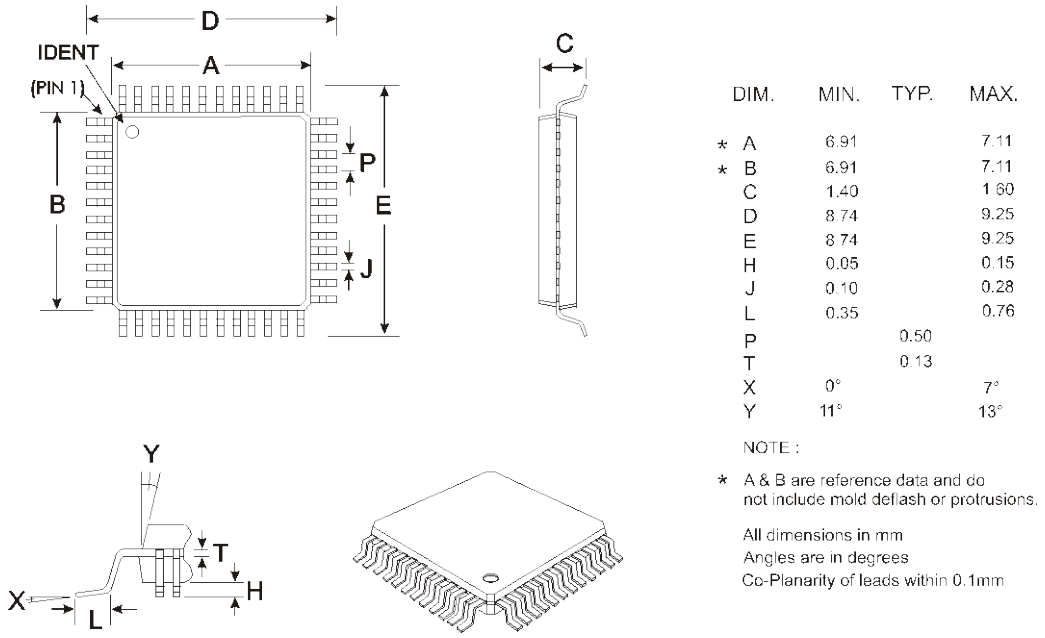
DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 32 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7131L9



	DIM.	MIN.	TYP.	MAX.
*	A	6.91		7.11
*	B	6.91		7.11
	C	1.40		1.60
	D	8.74		9.25
	E	8.74		9.25
	H	0.05		0.15
	J	0.10		0.28
	L	0.35		0.76
	P		0.50	
	T		0.13	
	X	0°		7°
	Y	11°		13°

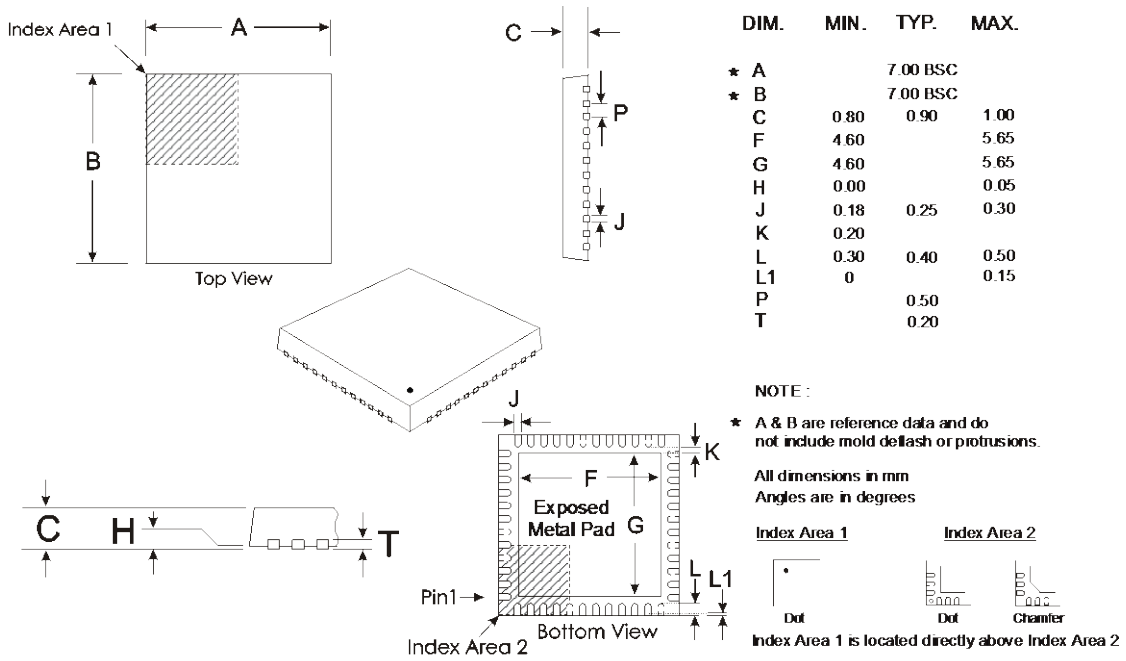
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 33 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7141L4



	DIM.	MIN.	TYP.	MAX.
*	A		7.00 BSC	
*	B		7.00 BSC	
	C	0.80	0.90	1.00
	F	4.60		5.65
	G	4.60		5.65
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Dot Dot Chamfer

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 34 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7141Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheet page of the CML website: [www.cmlmicro.com].

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7131/CMX7141
Digital PMR Processor
T102 Operation

UM/7131/41_FI-6.x/7 May 2016

USER MANUAL

Advance Information

7131/7141FI-6.x: ARIB STD-T102 Baseband Data Processor with Auxiliary System Clocks, ADCs and DACs

This User Manual is the second part of a two-part document.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

AMBE 3000 is a registered trademark of Digital Voice Systems Inc.

CONTENTS

Table Page

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.
It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com/].

8 Configuration Guide

8.1 C-BUS Register Details

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data/Control	16
$A9	R	AuxADC1 Data and Threshold Status/Checksum 2 hi	16
$AA	R	AuxADC2 Data and Threshold Status/Checksum 2 lo	16
$AB	W	System Clk 1 PLL Data	16
$AC	W	System Clk 1 REF	16
$AD	W	System Clk 2 PLL Data	16
$AE	W	System Clk 2 REF	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power-Down Control	16
$C1	W	Modem Control	16
$C2	W	TxAuxData	16
$C3	W	CMX6x8 Analogue Gain	16
$C5	R	Rx Data 4	16
$C6	R	Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	RxAuxData	16
$CD	W	Aux Config	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions.

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8.1.1 Reset Operations

A reset is automatically performed when power is applied to the CMX7131/CMX7141. A reset can be issued as a C-BUS command, either as a General Reset command ($01), or by setting the appropriate bit (b5) in the Powerdown Control register ($C0). In the latter case, an option exists to protect the values held in the Program Block (which is accessed via the Programming register, $C8). The action of each reset type is shown in the table below:

Table 19 Reset Operations

	Reset Type	BOOTEN pins (2, 1)	FI load Block 1 and 2	FI load Activation Block	Protect bit ($C0 b4) state	Activation Code	Program Block State
1	Power on	11 or 01	required	required	cleared by h/w	required	default
2	General Reset (C-BUS $01)	11 or 01	required	required	cleared by h/w	required	default
3	Reset (C-BUS $C0 b5)	11 or 01	optional	required	0	required	default
4	Reset (C-BUS $C0 b5)	11 or 01	optional	required	1	no	protected

Notes:
The Protect bit (C-BUS register $C0 b4) should NOT be set to 1 during an FI load.

The BOOTEN pins MUST be set to an appropriate state before and during any reset. After some types of reset, or after a new FI has been loaded, the device Activation Code will need to be sent before the CMX7131/CMX7141 exhibits any functionality (see Table 19). If the host detects a brownout, or other unexpected behaviour, it is recommended that the CMX7131/CMX7141 should be power-cycled and the FI re-loaded on completion of the power-on reset.

8.1.2 General Reset - $01 write

The General Reset command has no data attached to it. It sets all operational C-BUS registers to $0000, (apart from the registers marked as *reserved*). Note that some transient data may appear in the following registers during the power-up process – this should be ignored:

AuxADC1 Data	$A9	AuxADC2 Data	$AA
RF Synthesiser Status	$B4	Rx Data 0	$B8
Rx Data 1	$B9	Rx Data 2	$BA
Rx Data 3	$BB	Rx Data 4	$C5
Status	$C6	Modem Status	$C9
Aux Data Read	$CC		

Once the PRG flag (Status register, $C6 bit 0) is set to 1, the Device Identification Code ($7131 or $7141) can be read from the Rx Data 4 register ($C5). Power-on checksum 1 can be read from registers $B8 (hi word) and $B9 (lo word) and power-on checksum 2 can be read from registers $A9 (hi word) and $AA (lo word).

A power-on reset performs the same action as a General Reset command.

8.1.3 AuxADC Configuration - $A7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIOB wr	GPIOA wr	GPIOB mode	GPIOA mode	ADC2 Av Mode		ADC2 IP Select			ADC1 Av Mode		ADC1 IP Select			INV Rx/Tx	0

b15-14 GPIO write data. If enabled setting the appropriate bit in this field will assert the relevant GPIO pin.
b13-12 GPIO mode. If set to 1, the appropriate GPIO pin will become an input pin, which can be read back in the Modem Status register, $C9. Default is output.

		AuxADC Averaging Mode
b11	**b10**	**AuxADC2**
b6	**b5**	**AuxADC1**
1	1	*reserved*
1	0	*reserved*
0	1	Rolling average, uses Program Block 3.0 value
0	0	No averaging

			AuxADC Input Select
b9	**b8**	**b7**	**AuxADC2**
b4	**b3**	**b2**	**AuxADC1**
1	1	1	ADC4
1	1	0	ADC3
1	0	1	ADC2
1	0	0	ADC1
0	1	1	MIC
0	1	0	ALT
0	0	1	DISC
0	0	0	Off

b1 Invert the logic levels of RxENA and TxENA:
0 active low (default)
1 active high
b0 *reserved*

8.1.4 AuxDAC Data/Control - $A8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	0	Tone	RAM DAC	DAC Select		AuxDAC Data RAMDAC Control									

b15 ENA: enable selected AuxDAC 0 = disable 1 = enable
b14 *reserved*
b13 Tone: enable Aux Tone 0 = DAC2 operates normally
1 = DAC2 operates as tone generator. Data in b9-0 controls the output tone frequency (0-2kHz in 2Hz steps)[3]. The output tone amplitude is governed by b11-10:

e.g. For a 2Hz, 590mVrms tone, write: $A401
For a 30Hz, 590mVrms tone, write $A40F
For a 200Hz, 590mVrms tone, write: $A464
For a 200Hz, 300mV tone, write: $A864
For a 200Hz, 150mV tone, write: $AC64
For a 200Hz, 1.175Vrms tone, write: $A064

[3] DAC2 updates at 4kHz, therefore additional external filtering may be required to remove aliasing effects at higher frequencies. Above 500Hz, amplitude distortion may become apparent.

b12 RAMDAC: enable RAMDAC 0 = AuxDAC1 operates normally
1 = AuxDAC1 operates as a RAMDAC[4]. Data in b0-6 controls the RAMDAC functions.

b11, b10 DAC select: select the AuxDAC that b9-b0 data will be written to.
00 = AuxDAC1
01 = AuxDAC2
10 = AuxDAC3
11 = AuxDAC4

b9 – b0 AuxDAC data (unsigned)

Note: All other bit combinations not shown here are undefined and reserved for future use.

RAMDAC Operation:
When $A8 b12 is set to 1, writing data to this register controls the RAMDAC settings. Writing to DAC1 whilst the RAMDAC is still ramping may cause un-intended operation. In this mode b10 is ignored and the remaining bits perform the following functions:

b11 RAMDAC Scan Time multiplier – see Table 20
b10 *reserved*, clear to 0
b9 *reserved*, clear to 0
b8 *reserved*, clear to 0
b7 *reserved*, clear to 0
b6 Clear, clear to 0 for normal operation
set to 1 will reset the internal RAMDAC address pointer
b5-3 RAMDAC Scan Time:

Table 20 RAMDAC Scan Times

b5	b4	b3	Divider	RAMDAC Scan Time (ms)	
				b11=0	b11=1
0	0	0	1024	10.50	32
0	0	1	512	5.25	16
0	1	0	256	2.63	8
0	1	1	128	1.31	4
1	0	0	64	0.66	2
1	0	1	32	0.33	1
1	1	0	16	0.16	0.5
1	1	1	8	0.08	0.25

b2 Scan direction: 0 = Ramp down 1 = Ramp up
b1 Autocycle 0 = Disable 1 = Continuous ramp up/down
b0 RAMDAC start 0 = Stop 1 = Start RAMDAC ramping

To use the RAMDAC, proceed as follows:

First enable AuxDAC1, write: $8000
To initiate a RAMDAC ramp up, write: $9005
To initiate a RAMDAC ramp down, write: $9001
To stop RAMDAC at any time, write: $9000 (AuxDAC1 will return to its previous b9-0 value).
To powersave AuxDAC1, write: $0000

Notes:

- AuxDAC1 cannot be written to directly until the RAMDAC has been stopped, write: $9000 to stop.
- The C-BUS latency period (250µs) should be observed between successive writes to this register

[4] Do NOT write to directly to AuxDAC 1 whilst the RAMDAC is in operation. RAMDAC is only available when in Tx mode.

- RAMDAC operation is only available in Tx mode. Do NOT change mode whilst the RAMDAC is still ramping. Initiating a RAMDAC scan will NOT automatically bring DAC1 out of powersave.

8.1.5 AuxADC1 Data and Threshold Status- $A9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Aux Data Type				Aux Data (Type as indicated by upper nibble)											

b15-12	Aux Data Type selected (See register $CD Aux Config)
0000	Aux ADC 1 Data and threshold flags
0001	Aux ADC 2 Data and threshold flags
0010	Current AGC Gain and RSSI
0011	Squelch level
0100	*reserved*
0101	*reserved*
0110	Frequency error in Hz
0111	Result of CMX994 I/Q dc calibration
1000	*reserved*
1001	*reserved*
1010	*reserved*
1011	*reserved*
1100	*reserved*
1101	*reserved*
1110	*reserved*
1111	*reserved*

In each case the register result is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold Status		0	0	x	x	ADC1 Data									
Threshold Status		0	1	x	x	ADC2 Data									
0	0	1	0	AGC Gain step 0-8				RSSI (see Figure 10)							
0	0	1	1	Squelch level (Small = good signal) unsigned 12-bit number											
0	1	1	0	Frequency error in Hz, 2's complement signed 12-bit number											
0	1	1	1	*reserved*				Q Channel dc offset correction applied in CMX994				I Channel dc offset correction applied in CMX994			

Applicable to data types 0000_b, 0001_b:

b15, b14 Threshold Status

b15 = 1 Signal is above the high threshold
= 0 Signal is below the high threshold
b14 = 1 Signal is below the low threshold
= 0 Signal is above the low threshold

Applicable to data type 0111_b:

b3	b2	b1	b0	I Channel correction at maximum gain
b7	b6	b5	b4	Q Channel correction at maximum gain
1	1	1	1	-175mV
1	1	1	0	-150mV
1	1	0	1	-125mV

b3	b2	b1	b0	I Channel correction at maximum gain
b7	b6	b5	b4	Q Channel correction at maximum gain
1	1	0	0	-100mV
1	0	1	1	-75mV
1	0	1	0	-50mV
1	0	0	1	-25mV
1	0	0	0	No correction
0	1	1	1	+175mV
0	1	1	0	+150mV
0	1	0	1	+125mV
0	1	0	0	+100mV
0	0	1	1	+75mV
0	0	1	0	+50mV
0	0	0	1	+25mV
0	0	0	0	No correction

8.1.6 AuxADC2 Data and Threshold Status- $AA read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Aux Data TypeType				Aux Data (Type as indicated by upper nibble)											

Register detail is the same as register $A9 AuxADC1 Data and Threshold Status.

8.1.7 SYSCLK1 and SYSCLK2 PLL Data - $AB, $AD write
C-BUS address: $AB – System Clk 1 PLL
C-BUS address: $AD – System Clk 2 PLL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO Op Divide Ratio <5-0>						PLL Feedback Divide Ratio <9-0>									

b15-b10 Divide the selected output clock source by the value in these bits, to generate the System Clk output. Divide by 64 is selected by setting these bits to '0'.

b9-b0 Divide System Clk PLL VCO clock by value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the System Clk Reference and Source Configuration register ($AC). Divide by 1024 is selected by setting these bits to '0'.

8.1.8 SYSCLK1 and SYSCLK2 REF - $AC and $AE write
C-BUS address: $AC – System Clk 1 Ref
C-BUS address: $AE – System Clk 2 Ref

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select and PS Clock Sources					Op Slew		Ref Clock Divide Ratio <8-0>								

b15,12,11 Clk output divider source:

SYSCLK1 Source	b15	b12	b11
Xtal	0	X	X
SYSCLK PLL 1	1	0	0
Main PLL	1	0	1
Test	1	1	X

SYSCLK2 Source	b15	b12	b11
Xtal	0	X	X
SYSCLK PLL 2	1	0	0
Main PLL	1	0	1
SYSCLK1 PLL 1	1	1	0
Test	1	1	1

b14 Powersave PLL 0 = Powersave 1 = Enabled
b13 Powersave Output Divider 0 = Powersave bypass 1 = Enabled
b10-9 Output Slew Rate:

b10	b9	Output Slew Rate
0	0	Normal
0	1	Slow
1	0	Medium
1	1	Fast

b8-b0 Reference Clk divide value. Divide by 512 is selected by setting these bits to '0'.

Note that after a General Reset, the default setting will provide the XTAL frequency directly (CMX7131) or high impedance (CMX7141) on the SYSCLK1 and SYSCLK2 pins.

8.1.9 Analogue Output Gain - $B0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Inv_1	MOD1 Attenuation			Inv_2	MOD2 Attenuation			Input Invert	0	0	0	Audio Attenuation			

b15 MOD1 output polarity 0 = True 1 = Inverted
b11 MOD2 output polarity 0 = True 1 = Inverted
Used when interfacing with RF circuitry. Any change will take place immediately (within the C-BUS latency period) after these bits are changed.

b14	b13	b12	MOD1 Output Attenuation
b10	b9	b8	MOD2 Output Attenuation
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Fine level adjustment of MOD1 and MOD2 outputs can be achieved with the $C3 register.

(Also note that Fine level control of Output1 and Output2 can be achieved with the FINE OUTPUT ATTEN 1 and FINE OUTPUT ATTEN 2 registers (P4.2-3). These affect the MOD1, and MOD2 outputs according to the routing set in registers $A7 and $B1).

b7 Input Invert 0 = True 1 = Inverted (inverts the signal to Input 1 channel)
b6-4 reserved

b3	b2	b1	b0	Audio Output Attenuation
0	0	0	0	>60dB
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Audio Output is only available in SPI-Codec or Analogue PMR modes.

8.1.10 Input Gain and Signal Routing - $B1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input2 Gain			Input1 Gain			MOD1 Source		MOD2	AUDIO Source	Input1 Routing		Input2 Routing		RG IPS	SPI ENA

b12	b11	b10	Input1 Gain
b15	**b14**	**b13**	**Input2 Gain**
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

b7	MOD2 Source
0	V_{BIAS} -> MOD2
1	Output2 -> MOD2

b6	Audio Source
0	V_{BIAS} -> AUDIO
1	Output1 -> AUDIO

b5	b4	Input1 Signal Routing
b3	**b2**	**Input2 Signal Routing**
0	0	V_{BIAS}
0	1	DISC
1	0	ALT
1	1	MIC

b9	b8	MOD1 Signal Routing
0	0	V_{BIAS}
0	1	V_{BIAS}
1	0	Output1 -> MOD1
1	1	reserved

Note: In Tx I/Q mode, Output1 will provide the I signal and Output2 the Q signal. In Tx 2-point mode, both Output1 and Output2 provide the same signal.

b1 Regenerate FEC/Audio Codec Input Select:

If the Auxiliary C-BUS port is used with a CMX6x8 in C-BUS mode, then setting this bit in Rx will cause the CMX6x8 to correct the incoming data using its FEC, and then regenerate the FEC on the corrected bit stream and output it to the host. This is provided for repeater/base station operation.

If the Auxiliary C-BUS port is in SPI-Codec mode, then setting this bit selects the Input 2 block for routing Voice samples to the attached Vocoder rather than Input 1.

b0 SPI-Codec Enable (also see VOC_DIS, $C7:b7):

If VOC_DIS = 0

0 = Auxiliary SPI/C-BUS port in C-BUS mode
1 = Auxiliary SPI/C-BUS port in SPI Codec mode.
Port will be enabled automatically while a Voice call is in progress.

If VOC_DIS = 1

0 = Disable SPI-Codec
1 = Enable SPI-Codec

This bit must be set to the appropriate state before a change to Rx or Tx mode, ie: it can only be accessed during IDLE mode. Note that in SPI-Codec mode, in Tx operation, the transmit/mic signal should be routed through Input2 (which will then appear as PCM data on the SPI bus), and in Rx operation, the PCM data from the SPI bus is internally routed through Output1, which should then be routed to the AUDIO pin.

8.1.11 RF Synthesiser Data (CMX7131 only) - $B2 write

b15	b14	b13	b12	b11	b10	9 - 0
0	0	0	0	0	0	NUL
						RF Synthesiser 1
0	1	0	0	0	0	Load Tx N reg b9-0
0	1	0	0	0	1	Load Tx N reg b19-10
0	1	0	0	1	0	Load Tx R reg b9-0
0	1	0	0	1	1	Load Tx R reg b12-10
0	1	0	1	0	0	Load Rx N reg b9-0
0	1	0	1	0	1	Load Rx N reg b19-10
0	1	0	1	1	0	Load Rx R reg b9-0
0	1	0	1	1	1	Load Rx R reg b12-10
						RF Synthesiser 2
0	1	1	0	0	0	Load Tx N reg b9-0
0	1	1	0	0	1	Load Tx N reg b19-10
0	1	1	0	1	0	Load Tx R reg b9-0
0	1	1	0	1	1	Load Tx R reg b12-10
0	1	1	1	0	0	Load Rx N reg b9-0
0	1	1	1	0	1	Load Rx N reg b19-10
0	1	1	1	1	0	Load Rx R reg b9-0
0	1	1	1	1	1	load Rx R reg b12-10

N registers can be set from 1088 to 1048575. Settings outside this range are undefined.
R registers can be set from 2 to 8191. Settings outside this range are undefined.
b15 is reserved and should be cleared to 0.

8.1.12 RF Synthesiser Control (CMX7131 only) - $B3 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ref Clk Sel	Test	Tol	Sign	Gain	Rx	Tx	nPS	0	Test	Tol	Sign	Gain	Rx	Tx	nPS
	RF Synthesiser 2								RF Synthesiser 1						

b15 Reference Clk Source: 0 = RF synth clk 1 = XTAL
b14 b6 Test Mode: 0 = Normal 1 = test mode active
b13 b5 Phase Lock Tolerance 0 = 1 cycle 1 = 4 cycles (of reference clk)
b12 b4 Charge Polarity: 0 = Positive 1 = negative to increase VCO frequency
b11 b3 Charge Pump Gain: 0 = Low (625µA nominal) 1 = High (2.5mA nominal)

b2	**b1**	**RF Synthesiser 1**
b10	**b9**	**RF Synthesiser 2**
0	0	All Tx and Rx synthesisers disabled
0	1	Enable respective Tx synthesiser
1	0	Enable respective Rx synthesiser
1	1	NOT ALLOWED

b8 b0 Powersave 0 = powersave 1 = enabled

8.1.13 RF Synthesiser Status (CMX7131 only) - $B4 8-bit read

7	6	5	4	3	2	1	0
0	0	0	0	0	0	Synth 2 Lock	Synth 1 Lock

If either bits 1 or 0 of the this register change status, then bit 1 of the Status register is set to ‘1’,
Bit 1 of the Status register is not cleared until the RF Channel Status register is read.
Synthesiser 2 lock (bit 1) set to ‘1’ indicates that lock has been acquired on RF Synthesiser2.
Synthesiser 1 lock (bit 0) set to ‘1’ indicates that lock has been acquired on RF Synthesiser1.

See section 6.12 for further details of lock status operation.

8.1.14 TxData 0 - $B5 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxData bits 0-7								Transaction Counter		Block ID		Byte Counter			
CMX6x8 Pass-through b15-8								CMX6x8 Pass-through b7-0							
0								CMX994 Pass-through b7-0							

b7-6 Transaction Counter: modulo 4 counter that must be incremented every time the host writes a new block of data to the TxData registers. Note that the device detects that new data is available from the host by the change in value of this field: therefore the entire TxData Block must hold valid data when this field is updated and this register should be the last to be written to by the host in a TxData Block write sequence. The counter is reset to zero following a mode change (IDLE – Rx – Tx).

b5-4 Block ID: specifies the type of data loaded into the TxData registers:

b5-4	Block ID
00	*reserved*
01	Payload Data
10	RICH
11	RICH & SACCH

b3-0 Byte Counter: specifies the number of valid bytes of data loaded into the TxData registers.

b3-0	Byte Counter
0000	No data
0001	1 byte
- - - -	x bytes
1000	8 bytes
1001	9 bytes (maximum = 72bits)
1010	*reserved*
- - - -	*reserved*
1111	*reserved*

Note that data transfers which are not integer numbers of bytes should be padded with trailing zero's up to the byte boundary (ie: UDCH2 data).

In CMX6x8 Pass-through mode, the Programming Register ($C8) b14 should be set to 1 to indicate an 8-bit data write (data in $B5 b7-0) or cleared to 0 to indicate a 16-bit data write. The CMX6x8 register address is specified in $C8 b7-0.

In CMX994 Pass-through mode, the Programming Register ($C8) b14 should always be set to 1 as all data will be 8-bit write (data in $B5 b7-0). The CMX994 register address is specified in $C8 b7-0.

8.1.15 TxData 1 - $B6 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxData bits 8-15								TxData bits 16-23							

8.1.16 TxData 2 - $B7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxData bits 24-31								TxData bits 32-39							

8.1.17 RxData 0 - $B8 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxData bits 0-7								Transaction Counter		Block ID		Byte Counter			
x								CMX6x8 Pass-through b7-0							
x								CMX994 Pass-through b7-0							

b7-6 Transaction Counter: Modulo 4 counter that is incremented every time the CMX7131/CMX7141 loads a new block of data into the RxData registers. The counter is reset to zero following a mode change (IDLE – Rx – Tx).

b5-4 Block ID: specifies the type of data loaded into the RxData registers:

b5-4	Block ID
00	*reserved*
01	Payload Data
10	RICH
11	RICH & SACCH

b3-0 Byte Counter: specifies the number of valid bytes of data loaded into the RxData registers.

b3-0	Byte Counter
0000	No data
0001	1 byte
- - - -	x bytes
1000	8 bytes
1001	9 bytes (maximum = 72bits)
1010	*reserved*
- - - -	*reserved*
1111	*reserved*

Note that data transfers which are not integer numbers of bytes should be padded with trailing zero's up to the byte boundary (ie: UDCH2 data).

In CMX6x8 pass-through mode, an 8-bit data read will place data in $B8 b7-0, from the address specified in the Programming Register ($C8) b7-0.

In CMX994 Pass-through mode, these bits are undefined, as it is not possible to read from the CMX994 registers.

When 4-bit Log Likelihood Ratio (LLR) coding is used, 18 symbols will be transferred in the RxData registers, rather than 72 bits. Each symbol consists of a 4-bit nibble, coded as follows:

msb ... lsb	
0000	Most Confident 0
- - - -	- - - -
0111	Least Confident 0
1000	Least Confident 1
- - - -	- - - -
1111	Most Confident 1

The symbols are ordered in the same way as the hard-decision bits, so symbol 0 is transferred as bits 0 - 3 ($B8 b15 - 12) and symbol 17 is transferred as bits 68 - 71 ($C5 b3 - 0).

8.1.18 RxData 1 - $B9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxData bits 8-15								RxData bits 16-23							

8.1.19 RxData 2 - $BA read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxData bits 24-31								RxData bits 32-39							

8.1.20 RxData 3 - $BB read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxData bits 40-47								RxData bits 48-55							

8.1.21 Power Down Control - $C0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALT amp	MIC amp	DISC amp	IP1 ENA	OP1 ENA	OP2 ENA	MOD1 ENA	MOD2 ENA	Audio OP	BIAS	Reset	Prot	XTAL DIS	IP2 ENA	0	0

b15 ALT amp enable 0 = Off 1 = Enabled
b14 MIC amp enable 0 = Off 1 = Enabled
b13 DISC amp enable 0 = Off 1 = Enabled
b12 Input1 enable 0 = Off 1 = Enabled
b11 Output1 enable 0 = Off 1 = Enabled
b10 Output2 enable 0 = Off 1 = Enabled
b9 MOD1 enable 0 = Off 1 = Enabled
b8 MOD2 enable 0 = Off 1 = Enabled
b7 Audio Output enable 0 = Off 1 = Enabled
b6 BIAS block enable 0 = Off 1 = Enabled
b5 Reset 0 = normal 1 = Reset/powersave
b4 Program Block Protect 0 = normal 1 = Protected
If cleared, the Program Blocks will be initialised on Power on or reset. If set, then the Program Blocks will retain their previous contents.
b3 XTAL disable 0 = Enabled 1 = Disabled/powersave
Setting this bit effectively stops all signal processing within the device.
b2 Input2 enable 0 = off 1 = enable Input 2 path (required if using Tx with SPI and codec enabled)
b1 *reserved* 0 1 = DO NOT USE
b0 *reserved* 0 1 = DO NOT USE

Note: Care should be taken when writing to b5 and b3. These are automatically programmed to an operational state following a power-on (ie: all 0's). Writing a 1 to either b5 or b3 will effectively cause the device to cease all processing activity, including responding to other C-BUS commands (except General Reset, $01).

When b5 is set, the device will be held in reset and all signal processing will cease (including AuxADC operation); when subsequently cleared to 0, the BOOTEN pins will be read and the appropriate boot mode executed. In the Host Load configuration, if the FI is unchanged and the power supplies have remained stable during the reset period, it is permissible to leave the BOOTEN pins in the Host Load state and send only the Activation Block rather than the full FI to the device. Otherwise, the BOOTEN pins should be set to the "No FI Load" state BEFORE clearing the Reset.

When b3 is set the Xtal is disabled. When b3 is subsequently cleared, it may take some time for the clock signal to become stable, hence care should be taken in using this feature.

8.1.22 Modem Control - $C1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								Modem Control				Modem Mode			

b15-8 *reserved - 00000000*

b7-4	Rx Modem Control	Tx Modem Control
0000	Rx idle	Tx idle
0001	Rx T102 Formatted	Tx T102 Formatted
0010	Rx Raw	*reserved*
0011	Rx 4FSK Eye including I/Q dc calculation in RXDATA0, RXDATA1 and computed Powersave Levels 1, 2, 3 in RXDATA2-4.	Tx 4FSK PRBS
0100	Rx 4FSK Pass-through	Tx 4FSK Preamble
0101	*reserved*	Tx 4FSK Mod setup
0110	Sync	Test
0111	Reset/abort	Reset/abort
others	*reserved*	*reserved*

b3-0	Modem Mode	GPIO2 – TxENA	GPIO1 – RxENA
0000	IDLE – low power mode	1	1
0001	Rx mode	1	0
0010	Tx mode	0	1
0011	*reserved*	x	x
0100	CMX6x8/CMX994 Pass-through	1	1
0101	Rx with CMX994 I/Q cal	1	0
0110	*reserved*	x	x
0111	*reserved*	x	x
1000	*reserved*	x	x
1001	Rx with Powersave	1	0
others	*reserved*	x	x

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

In Tx mode, when Tx Formatted mode is selected the first block of data should have been loaded into the TxData registers before the Tx command was issued. If the Modem Control bits are set to Tx idle any remaining data in the device's internal buffers will be transmitted but no new data will be accepted.

The output signal generated by Tx 4FSK Mod Setup mode depends on the modulation type as set by b0 of the Modem Configuration register, $C7. In 2-point mode it will output a repeating sequence of eight +3 symbols followed by eight –3 symbols giving an alternating reference deviation. In I/Q mode it will output a continuous stream of +3 symbols giving a steady reference.

CMX6x8/CMX994 Pass-through mode will transfer data to/from the CMX6x8 or to the CMX994 C-BUS register address specified in the Programming register ($C8) via the TxData0/RxData0 registers. The direction of data transfer is determined by the setting of b15 of the Programming register (b0-7 contain the CMX6x8/CMX994 register address).

The following registers or bits can be changed whilst the device is in Tx or Rx mode as appropriate (Note: not all possible changes are appropriate):

- AuxADC Configuration - $A7 write
- AuxDAC Data/Control - $A8 write
- SYSCLK1 and SYSCLK2 PLL Data - $AB, $AD write
- SYSCLK1 and SYSCLK2 REF - $AC and $AE write
- Analogue Output Gain - $B0 write (except b7)
- Input Gain and Signal Routing - $B1 write (except b0)

- RF Synthesiser Data (CMX7131 only) - $B2 write
- RF Synthesiser Control (CMX7131 only) - $B3 write
- TxData 0 - $B5 write
- TxData 1 - $B6 write
- TxData 2 - $B7 write
- Power Down Control - $C0 write
- Modem Control - $C1 write
- CMX6x8 Analogue Gain- $C3 write
- TxData 3 - $CA write
- TxData 4 - $CB write
- Interrupt Mask - $CE write

Other registers should only be written to in IDLE mode, or will only become effective after a mode change.

8.1.23 TxAuxData - $C2 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								*reserved*							

Reserved for future use.

8.1.24 CMX6x8 Analogue Gain- $C3 write

The top four bits of this register activate different functions and allow them to be changed “on the fly” rather than through the program block mechanism.

$C3:b15-12				$C3:b11-0
15	**14**	**13**	**12**	
0	0	0	0	Vocoder gain settings
0	0	0	1	MOD fine gain $x000
0	0	1	0	Tx symbol level $x180
0	0	1	1	Rx SPI/PCM Voice level $xFFF
0	1	0	0	*reserved*
0	1	0	1	*reserved*
0	1	1	0	*reserved*
0	1	1	1	*reserved*
1	0	0	0	*reserved*
1	0	0	1	*reserved*
1	0	1	0	*reserved*
1	0	1	1	*reserved*
1	1	0	0	*reserved*
1	1	0	1	*reserved*
1	1	1	0	RAMDAC scaling $xFFF
1	1	1	1	FS Error Tolerance and Preamble Length $x109

0000_b: Vocoder Gain Settings

b11-10 *reserved - 00*
b9 Increase Mic/Input Gain by +20dB if set to ‘1’.
b8 Increase Speaker/Output Gain by +6dB if set to ‘1’.

b7-4	Input Gain (dB)
0000	0 (default)
0001	1.5
0010	3.0
0011	4.5
0100	6.0
0101	7.5
0110	9.0
0111	10.5
1000	12.0
1001	13.5
1010	15.0
1011	16.5
1100	18.0
1101	19.5
1110	21.0
1111	22.5

b3-0	Output Gain (dB)
0000	-14 (default)
0001	-12
0010	-10
0011	-8
0100	-6
0101	-4
0110	-2
0111	0
1000	2
1001	4
1010	6
1011	8
1100	10
1101	12
1110	14
1111	16

0001_b: Set MOD fine gain in 0.2 dB steps:

b11-8	b7-4: MOD2	b3-0: MOD1	Attenuation (dB)
0000	0000		0
0000	0001		0.2
0000	0010		0.4
0000	0011		0.6
0000	0100		0.8
0000	0101		1.0
0000	0110		1.2
0000	0111		1.4
0000	1000		1.6
0000	1001		1.8

0010b: Tx symbol level. Allows the level of 4FSK symbols to be adjusted in both LD and I/Q modes (default: x1 = $2180)

0011b Rx SPI/PCM voice level (default: x1 = $3FFF)

0100b to 1101b: *reserved*

1110b RAMDAC scaling (default: $EFFF)
This will automatically re-scale the values in the RAMDAC table so that the values can be changed without the host having to recalculate and re-load the entire table.

1111b FS Error Tolerance and Preamble Length (default $F209)
The FS Error Tolerance and Preamble Length field formats and meanings match those defined in Program Block P0.1. It is recommended that the FS Error Tolerance value be set to 1 to avoid potential problems with FS2 false detects.

8.1.25 RxData 4 - $C5 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxData bits 56-63								RxData bits 64-71							

8.1.26 Status - $C6 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	Event	Squelch	RSSI	Analog	x	Aux ADC2	Aux ADC1	Called	Tx Done	Data Ready	FS1 Det	FS2 Det	x	RF	PRG

b15 IRQ

Changes in the Status register will cause this bit to be set to 1 if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when this bit is 1 and the IRQ MASK bit (b15 of Interrupt Mask register, $CE) is set to 1.

b14 Event

The Modem Status register should be read to determine the cause.

b13: Squelch

Indicates that the received signal has a squelch level less than the threshold set using Aux Config - $CD. A low level indicates a good signal. Once a Squelch IRQ has been produced the Squelch threshold comparison is disabled, preventing further IRQs. It may be re-armed by re-writing the threshold to the Aux Config $CD register

b12: RSSI

Indicates that the received signal has an RSSI greater than the threshold set using Aux Config - $CD. A high level indicates a strong signal. Once a RSSI IRQ has been produced the RSSI threshold comparison is disabled, preventing further IRQs. It may be re-armed by re-writing the threshold to the Aux Config $CD register

b11 Analogue event

Do not use.

b10 *reserved*

Do not use.

b9 AuxADC2

Set when the AuxADC2 thresholds have been triggered.

b8 AuxADC1

Set when the AuxADC1 thresholds have been triggered.

b7 Called

Set when the User Code in an incoming call matches an Own-ID loaded in Program Block 1, or when the “All-Call” all zeros User Code is received. The matched Own-ID is reported to the host in the AuxData register, $CC. In Rx mode the host can maximise time spent in powersave by enabling this IRQ and ignoring the Frame Sync IRQs. The RxData available IRQ may be set at the same time to indicate the first block of control channel data can be read from the RxData registers.

b6 TxDone

Set when the last Tx symbol has left the modulator and the host can safely change the Modem Mode back to Rx or IDLE

b5 RxData available/TxData ready

Rx mode: set when there is data available for the host to read from the RxData registers

Tx mode: set when the modem is ready to receive new data in the TxData registers

b4 Frame Sync 1 Detected

Set when a Preamble + Sync Word sequence has been detected

b3 Frame Sync 2 Detected

Set when a Sync Word without a Preamble has been detected

b2 *reserved*

Do not use

b1 RF

CMX7131 only – RF synthesiser status

b0 Programming Register Ready (PRG) flag

When this bit is set to 1 the Programming register, $C8 is available for host writes. After each write the host must wait for it to be re-set before writing to the Programming register again.

Bits 2 to 15 of the Status register are cleared to '0' after the Status register is read.

The data in this register is not valid if bit 5 of the Power Down Control register, $C0 is set to 0.

8.1.27 Modem Configuration - $C7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx/Rx Sequencer		FS Timing	Open Rx	No Pre	Voc Sel	FS2 Config	FS2 Enable	VOC DIS	0	0	Soft Data	Sinc Filter	0	0	Tx_I/Q

b15 Tx Sequencer
0 = disable Tx sequencer
1 = enable Tx Sequencer when entering Tx mode
b14 Rx Sequencer
0 = disable Rx sequencer
1 = enable Rx Sequencer when entering Rx mode
b13 Frame Sync Timing
0 = Discard timing information (default)
1 = Maintain symbol and frame timing for use in Frame Sync 2 detects
b12 Open Rx
0 = Incoming calls are accepted only if address and Information Type are valid (default)
1 = Open Receiver (all incoming calls are accepted)

Note that if b12 is set to 1 (Open Receiver mode), the CMX7131/CMX7141 will not wait for the 'Front Unit' flag bit in the SACCH block before accepting incoming calls. In this case, the host will need to perform the check.

b11 0 = Tx with preamble (default)
1 = Tx with no preamble
b10 0 = Use Vocoder 1 (default)
1 = Use Vocoder 2
b9 0 = Require Sync Words in two successive frames for an FS2 detect (default)
1 = Allow initial Frame Sync 2 detects from a single Sync Word (not recommended)
b8 0 = Disable Frame Sync 2 detects (default)
1 = Enable Frame Sync 2 detects (Sync Word without a Preamble)
b7 0 = Enable Automatic Vocoder operation - port becomes active during Voice Calls (default)
1 = Disable Automatic Vocoder operation – port manually controlled by SPI_ENA)
b6-5 *reserved*
b4 0 = Hard decision payload data output in RxData registers (default)
1 = 4-bit LLR payload data output in RxData registers
b3 0 = Enable Sinc shaping filters (default)
1 = disable Sinc shaping filters
b2 *reserved*
b1 *reserved*
b0 0 = MOD1 and MOD2 in 2-point modulation mode (default)
1 = MOD1 and MOD2 in I/Q modulation mode

The Modem Configuration register should only be written to when the device is in IDLE mode. Settings will take effect when the device is put into Tx or Rx mode (by writing to the Modem Control register $C1).

8.1.28 Programming Register - $C8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Program Block Address				Program Block Data											
RD	8-bit	0	0	0	0	0	0	CMX6x8 Register Address							
0	1	1	0	0	0	0	0	CMX994 Register Address							

See section 8.2 for a definition of programming block operation.

Pass-through modes are enabled using the Modem Control register ($C1):

In CMX6x8 Pass-through mode (b13=0), b15 set to 1 indicates a read, cleared to 0 indicates a write command to/from the address defined in $C8 b7-0. When writing data, b14 set to 1 indicates 8-bit data in the TxData0 register ($B5) b7-0, b14 cleared to 0 indicates 16-bit data in register $B5.

In CMX994 Pass-through mode (b13=1), b15 should always be cleared to 0 indicating a write command to the address defined in $C8 b7-0. All data is 8-bit and transferred via TxData0 ($B5) b7-0, so b14 should be set to 1. It is not possible to read from the CMX994 registers.

8.1.29 Modem Status - $C9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	Ramp	x	x	I/Q Demod Status		Modem Status				GPIO Read		x	x

b15-13 *reserved*
b12 RAMDAC ramping in progress
b11-10 *reserved*
b 9-8 I/Q Demod Status

The I/Q demodulation process can raise an Event IRQ, and will update its status on certain events:

I/Q Demod Status b9,8	Status/Event
00	Idle
01	CMX994 Calibration sequence complete
10	Powersave mode exited due to signal detection
11	*reserved*

b7-4 4FSK Modem Status

b7-b4	Status/Error Condition	Note
0000	Modem idle	
0001	Rx – no data detected	
0010	Rx – receiving data	
0011	Rx – call dropped	
0100	Tx – ramping	
0101	Tx – sending data	
0110	Framesync not recognised	
0111	*reserved*	
1000	SACCH CRC failure	
1001	RICH parity failure	
1010	SACCH/RICH CRC and parity failure	
1011	*reserved*	
1100	FACCH CRC failure	
1101	Data out of sequence (Transaction counter error in Tx)	
1110	Data Overrun in Rx	
1111	Data Underrun in Tx	

b3 GPIOB Input state
b2 GPIOA Input state
b1 *reserved*
b0 *reserved*

8.1.30 TxData 3 - $CA write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxData bits 40-47								TxData bits 48-55							

8.1.31 TxData 4 - $CB write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxData bits 56-63								TxData bits 64-71							

8.1.32 RxAuxData - $CC read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID match			x	x	x	x	x	x	Manufacturer ID						

When a “Called” IRQ is issued, this register indicates which Own-ID was matched against the User Code contained in the incoming call.

b15-13 Matched Own-ID:
000 = No match
001 = ID 1 matched
010 = ID 2 matched
011 = ID 3 matched
100 = ID 4 matched
101 = ID 5 matched
110 = ID 6 matched
111 = All-Call.

b12-7 *Reserved* – do not use

b6-0 Manufacturer ID received

8.1.33 Aux Config - $CD write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parameter Select				Aux Data											

A write to the Aux Config $CD register allows configuration of various Auxiliary data parameters, such as powersave thresholds (see section 6.6.18). The parameter type is selected using bits 15-12, and the parameter data is given in bits 11-0. Allowed parameters are as follows:

Parameter Select (b15-12)	Parameter set using Aux Data (b11-0)
0000	Aux ADC1 low threshold
0001	RSSI high threshold
0010	Squelch low threshold
0011	Aux 1 data and Aux 2 data output selection
0100	Aux ADC1 high threshold
0101	Powersave threshold 1 (Sampled energy) – [default = 300_d]
0110	Powersave threshold 2 (On channel energy) – [default = 263_d]
0111	Powersave threshold 3 (Squelch energy) – [default = 4000_d]
1000	Aux ADC 2 low threshold
1001	Power save off time – [default = 100_d]
1010	*reserved*
1011	*reserved*
1100	Aux ADC 2 high threshold
1101	*reserved*
1110	*reserved*
1111	*reserved*

8.1.34 Interrupt Mask - $CE write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	Event	Squelch	RSSI	Analog	0	Aux ADC2	Aux ADC1	Called	Tx Done	Data RDY	FS1 Det	FS2 Det	0	RF	PRG

See section 8.1.26.

8.1.35 Reserved - $CF write

This C-BUS address is allocated for production testing and must not be accessed in normal operation.

8.2 Programming Register Operation

In order to support radio systems that may not comply with the default settings of the CMX7131/CMX7141, a set of Program Blocks is available to customise the features of the device. It is envisaged that these blocks will usually only be written to following a power-on of the device and hence can only be accessed while the device is in IDLE mode (Modem Control register, $C1:b3-0 = 0000).. Access to these blocks is via the Programming register ($C8).

All other interrupt sources should be disabled and the AuxADCs switched off while loading the Program Blocks.

The Programming register should only be written to when the PRG flag in the Status register ($C6 bit 0) is set to 1 and the Rx and Tx modes are disabled (b3-0 = 0000 in the Mode Control register, $C1) and the AuxADC is disabled.

The PRG flag is cleared when the Programming register is written to by the host. When the corresponding programming action has been completed (normally within the C-BUS latency period, 250µs) the CMX7131/CMX7141 will set the flag back to 1 to indicate that it is now safe to write the next programming value. The Programming register must not be written to while the PRG flag bit is 0. Programming is performed by writing a sequence of 16-bit words to the Programming register in the order shown in the following tables. Writing data to the Programming register MUST be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g. If only 'Fine Output Atten 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block.

The internal pointer for each Program block write is initialised by setting bit 15 to 1. Bits 14-12 are then used to select the particular Program block in use, as shown in Table 21. Subsequent writes to the Programming register (with b15 cleared to 0) will increment the pointer until the end of the Program Block is reached. Program Block 3 has an additional feature to facilitate RAMDAC programming, where the first eleven entries of the block may be skipped by setting both b15 and b10 to 1 to initialise the pointer directly to the start of the RAMDAC table.

Table 21 Program Block Selection

b15	b14	b13	b12		Bit field (max)
1	0	x	x	Select Block 4	14
1	1	0	0	Select Block 0	12
1	1	0	1	Select Block 1	12
1	1	1	0	Select Block 2	12
1	1	1	1	Select Block 3	12

Once the final write to the Programming register has been executed, a final check of the PRG flag should be performed before returning to normal operation.

8.2.1 Program Block 0 – Modem Configuration

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	Call Drop Threshold (default=5)											
P0.1	0	1	0	0	FS Error Tolerance				Preamble Length (bytes)							
P0.2	0	1	0	0	Repeated END frames				Repeated HEADER frames							
P0.3	0	1	0	0	*reserved – clear to 0*											
P0.4	0	1	0	0	*reserved – clear to 0*											
P0.5	0	1	0	0	*reserved – clear to 0*											
P0.6	0	1	0	0	*reserved – clear to 0*											
P0.7	0	1	0	0	*reserved – clear to 0*											
P0.8	0	1	0	0	*reserved – clear to 0*											
P0.9	0	1	0	0	*reserved – clear to 0*											
P0.10	0	1	0	0	*reserved – clear to 0*										IFD	Rx_ I/Q

Default values:

P0.0	$005	P0.5	
P0.1	$209	P0.6	
P0.2	$000	P0.7	
P0.3		P0.8	
P0.4		P0.9	
		P0.10	$000

P0.3 to P0.9 should be cleared to zero when programming location P0.10.

The number of Repeated Frames specifies the number of additional frames sent:

b11-8 – number of additional END frames

b7-0 – number of additional HEADER frames

The Call Drop Threshold specifies the number of consecutive corrupt frames required for the T102 receiver to automatically drop a call and restart Frame Sync search. Frames are considered corrupt if the Frame Sync Word is received incorrectly (3 or more bit errors). Dropped calls are reported with a status code in the Modem Status register ($C9) and an "Event" interrupt. If the threshold is set to zero the T102 receiver will never drop calls.

The FS Error Tolerance field specifies the number of bit errors that can be tolerated and a valid FS still be indicated. Bit 11 is the msb.

The Preamble Length specifies the number of repeating symbols of preamble [+3 +3 -3 -3] sent in Tx Mode in addition to the 12 symbols defined in the standard (default = 0, maximum = 127).

The IFD bit inverts the FM demod signal when set to 1.

The Rx_I/Q enable bit selects I/Q mode when set to 1, LD mode when cleared to 0.

8.2.2 Program Block 1 – Own ID Settings:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	0	0	0	0	0	0	Own-ID 1					
P1.1	0	1	0	1	0	0	0	0	0	0	Own-ID 2					
P1.2	0	1	0	1	0	0	0	0	0	0	Own-ID 3					

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.3	0	1	0	1	0	0	0	0	0	0	Own-ID 4					
P1.4	0	1	0	1	0	0	0	0	0	0	Own-ID 5					
P1.5	0	1	0	1	0	0	0	0	0	0	Own-ID 6					
P1.6	0	1	0	1	0	0	0	0	Manufacturer ID 1							
P1.7	0	1	0	1	0	0	0	0	Manufacturer ID 2							
P1.8	0	1	0	1	0	0	0	0	Manufacturer ID 3							
P1.9	0	1	0	1	0	0	0	0	Manufacturer ID 4							
P1.10	0	1	0	1	0	0	0	0	Manufacturer ID 5							
P1.11	0	1	0	1	*reserved – clear to 0*											
P1.12	0	1	0	1	SCLKPol		0	0	*reserved – clear to 0*							
P1.13	0	1	0	1	*reserved – clear to 0*											
P1.14	0	1	0	1	SCLKPol		0	0	*reserved – clear to 0*							
P1.15	0	1	0	1	CMX6x8 initialisation word 1: VCFG ($07=$14)											
P1.16	0	1	0	1	CMX6x8 Idle configuration word 1: Powersave ($09=$10)											
P1.17	0	1	0	1	CMX6x8 Idle configuration word 2: VCTRL_lo ($11=$00)											
P1.18	0	1	0	1	CMX6x8 Idle configuration word 3: VCTRL_hi ($11=$00)											
P1.19	0	1	0	1	CMX6x8 Idle configuration word 4: EXCODCONT ($xx=$00)											
P1.20	0	1	0	1	CMX6x8 Rx configuration word 1: Powersave ($09=$13)											
P1.21	0	1	0	1	CMX6x8 Rx configuration word 2: VCTRL_lo ($11=$09)											
P1.22	0	1	0	1	CMX6x8 Rx configuration word 3: VCTRL_hi ($11=$00)											
P1.23	0	1	0	1	CMX6x8 Rx configuration word 4: EXCODCONT ($xx=$00)											
P1.24	0	1	0	1	CMX6x8 Tx configuration word 1: Powersave ($09=$13)											
P1.25	0	1	0	1	CMX6x8 Tx configuration word 2: VCTRL_lo ($11=$02)											
P1.26	0	1	0	1	CMX6x8 Tx configuration word 3: VCTRL_hi ($11=$00)											
P1.27	0	1	0	1	CMX6x8 Tx configuration word 4: EXCODCONT ($xx=$00)											

Default values:

P1.0:	$000	P1.15	$014
P1.1:	$000	P1.16	$010
P1.2	$000	P1.17	$000
P1.3	$000	P1.18	$000
P1.4	$000	P1.19	$000
P1.5	$000	P1.20	$013
P1.6	$000	P1.21	$009
P1.7	$000	P1.22	$000
P1.8	$000	P1.23	$000
P1.9	$000	P1.24	$013
P1.10	$000	P1.25	$002
P1.11	$000	P1.26	$000
P1.12	$000	P1.27	$000
P1.13	$000		
P1.14	$000		

P1.0 to 1.5 set the unit's 6-bit Own-IDs. If P1.0 is cleared to zero, the device will accept any User Code when validating incoming T102 calls in Rx mode (this is the default state).

P1.6 to 1.10 set the Manufacturer ID codes that will be accepted for a valid call. If cleared to zero (default) all ID's will be accepted.

Bits 11 and 10 of P1.12 specify the EPSCLK polarity used by the vocoder when using SPI-CODEC mode.

P1.15 to 1.27 define the default configuration values for the CMX6x8. These values will be written to the defined registers in the CMX6x8 at:

- o Initialisation
- o IDLE mode
- o Rx mode
- o Tx mode

The device defaults to CMX618 using internal codecs. If a CMX608 or external codecs are in use, then additional set-up commands may be required, which can be executed by the host and the CMX6x8 pass-through facility. See the relevant CMX6x8 data sheet for details.

8.2.3 Program Block 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	I/Q AGC	0	0	HW AGC	0	0	0	0	0	0	0	0

Default values: P2.0: $000

b11 Disable I/Q AGC function in CMX994
b10-9 r*eserved*
b8 Hardware AGC enable – uses external components and AuxADC1 as shown in Figure 6, see section 5.2.7
b7-0 *reserved*

8.2.4 Program Block 3 – AuxDAC, RAMDAC and Clock Control

This block is divided into two sub-blocks to facilitate loading the RAMDAC buffer. Set bit 15 to restart a loading sequence. If bit 10 is set then loading the first ten locations will be skipped. If bit 10 is clear, the first ten locations must be loaded before continuing to the RAMDAC load.

The Internal clk dividers only require modification if a non-standard Xtal frequency is used (see Table 9).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3.0	1	1	1	1	0	0	0	0	AuxADC1 Average Counter							
P3.1	0	1	1	1	0	0	0	0	reserved							
P3.2	0	1	1	1	GP Timer value in IDLE mode											
P3.3	0	1	1	1	VCO output and AUX clk divide in IDLE mode											
P3.4	0	1	1	1	Ref clk divide in Rx or Tx mode											
P3.5	0	1	1	1	PLL clk divide in Rx or Tx mode											
P3.6	0	1	1	1	VCO output and AUX clk divide in Rx or Tx mode											
P3.7	0	1	1	1	0	0	0	0	Internal ADC/DAC clk divide in Rx or Tx mode							
P3.8	0	1	1	1	0	0	0	0	ADC Internal Control 1							
P3.9	0	1	1	1	0	0	0	0	ADC Internal Control 2							
P3.10	0	1	1	1	0	0	0	0	0	0	0	0	ADC Internal Control 3			
P3.11	1	1	1	1	0	1	User Defined RAMDAC data 0									
P3.xx	0	1	1	1	0	1	User Defined RAMDAC data xx									
P3.74	0	1	1	1	0	1	User Defined RAMDAC data 63									
P3.75	0	1	1	1	Tx Sequencer Timer – Tx_ENA active delay											
P3.76	0	1	1	1	Tx Sequencer Timer – Ramp UP delay											
P3.77	0	1	1	1	Tx Sequencer Timer – Modulation Start Time											
P3.78	0	1	1	1	Tx Sequencer Timer – Ramp Down delay											
P3.79	0	1	1	1	Tx Sequencer Timer – Tx_ENA inactive delay											
P3.80	0	1	1	1	Tx Sequencer RAMDAC scan time configuration											

Default Values:

P3.0	$000
P3.1	$000
P3.2 - P3.7:	see Table 9
P3.8	$000
P3.9	$101
P3.10	$002
P3.11 - P3.74:	see Table 22
P3.75 – P3.80:	see Table 23

Table 22 RAMDAC Values

Default DAC RAM contents after reset (hexadecimal)															
0 000	1 001	2 003	3 006	4 00A	5 010	6 017	7 01F	8 028	9 033	10 03E	11 04B	12 059	13 068	14 078	15 089
16 09A	17 0AD	18 0C1	19 0D5	20 0EA	21 100	22 116	23 12D	24 145	25 15D	26 175	27 18E	28 1A7	29 1C0	30 1D9	31 1F3
32 20C	33 226	34 23F	35 258	36 271	37 28A	38 2A2	39 2BA	40 2D2	41 2E9	42 2FF	43 315	44 32A	45 33E	46 352	47 365
48 376	49 387	50 397	51 3A6	52 3B4	53 3C1	54 3CC	55 3D7	56 3E0	57 3E8	58 3EF	59 3F5	60 3F9	61 3FC	62 3FE	63 3FF

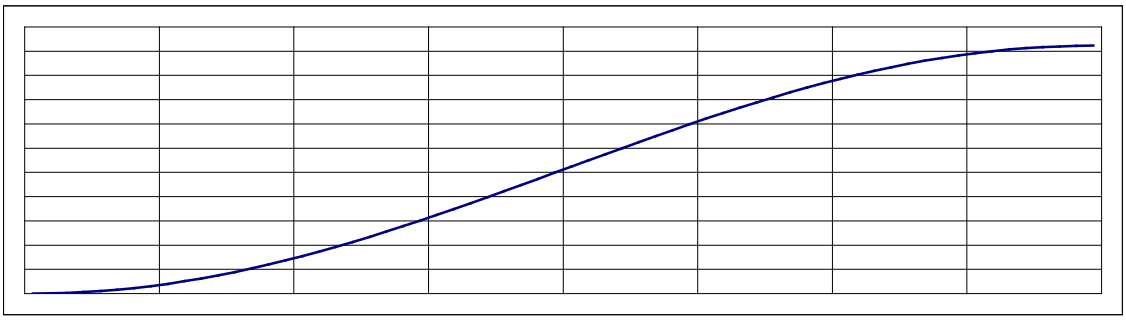


Table 23 Tx Sequencer Values

	Default Value	Description
P3.75	$000	Delay between the Tx Command received and Tx_ENA becoming active
P3.76	$000	Delay between the TX Command received and the RAMDAC starting up
P3.77	$050	Delay between the Tx Command and the start of the Modulation
P3.78	$000	Delay from End of Modulation (TxDone) to RAMDAC starting down
P3.79	$050	Delay from End of Modulation to Tx_ENA becoming inactive
P3.80	$000	Tx Sequencer RAMDAC scan time configuration

Note: the delay values are in multiples of 250µs. Delays from End of Modulation (TxDone) are interpreted as signed values, allowing the associated actions to be triggered up to 5ms before the TxDone IRQ is issued, if required.

The RAMDAC scan time configuration (P3.80) defines the duration of the ramp (up and down) to be applied when the sequencer is used. It is set according to Table 20 RAMDAC Scan Times. Only the relevant bits (b11, b5-3) are functional in this field. When the sequencer is triggered any previously programmed RAMDAC scan time will be overwritten by the current value in this location.

8.2.5 Program Block 4 – Gain and Offset Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	*reserved – clear to 0*													
P4.1	0	0	*reserved – clear to 0*													
P4.2	0	0	Fine Output Atten 1													
P4.3	0	0	Fine Output Atten 2													
P4.4	0	0	Output 1 Offset Control													
P4.5	0	0	Output 2 Offset Control													

Default values:

P4.0	$8000	P4.3	$0000
P4.1	$0000	P4.4	$0000
P4.2	$0000	P4.5	$0000

$C8 (P4.0) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	*reserved – clear to 0*													

This register is reserved and should be cleared to '0'.

$C8 (P4.1) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.1	0	0	*reserved – clear to 0*													

This register is reserved and should be cleared to '0'.

$C8 (P4.2-3) Fine Output Atten 1 and Fine Output Atten 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Atten 1 (unsigned integer)													
P4.3	0	0	Fine Output Atten 2 (unsigned integer)													

Atten = 20 × log([32768-OG]/32768)dB. OG is the unsigned integer value in the 'Fine Output Gain' field.

Fine output gain adjustment should be kept within the range 0dB to -3.5dB. This adjustment occurs before the coarse output gain adjustment (register $B0). Alteration of Fine Output Gain 1 will affect the gain of both MOD1 and AUDIO outputs. Fine gain adjustment of the CMX7131/CMX7141 MOD1 and MOD2 outputs can be made directly by the 0001_b subfield of the CMX6x8 Analogue Gain ($C3) register: this is the preferred fine gain adjustment method, as there is no need to return to IDLE mode.

$C8 (P4.4-5) Output 1 Offset and Output 2 Offset

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's Complement offset for MOD1, resolution = AV_{DD} / 65536 per LSB													
P4.5	0	0	2's Complement offset for MOD2, resolution = AV_{DD} / 65536 per LSB													

The programmed value is subtracted from the output signal. Can be used to compensate for inherent offsets in the output path via MOD1 (Output 1 Offset) and MOD2 (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV. This adjustment occurs before the coarse output gain adjustment (register $B0), therefore an alteration to the latter register will require a compensation to be made to the output offset.

8.2.6 Initialisation of the Program Blocks

Removal of the Signal Processing block from reset (Power-down register, $C0, b5 1→ 0), with b4 kept low (= 0), will cause all of the Program Blocks (P0 – P4) to be reset to their default values.

9 Function Image™ Updates

```
VERSION HISTORY: CMX7141 FI-6 T102 MODEM
========================================

Version 6.1.2.3
===============

o If both Audio routing enabled in $B1 and manual SPI control selected,
Output1
  will now remain enabled when mode changed (previously it would automatically
  shut down).
o EPCSN bug fixed on 7241/7341 hardware (does not affect 7131/7141 hardware).


Version 6.1.2.2
===============

o Engineering test build - *** NOT FOR GENERAL RELEASE ***
  Rx-only.
  CMX994 C-BUS access modified to avoid possible bus contention with SPI-
Codec.
o SPI bus synchronisation bug fixed on 7241/7341 hardware (does not affect
7131/7141 hardware).


Version 6.1.2.1
===============

o I/Q operation: CMX994 AGC hysteresis corrected.
o Setting transaction type bits on last data to 00 supresses Tx underrrun
errors.
o Optimisations to FS2 search for late entry. Timing requirements tightened up
to
  reduce false detections.
o T102 frame type processing tweaked to frames in the case of corrupted RICH
data.
o Bug fix - Bad frame count re-initialised on each received voice burst


Version 6.1.2.0
===============

o I/Q Rx Channel Filter - filter bandwidth tuned to give improved
  adjacent channel rejection.
o RxENA and TxENA can be inverted by setting $A7 = xxxx xxxx xxxx xx10
o TxUnderflow indication removed when Tx_REL detected.
o Reduction in possible transients on SPI bus at mode changes.
o Bug fix for MainCLK PLL settling time when entering active modes.
o Removed squelch measurement in I/Q mode (not required for digital
operation).
o Reduced complexity of atan lookup function for CMX7141 platform.
o Improved CMX7241 compatibility - SYSCLK1 disabled at startup, EPCSN
  released after booting, Output1/2 power-on glitch removed, unused RAM
initialised..
o Make use of hardware acceleration features of CMX7241/7341 when available
(CORDIC).
o Changed Powersave operation on CMX994 to use reg $12 instead of reg $11
```

```
Version 6.1.1.0
===============

o Bug in Tx Sequencer initialisation fixed.
o Tx sequencer RAMDAC timer values specified in P3.80, same
  format as normal RAMDAC ramp control shown in table 20.

Imported updates from the NXDN project 3.1.0.8:

o Improved SPI bus communication to avoid potential bus coflicts between
CMX994,
  vocoder and SPI codec modes. SPI codec can be enabled/disabled manually
  whilst in Rx mode using $B1:b0.
o Release Note "CMX7131 / CMX7141 / CMX8341 Function Image Release Notes"
dated
  8th November 2013 also applies to this FI.
o Reduced CMX994 calibration time in I/Q mode.
o Applied DC level tracking to Rx Eye in I/Q mode.
o Optimised SPI use for Vocoder control (Reduces C-BUS activity).
o Added SPI/PCM Rx Voice level scaling as $C3:3xxx.
o Added RAMDAC scaling feature as $C3:Exxx
  Note that the RAMDAC profile can only be loaded whilst in Idle mode, BUT
  the RAMDAC itself will only become active in Tx mode. For test purposes,
  $A8=$9007 will ramp the RAMDAC up and down continuously.
o Improved I/Q Rx Mode squelch operation.
o Added the ability to change the FS Error Tolerance (N1 and N2) using the
  $C3:Fxxx register, using the same format as P0.1. Note that using the
  recommended value (=2) may result in spurious false FS2 detects.
  If set to 1, this solves potential problems with FS2 false detects on
  test waveforms.
o Added mode "tx_level_adjust" using $C3=$2xxx. Use $2180 for default level.
  This allows the levels of the 4FSK symbols to be adjusted in both LD
  and I/Q modes.


Version 6.1.0.0
===============

o Add I/Q Rx and CMX994 interface.


Version 6.0.2.2
===============

o Framesync detection: improved reliability of FS2 detects.

o Framesync detection: the "silence frames" generated by a
  CMX6x8 vocoder with noise-gating enabled sometimes cause
  spurious FS2 (Sync Word only) detects, which may delay
  or prevent late entry into the call. These vocoder-data
  FS2 detects are now checked for and suppressed.


Version 6.0.2.1
===============

o Framesync detection: fixed an issue which occasionally caused
  unreliable FS1 (Preamble + Synchronisation Word) detects.
```

```
Version 6.0.2.0
===============

o SPI-CODEC mode: this function can now be controlled manually by
  the host during TX and RX operation. After setting bit #7 in the
  MODEM CONFIG register ($C7) to disable automatic vocoder support
  functions, bit #0 in the GAIN AND ROUTING REGISTER ($B1) can then
  be used to directly enable/disable the SPI-CODEC signal path at
  any time during TX or RX.

o Program Block P4.5 (Output 2 offset): fixed an issue causing
  output polarities to become inverted for some negative values
  of this parameter.


Version 6.0.1.0
===============

o Program Block P0.0: the default value for the Call Drop Threshold
  is now five consecutive corrupt frames, and the decision is based
  only on the Synchronisation Word received in each frame. This now
  correctly implements the Step-out Conditions in T-102 section 7.2.

o Program Block P0.2: this register now sets repeat counts for Start
  and End frames in TX mode. The CMX7141 will automatically re-send
  these frames the required number of times.

  In RX mode the CMX7141 will report all received Start frames but
  only the first valid End frame.

o Program Block P0.3: this register now sets the seed value used to
  initialise the whitening scrambler in both TX and RX.

o Framesync detection: bit #13 in the MODEM CONFIG register ($C7)
  now enables single Synchronisation Word detection using previous
  frame timing information, as specified by section 7.2 of T-102,
  condition (2)a(b). This is required in systems where timing is
  Base Station dependent, but not in Transmitting Station dependent
  systems or for direct communication between mobiles.

o Frame types: mixed TCH frame types (speech + control channel) are
  now supported in both TX and RX.

o SACCH transfers in RX: in version 6.0.0.0 the byte ordering of the
  received SACCH data fields in the RXDATA host transfer registers
  was accidentally swapped. This has now been corrected.


Version 6.0.0.0
===============

First alpha release after testing.
```

10 Application Notes

10.1 Simple Tx Configuration

Once the FI has been successfully loaded, the following sequence of C-BUS commands will produce a 4FSK PRBS signal at the MOD1 output pin:

C-BUS address	C-BUS Data	Comment
$C0	$0A40	Enable OP1, MOD1, Bias blocks
$B1	$0200	Route Output1 to MOD1
$B0	$7000	Set output gain to 0dB
$C1	$0032	Set modem to PRBS, Tx

10.2 Simple Rx Configuration

Once the FI has been successfully loaded, the following sequence of C-BUS commands will produce an “eye” diagram of the 4FSK signal presented on the ALT input at the MOD1 and MOD2 output pins:

C-BUS address	C-BUS Data	Comment
$C0	$9F40	Enable IP1, ALT, OP1, OP2, MOD1, MOD2, Bias blocks
$B1	$02A0	Route ALT to Input1, Output1 to MOD1, Output2 to MOD2
$B0	$7700	Set output gains to 0dB
$C1	$0031	Set modem to EYE, Rx

Infinite Capabilities . . .
FirmASIC®
. . . Maximum Flexibility

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		