19-4653; Rev 2; 12/10

EVALUATION KIT AVAILABLE

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

General Description

The MAX9670/MAX9671 dual SCART matrices route audio and video signals between a set-top box decoder chip and two external SCART connectors under I²C control. Operating from a 3.3V supply and a 12V supply, the MAX9670/MAX9671 consume 66mW during quiescent operation and 300mW during average operation when driving typical signals into typical loads. Video input detection, video load detection, and a 2.8mW standby mode facilitate the design of intelligent, low-power set-top boxes.

The MAX9670/MAX9671 audio section contains a buffered crosspoint to route audio inputs to audio outputs and programmable volume control from -62dB to 0dB in 2dB steps. The DirectDrive® output amplifiers create a $2V_{RMS}$ full-scale audio signal biased around ground, eliminating the need for bulky output capacitors and reducing click-and-pop noise. The zero-cross detection circuitry also further reduces clicks and pops by enabling audio sources to switch only during a zero-crossing. The MAX9671 offers TV left and right audio inputs.

The MAX9670/MAX9671 video section contains a buffered crosspoint to route video inputs to video outputs. The standard-definition video signals from the set-top box decoder chip are lowpass filtered to remove out-of-band artifacts.

The MAX9670/MAX9671 also support slow-switching and fast-switching signals. An interrupt signal from the MAX9670/MAX9671 informs the microcontroller when the system status has changed.

Applications

Set-Top Boxes

TVs

DVD Players

Typical Application Circuit appears at end of data sheet.

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

Features

- **66mW Quiescent Power Consumption**
- **2.8mW Standby Mode Consumption**
- **Programmable Audio Gain Control of -62dB to 0dB (TV Audio Outputs)**
- **Clickless, Popless, DirectDrive Audio**
- **Video Input and Video Load Detection**
- **Video Reconstruction Filter with 10MHz Passband and 52dB Attenuation at 27MHz**
- **3.3V and 12V Supply Voltages**

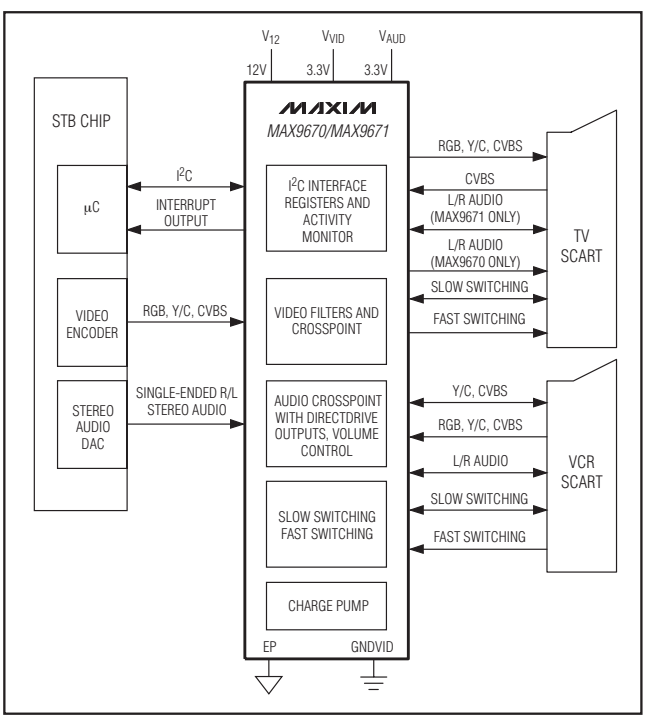
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TV R+L AUDIO INPUTS
MAX9670CTL+	0°C to +70°C	40 TQFN-EP*	No
MAX9671CTH+	0°C to +70°C	44 TQFN-EP*	Yes

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

System Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

ABSOLUTE MAXIMUM RATINGS

V_{VID} to GNDVID .....-0.3V to +4V
V_{12} to EP .....-0.3V to +14V
V_{AUD} to EP .....-0.3V to +4V
EP to GNDVID .....-0.1V to +0.1V
All Video Inputs, VCRIN_FS to GNDVID .....-0.3V to +4V
All Audio Inputs to EP .....-1V to (V_{EP} + 1V)
SDA, SCL, DEV_ADDR, $\overline{INT}$ to GNDVID .....-0.3V to +4V
TV_SS, VCR_SS to EP .....-0.3V to (V_{12} + 0.3V)
Current
  All Video/Audio Inputs .....±20mA
  C1P, C1N, CPVSS .....±50mA
Output Short-Circuit Current Duration
  Video and Fast-Switching Outputs to V_{VID}, GNDVID .....Continuous
  Audio Outputs to V_{AUD}, EP .....Continuous
  TV_SS, VCR_SS to V_{12}, EP .....Continuous
Continuous Power Dissipation (T_A = +70°C)
  40-Pin TQFN-EP (derate 26.3mW/°C above +70°C) ...2105.3mW
  44-Pin TQFN-EP (derate 26.3mW/°C above +70°C) ...2222.2mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
  40/44-pin TQFN-EP .....1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
  40/44-pin TQFN-EP .....27°C/W
Operating Temperature Range .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistance were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Video Supply Voltage Range	V_{VID}	Inferred from video PSRR test at 3V and 3.6V		3	3.3	3.6	V
Audio Supply Voltage Range	V_{AUD}	Inferred from audio PSRR test at 3V and 3.6V		3	3.3	3.6	V
V_{12} Supply Voltage Range	V_{12}	Inferred from slow-switching levels		11.4	12	12.6	V
V_{VID} Quiescent Supply Current	I_{VID_Q}	Normal operation; all video output amplifiers are enabled and muted (Note 3)			16	30	mA
		Standby mode, slow switch inputs low				1500	µA
		Shutdown				35	
V_{AUD} Quiescent Supply Current	I_{AUD_Q}	Normal operation (Note 3)			3.2	6	mA
		Shutdown				35	µA
V_{12} Quiescent Supply Current	I_{12_Q}	Normal operation (Note 3)	Slow-switching output set to low-level		0.3	100	µA
			Slow-switching output set to medium-level		475		
		Shutdown, T_A = +25°C				10	µA
VIDEO CHARACTERISTICS							
DC-COUPLED INPUT							
Input Voltage Range	V_{IN}	R_L = 75Ω to GNDVID or 150Ω to V_{VID}/2; inferred from gain test	V_{VID} = 3V		1.15		V_{P-P}
			V_{VID} = 3.135V			1.15	
			V_{VID} = 3.3V		1.3		
Input Current	I_{IN}	V_{IN} = 0.3V, T_A = +25°C			1	2	µA
Input Resistance	R_{IN}				300		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC-COUPLED INPUT						
Sync-Tip Clamp Level	V_{CLP}	Sync-tip clamp	-13	-4	+6	mV
Sync Crush		Sync-tip clamp; percentage reduction in sync pulse ($0.3V_{P-P}$); guaranteed by input clamping current measurement, T_A = +25°C			2	%
Input Clamping Current		Sync-tip clamp, V_{IN} = 0.3V, T_A = +25°C		1	2	µA
Maximum Input Source Resistance		Input sync-tip circuit must be stable even if the source resistance is as high as 300Ω		300		Ω
Input Voltage		Bias circuit	0.57	0.6	0.63	V
		High-impedance input circuit	0.3 x V_{VID}		0.36 x V_{VID}	
Input Resistance		Bias circuit		10		kΩ
		High-impedance input circuit		222		
DC CHARACTERISTICS						
DC Voltage Gain	A_V	Guaranteed by output voltage swing	1.95	2	2.05	V/V
DC Gain Mismatch Among R, G, and B Outputs		Guaranteed by output voltage swing of TV_R/C_OUT, TV_G_OUT, and TV_B_OUT; first input signal set is VCR_R/C_IN, VCR_G_IN, and VCR_B_IN; second signal set is ENC_R/C_IN, ENC_G_IN, and ENC_B_IN	-2		+2	%
Output Level		Sync-tip clamp (V_{IN} = V_{CLP})	0.1	0.30	0.51	V
		Bias circuit	1.3	1.5	1.78	
Output Voltage Swing		Sync-tip clamp, measured at output, V_{VID} = 3V, V_{IN} = V_{CLP} to (V_{CLP} +1.15V), R_L = 150Ω to V_{VID}/2, R_L = 75Ω to GNDVID		2.3		V_{P-P}
		Measured at output, V_{VID} = 3.135V, V_{IN} = V_{CLP} to (V_{CLP} + 1.15V), R_L = 150Ω to V_{VID}/2, R_L = 75Ω to GNDVID	2.243	2.3	2.358	
		Bias circuit, measured at output, V_{VID} = 3V, V_{IN} = (V_{BIAS} - 0.575V) to (V_{BIAS} + 0.575V), R_L = 150Ω to V_{VID}/2, R_L = 75Ω to GNDVID		2.3		
		Measured at output, V_{VID} = 3.135V, V_{IN} = (V_{BIAS} - 0.575V) to (V_{BIAS} + 0.575V), R_L = 150Ω to V_{VID}/2, R_L = 75Ω to GNDVID	2.243	2.3	2.358	
Output Short-Circuit Current				100		mA
Output Resistance	R_{OUT}			0.5		Ω
Output Leakage Current		Output disabled (load detection not active)			170	µA
Power-Supply Rejection Ratio		3V ≤ V_{VID} ≤ 3.6V	35			dB

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS							
Filter Passband Flatness		V_{OUT} = $2V_{P-P}$, f = 100kHz to 5.5MHz			-1		dB
Filter Attenuation		V_{OUT} = $2V_{P-P}$, attenuation is referred to 100kHz	f = 9.5MHz		3		dB
			f = 27MHz		40		
			f = 54MHz		55		
Slew Rate		V_{OUT} = $2V_{P-P}$, no filter in video path			60		V/µs
Settling Time		V_{OUT} = $2V_{P-P}$, settle to 0.1% (Note 4)			400		ns
Differential Gain	DG	5-step modulated staircase, f = 4.43MHz			0.15		%
Differential Phase	DP	5-step modulated staircase, f = 4.43MHz			0.5		Degrees
2T Pulse-to-Bar K Rating		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.3		K%
2T Pulse Response		2T = 200ns			0.2		K%
2T Bar Response		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.2		K%
Nonlinearity		5-step staircase			0.1		%
Group Delay Distortion		100kHz ≤ f ≤ 5MHz, outputs are $2V_{P-P}$			11		ns
Glitch Impulse Caused by Charge-Pump Switching		Measured at outputs			100		pV-s
Peak Signal to RMS Noise		100kHz ≤ f ≤ 5MHz			70		dB
Power-Supply Rejection Ratio		f = 100kHz, $100mV_{P-P}$			47		dB
Output Impedance		f = 5MHz			2		Ω
Video Crosstalk		f = 4.43MHz			-80		dB
Reverse Isolation		VCR SCART inputs to encoder inputs, full-power mode with VCR being looped through to TV, f = 4.43MHz			92		dB
Pulldown Resistance		Enable VCR_R/C_OUT pulldown through I^2C interface			4.4	7.5	Ω
AUDIO CHARACTERISTICS							
Voltage Gain		V_{IN} = -0.707V to +0.707V		3.95	4	4.05	V/V
Gain Mismatch		V_{IN} = -0.707V to +0.707V		-1.5		+1.5	%
Flatness		f = 20Hz to 20kHz, $0.25V_{RMS}$ input			0.006		dB
Frequency Bandwidth		$0.25V_{RMS}$ input, frequency where output is -3dB referenced to 1kHz			230		kHz
Capacitive Drive		No sustained oscillations; 75Ω series resistor on output			300		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance		V_{IN} = -0.707V to +0.707V		10		MΩ
Input Bias Current		V_{IN} = 0, T_A = +25°C			500	nA
Input Signal Amplitude		f = 1kHz, THD < 1%		0.5		V_{RMS}
Output DC Level		No input signal, V_{IN} grounded	-4		+4	mV
Power-Supply Rejection Ratio		DC	75	100		dB
		f = 1kHz		90		
Signal-to-Noise Ratio		f = 1kHz, 0.25V_{RMS} input, 20Hz to 20kHz		96		dB
Total Harmonic Distortion Plus Noise		R_L = 3.33kΩ, f = 1kHz, 0.25V_{RMS} input		0.002		%
		R_L = 3.33kΩ, f = 1kHz, 0.5V_{RMS} input		0.001		
Output Impedance		f = 1kHz		0.4		Ω
Volume Control Attenuation Step		Programmable gain to TV SCART volume control from -62dB to 0		2		dB
Volume Control Minimum Attenuation				0		dB
Volume Control Maximum Attenuation				62		dB
Mute Suppression		f = 1kHz, 0.25V_{RMS} input		110		dB
Audio Crosstalk		f = 1kHz, 0.25V_{RMS} input		100		dB
VIDEO-TO-AUDIO INTERACTION						
Crosstalk		Video input: f = 15kHz, 1V_{P-P} signal Audio input: f = 15kHz, 0.5V_{RMS} signal		92		dB
CHARGE PUMP						
Switching Frequency				570		kHz
FAST SWITCHING						
Input Low					0.4	V
Input High Level			1			V
Input Current		T_A = +25°C			10	µA
Output Low Voltage		I_{OL} = 0.5mA			0.1	V
Output High Voltage		I_{OH} = 0.5mA	V_{VID} - 0.1			V
Output Resistance				7		Ω
Rise Time		143Ω to GNDVID		12		ns
Fall Time		143Ω to GNDVID		10		ns
SLOW SWITCHING						
Input Low Voltage					2	V
Input Medium Voltage			4.5		7	V
Input High Voltage			9.5			V

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current				70	100	µA
Output Low Voltage		10kΩ to EP, 11.4V ≤ V_{12} ≤ 12.6V			1.5	V
Output Medium Voltage		10kΩ to EP, 11.4V ≤ V_{12} ≤ 12.6V	5		6.5	V
Output High Voltage		10kΩ to EP, 11.4V ≤ V_{12} ≤ 12.6V	10			V
DIGITAL INTERFACE						
Input High Voltage	V_{IH}		0.7 x V_{VID}			V
Input Low Voltage	V_{IL}				0.3 x V_{VID}	V
Input Hysteresis	V_{HYS}			0.06 x V_{VID}		V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-1		+1	µA
Input Capacitance				6		pF
Input Current		0.1V_{VID} < SDA < 3.3V, 0.1V_{VID} < SCL < 3.3V I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V+ is switched off, T_A = +25°C	-10		+10	µA
Output Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 5)	0		0.9	µs
Data Setup Time	$t_{HD, DAT}$		100			ns
Fall Time of SDA Transmitting	t_F	I_{SINK} ≤ 6mA, C_B = total capacitance of one bus line in pF, t_R and t_F measured between 0.3V_{VID} and 0.7V_{VID}		100		ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Pulse Width of Spike Suppressed	t_{SP}	Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns	0		50	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{12} = 12V, V_{VID} = V_{AUD} = 3.3V, V_{GNDVID} = V_{EP} = 0V, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

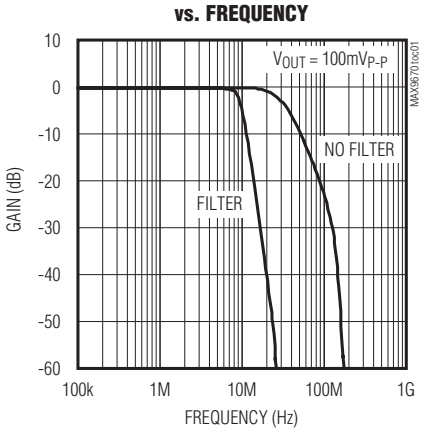
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OTHER DIGITAL I/O						
DEV_ADDR Low Level					0.3 x V_{VID}	V
DEV_ADDR High Level			0.7 x V_{VID}			V
DEV_ADDR Input Current		T_A = +25°C	-1		+1	µA
Interrupt Output Low Voltage		I_{OL} = 0.5mA			0.1	V
Interrupt Output Leakage Current		$\overline{INT}$ high impedance, T_A = +25°C			10	µA

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Normal operation mode is full power with input video and load detection active.
Note 4: The settling time is measured from the 50% of the input swing to the 0.1% of the final value of the output.
Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

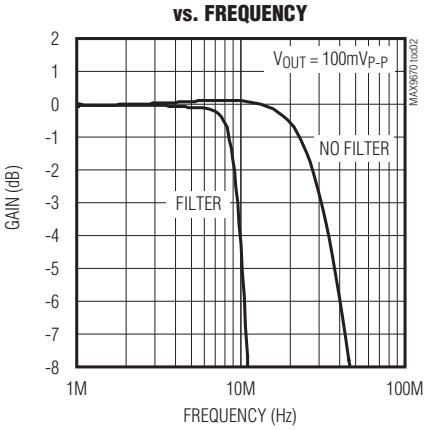
Typical Operating Characteristics

(V_{VID} = V_{AUD} = 3.3V, V_{12} = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

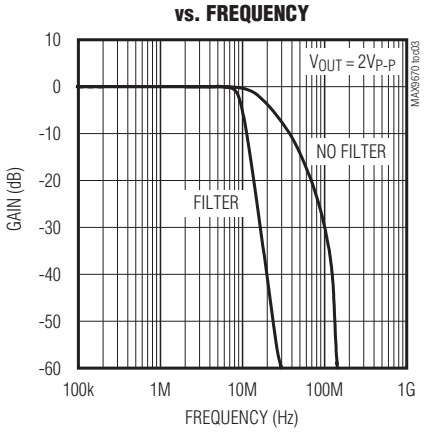
SMALL-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



LARGE-SIGNAL GAIN vs. FREQUENCY

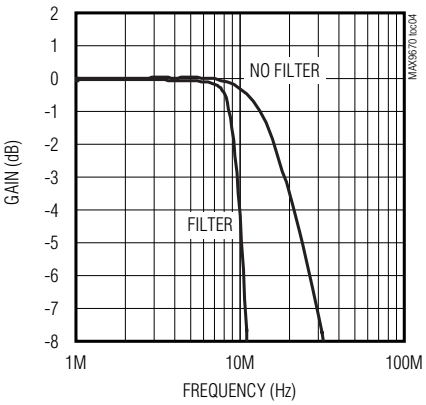


Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

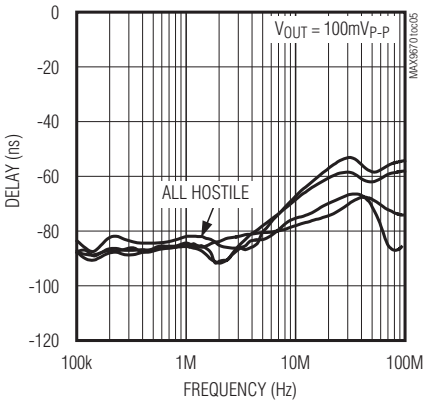
Typical Operating Characteristics (continued)

(V_{VID} = V_{AUD} = 3.3V, V_{12} = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

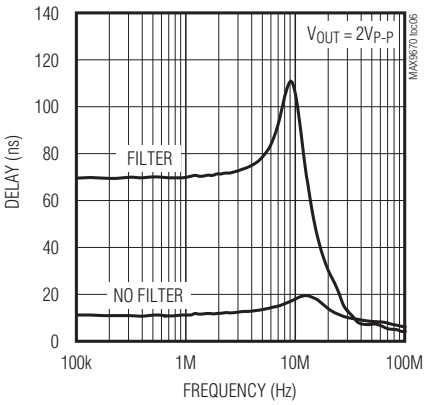
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



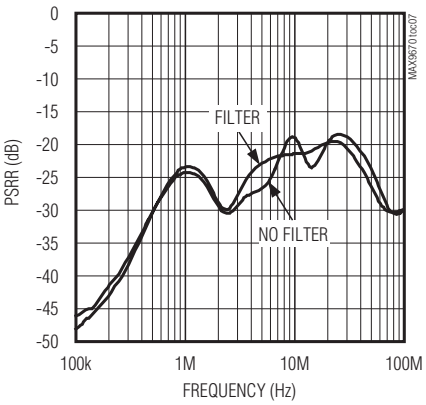
VIDEO CROSSTALK vs. FREQUENCY



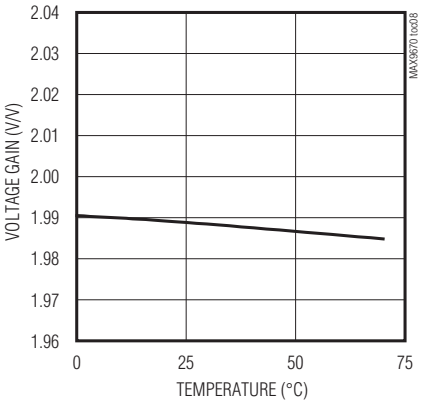
GROUP DELAY vs. FREQUENCY



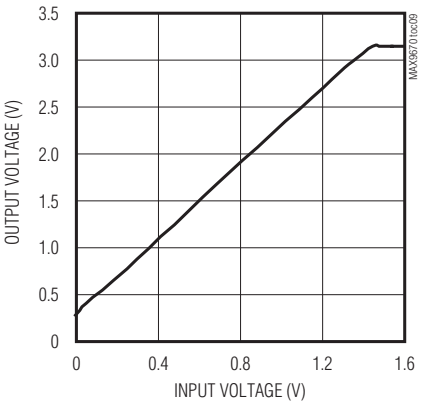
VIDEO POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



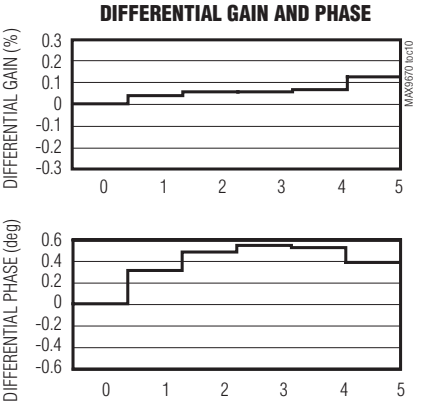
VIDEO VOLTAGE GAIN vs. TEMPERATURE



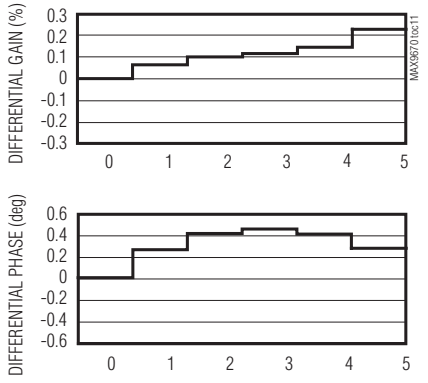
VIDEO OUTPUT VOLTAGE vs. INPUT VOLTAGE



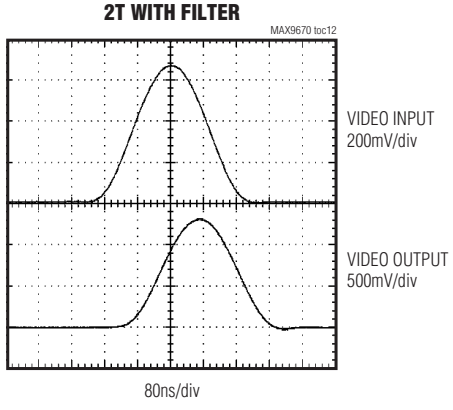
DIFFERENTIAL GAIN AND PHASE



DIFFERENTIAL GAIN AND PHASE



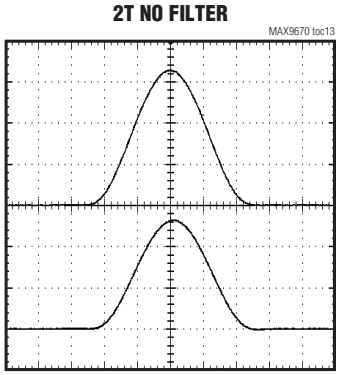
2T WITH FILTER



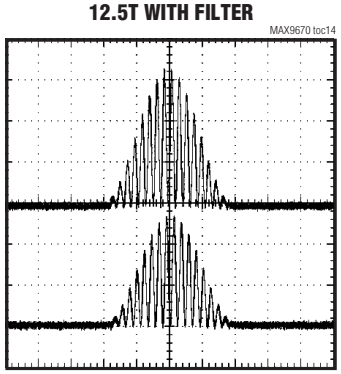
Typical Operating Characteristics (continued)

(V_{VID} = V_{AUD} = 3.3V, V_{12} = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

2T NO FILTER



12.5T WITH FILTER



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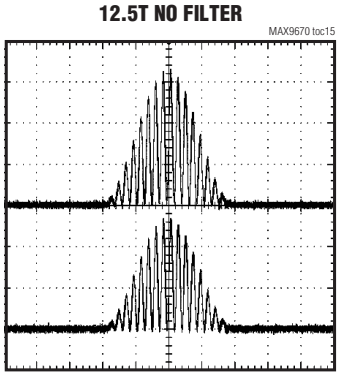
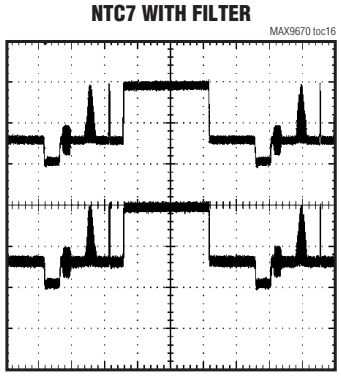


NTC7 WITH FILTER



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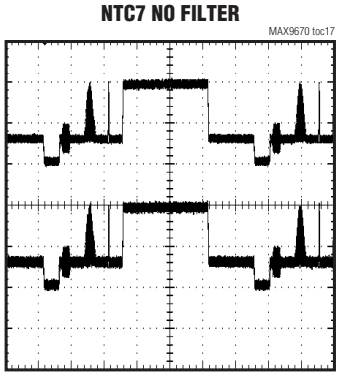
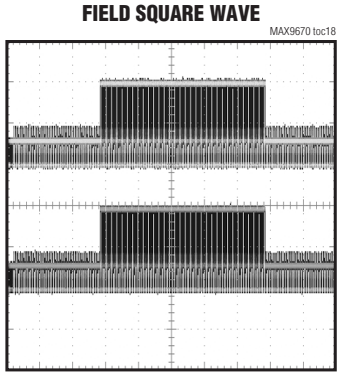


FIELD SQUARE WAVE

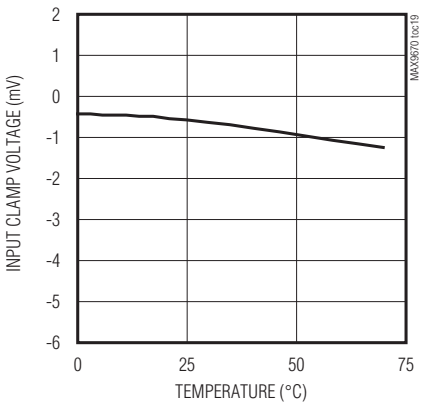


Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

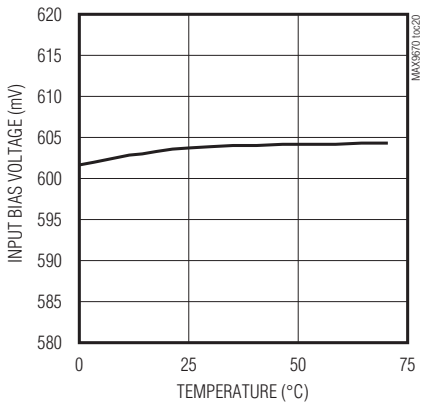
Typical Operating Characteristics (continued)

(V_{VID} = V_{AUD} = 3.3V, V_{12} = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

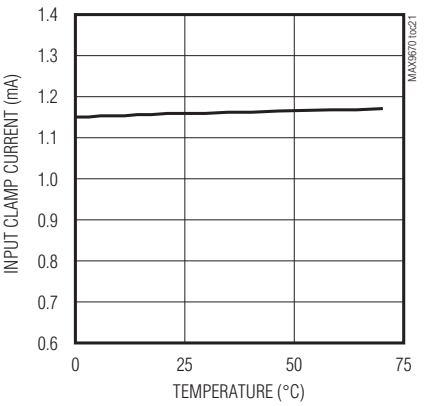
VIDEO INPUT SYNC-TIP CLAMP VOLTAGE vs. TEMPERATURE



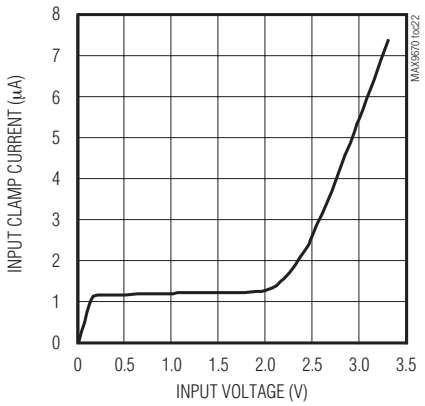
VIDEO INPUT BIAS VOLTAGE vs. TEMPERATURE



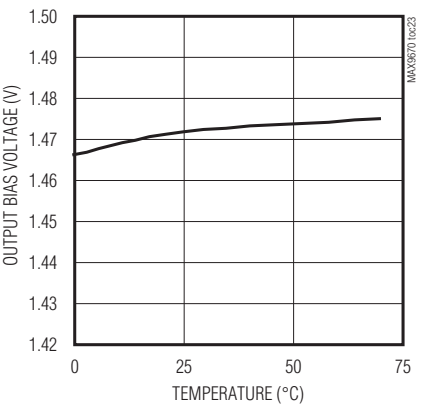
VIDEO INPUT SYNC-TIP CLAMP CURRENT vs. TEMPERATURE



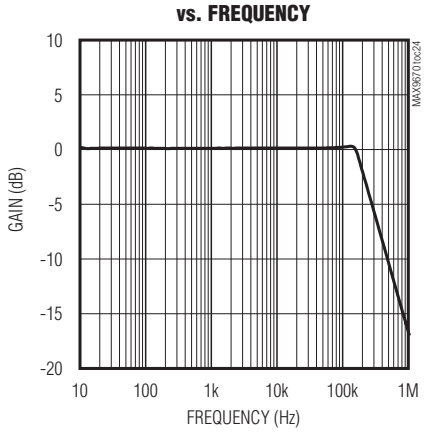
VIDEO INPUT SYNC-TIP CLAMP CURRENT vs. INPUT VOLTAGE



VIDEO OUTPUT BIAS VOLTAGE vs. TEMPERATURE



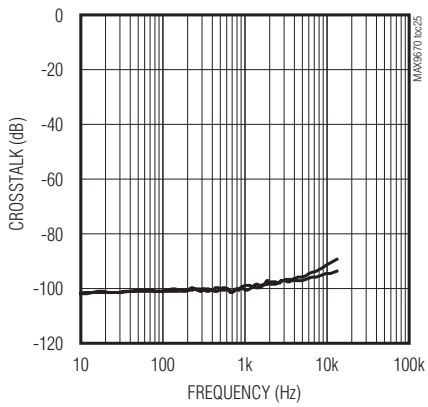
AUDIO LARGE-SIGNAL GAIN vs. FREQUENCY



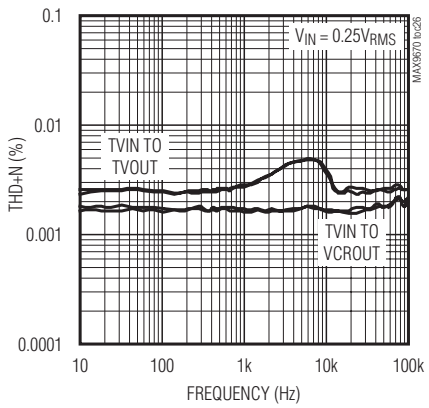
Typical Operating Characteristics (continued)

(V_{VID} = V_{AUD} = 3.3V, V_{12} = 12V, V_{GNDVID} = V_{EP} = 0V, video load is 150Ω to GNDVID, audio load is 10kΩ to EP, T_A = +25°C, unless otherwise noted.)

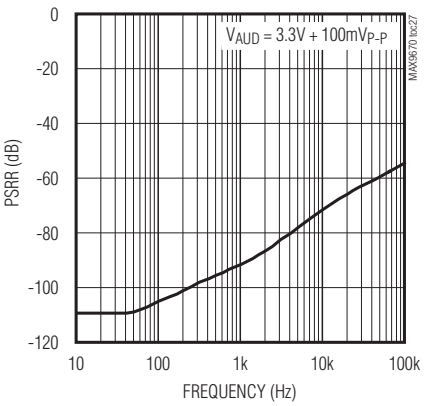
AUDIO CROSSTALK vs. FREQUENCY



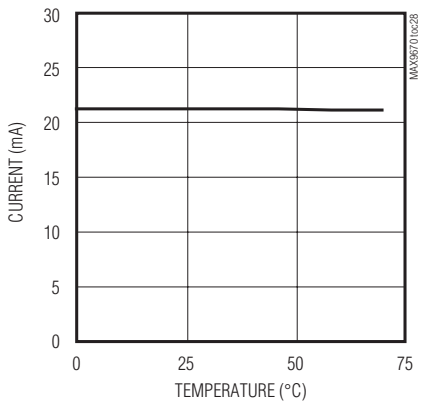
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



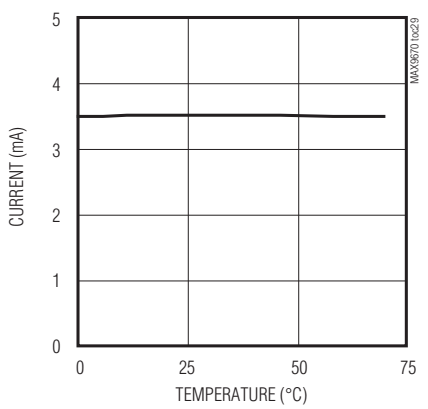
V_{AUD} POWER-SUPPLY REJECTION RATIO (INPUT REFERRED) vs. FREQUENCY



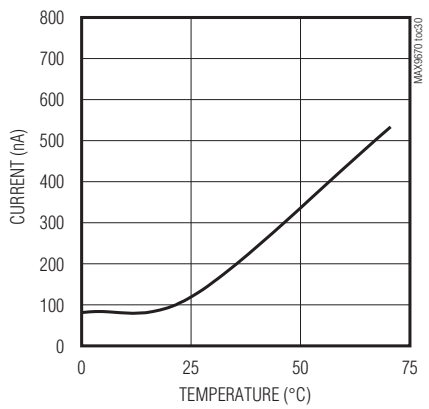
V_{VID} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



V_{AUD} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



V_{12} QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Pin Description

PIN		NAME	FUNCTION
MAX9670	MAX9671		
1	1	SDA	Bidirectional I^2C Data I/O. Output is open drain and tolerates up to 3.6V.
2	2	SCL	I^2C Clock Input
3	3	DEV_ADDR	Device Address Set Input. Connect to GNDVID, V_{VID}, SDA or SCL. See Table 3.
4	4	$\overline{INT}$	Interrupt Output. This is an open-drain output that pulls down to GNDVID to indicate a change in the VCR slow switching or fast switching input, the activity status of the composite video inputs, or the load status of the composite video outputs.
5	5	V_{AUD}	Audio Supply. Connect to a 3.3V supply. Bypass with a 10µF aluminum electrolytic capacitor and a 0.47µF ceramic capacitor to EP.
6	6	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 0.47µF capacitor from C1P to C1N.
7	7	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 0.47µF capacitor from C1P to C1N.
8	8	CPVSS	Charge-Pump Negative Power Supply. Bypass with a 1µF ceramic capacitor to EP.
9	9	ENC_INL	Encoder Left-Channel Audio Input
10	10	ENC_INR	Encoder Right-Channel Audio Input
—	11	TV_INL	TV SCART Left-Channel Audio Input
—	12	TV_INR	TV SCART Right-Channel Audio Input
11	13	VCR_INL	VCR SCART Left-Channel Audio Input
12	14	VCR_INR	VCR SCART Right-Channel Audio Input
13	15	TV_OUTL	TV SCART Left-Channel Audio Output
14	16	VCR_OUTL	VCR SCART Left-Channel Audio Output
15	17	VCR_OUTR	VCR SCART Right-Channel Audio Output
16	18	TV_OUTR	TV SCART Right-Channel Audio Output
17	19	TV_SS	TV SCART Bidirectional Slow-Switch Signal
18	20	V_{12}	+12V Supply for the Slow Switching Circuit. Bypass with a 10µF + 0.47µF ceramic capacitor to EP.
19	21	VCR_SS	VCR SCART Bidirectional Slow-Switch Signal
20	22	TVOUT_FS	TV SCART Fast-Switching Logic Output
—	23, 44	N.C.	No Connection. Leave unconnected.
21	24	VCRIN_FS	VCR SCART Fast-Switching Logic Input
22	25	ENC_B_IN	Encoder Blue Video Input
23	26	ENC_G_IN	Encoder Green Video Input
24	27	VCR_B_IN	VCR SCART Blue Video Input
25	28	VCR_G_IN	VCR SCART Green Video Input
26	29	TV_B_OUT	TV SCART Blue Video Output
27	30	TV_G_OUT	TV SCART Green Video Output

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9670	MAX9671		
28	31	GNDVID	Video Ground
29	32	VCR_R/C_IN	VCR SCART Red/Chroma Video Input
30	33	V_{VID}	Video and Digital Supply. Connect to a 3.3V supply. Bypass with parallel 1µF and 0.1µF ceramic capacitors to GNDVID. V_{VID} also serves as a digital supply for the I^2C interface.
31	34	ENC_C_IN	Encoder Chroma Video Input
32	35	ENC_R/C_IN	Encoder Red/Chroma Video Input
33	36	TV_R/C_OUT	TV SCART Red/Chroma Video Output
34	37	VCR_R/C_OUT	VCR SCART Red/Chroma Video Output
35	38	VCR_Y/CVBS_OUT	VCR SCART Luma/Composite Video Output
36	39	TV_Y/CVBS_OUT	TV SCART Luma/Composite Video Output
37	40	VCR_Y/CVBS_IN	VCR SCART Luma/Composite Video Input
38	41	TV_Y/CVBS_IN	TV SCART Luma/Composite Video Input
39	42	ENC_Y_IN	Encoder Luma Video Input
40	43	ENC_Y/CVBS_IN	Encoder Luma/Composite Video Input
—	—	EP	Exposed Pad. The exposed pad is the internal ground for the audio amplifiers and charge pump. A low-impedance connection between ground and EP is required for proper isolation.

Detailed Description

The MAX9670/MAX9671 represents Maxim's third generation of SCART audio/video (A/V) switches. Under I^2C control, these devices route audio, video, and control information between the set-top box decoder chip and two SCART connectors. The audio signals are left audio and right audio. The video signals are composite video with blanking and sync (CVBS) and component video (red, green, blue). S-video (Y/C) can be transported across the SCART interface if CVBS is reassigned to luma (Y) and red is reassigned to chroma (C). Support for S-video is optional. The slow-switch signal and the fast-switch signal carry control information. The slow-switch signal is a 12V, three-level signal that indicates whether the picture aspect ratio is 4:3 or 16:9 or causes the television to use an internal A/V source such as an antenna. The fast-switch signal indicates whether the television should display CVBS or RGB signals.

CVBS, left audio, and right audio are full duplex. All the other signals are half duplex. Therefore, one device on the link must be designated as the transmitter, and the other device must be designated as the receiver.

The low power consumption and the advanced monitoring functions of the MAX9670/MAX9671 enable the creation of lower power set-top boxes, televisions, and DVD players. Unlike competing SCART ICs, the audio and video circuits of the MAX9670/MAX9671 operate entirely from 3.3V rather than from 5V and 12V. Only the slow-switch circuit of the MAX9670/MAX9671 requires a 12V supply. The MAX9670/MAX9671 also have circuits that detect activity on the CVBS inputs, loads on the CVBS outputs, and the level of the slow-switch signals. The $\overline{INT}$ signal informs the microcontroller if there are any changes so that the microcontroller can intelligently decide whether to power up or power down the equipment.

In addition, the MAX9670/MAX9671 have DirectDrive audio circuitry to eliminate click-and-pop noise. With DirectDrive, the DC bias of the audio line outputs is always at ground, no matter whether the MAX9670/MAX9671 are being powered up or powered down. Conventional audio line output drivers that operate from a single supply require series AC-coupling capacitors. During power-up, the DC bias on the AC-coupling capacitor moves from ground to a positive voltage, and during power-down, the opposite occurs. The changing DC bias usually causes an audible transient.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

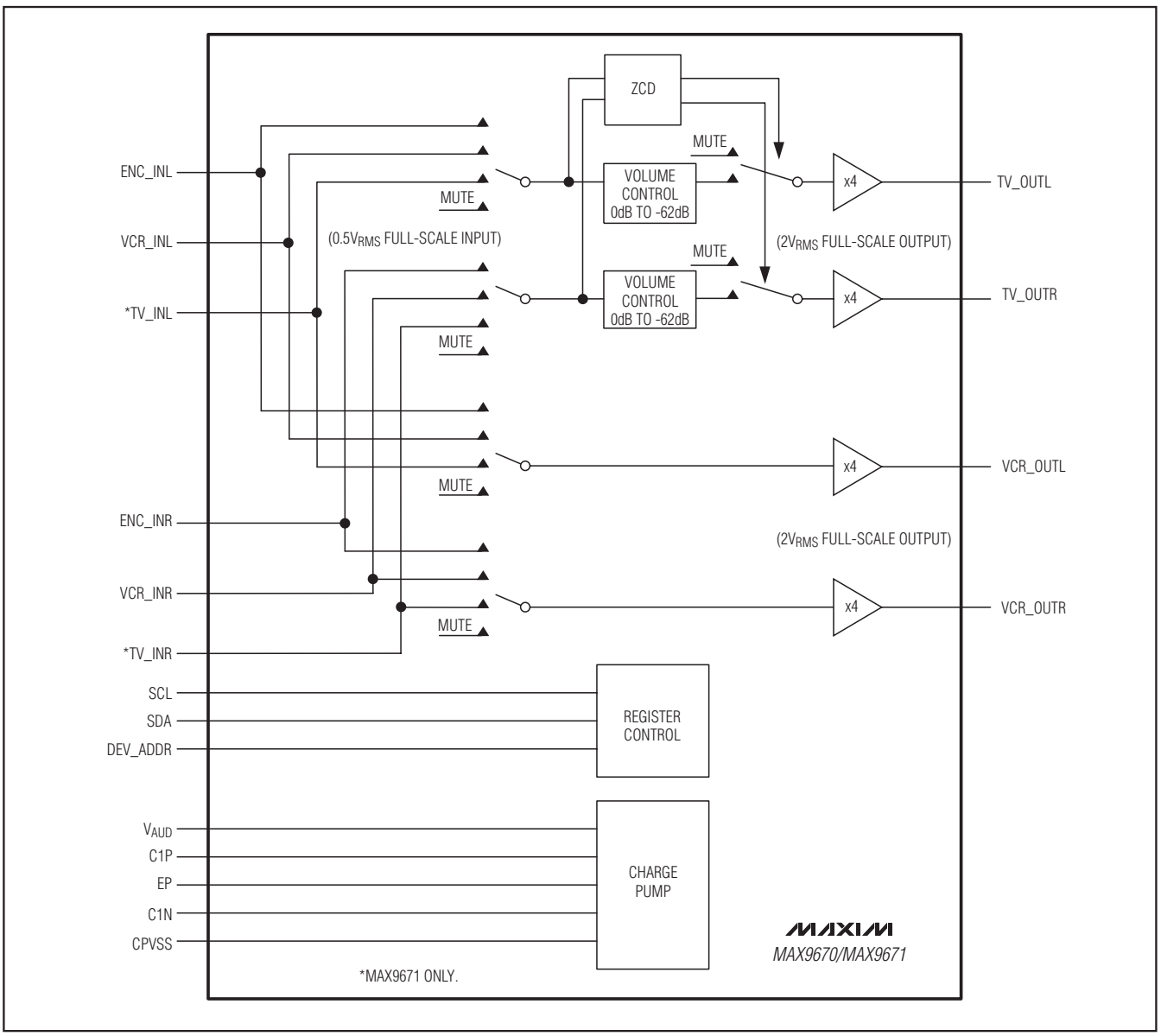


Figure 1. MAX9670/MAX9671 Audio Section Functional Diagram

Audio Section

The MAX9670 audio circuit is essentially a stereo, 2-by-2, nonblocking, audio crosspoint with output drivers. The encoder (stereo audio DAC) and the VCR are the two input sources, and the two outputs go to the TV SCART connector and the VCR SCART connector. See Figure 1. The MAX9671 audio circuit is similar to that of the MAX9670 except that it is a stereo, 3-by-2, nonblocking audio crosspoint with TV as the third input source.

The integrated charge pump inverts the +3.3V supply to create a -3.3V supply. The audio circuit operates from bipolar supplies so the audio signal is always biased to ground.

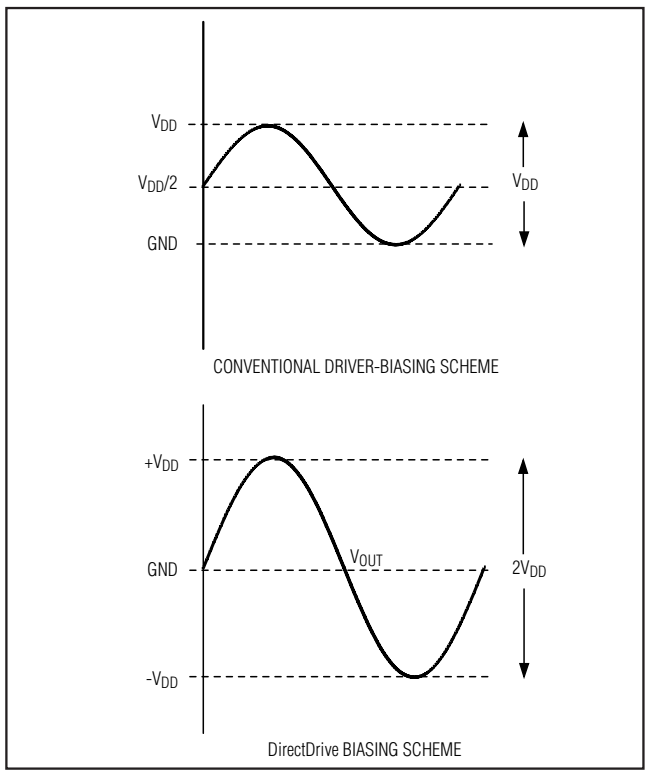


Figure 2. Conventional Driver Output Waveform vs. MAX9670/ MAX9671 Output Waveform.

Clickless Switching

The TV audio channel incorporates a zero-crossing detect (ZCD) circuit that minimizes click noise due to abrupt signal level changes that occur when switching between audio signals at an arbitrary moment.

To implement the zero-crossing function when switching audio signals, set the ZCD bit high (Audio Control register 00h, bit 6). Then set the mute bit high (Audio Control register 00h, bit 0). Next, wait for a sufficient period of time for the audio signal to cross zero. This period is a function of the audio signal path's low-frequency 3dB corner (f_{L3dB}). Thus, if f_{L3dB} = 20Hz, the time period to wait for a zero-crossing detect is 1/20Hz or 50ms.

After the wait period, select a new audio source for the TV audio channel by writing to bits 1 and 0 of TV Audio Control register (01h). Finally, clear mute (Audio Control register, 00h, bit 0), but leave ZCD (Audio Control register 00h, bit 6) high. The MAX9670/MAX9671 switches the signal out of mute at the next zero crossing. See Tables 12 and 13.

Audio Outputs

The MAX9670/MAX9671 audio output amplifiers feature Maxim's DirectDrive architecture, thereby eliminating the need for output-coupling capacitors required by conventional single-supply audio line drivers. An internal charge pump inverts the positive supply (V_{AUD}), creating a negative supply (CPVSS). The audio output amplifiers operate from these bipolar supplies with their outputs biased about audio ground (Figure 2). The benefit of this audio ground bias is that the amplifier outputs do not have a DC component. The DC-blocking capacitors required with conventional audio line drivers are unnecessary, conserving board space, reducing system cost, and improving frequency response.

Conventional single-supply audio line drivers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias. Clicks and pops are created when the coupling capacitors are charged during power-up and discharged during power-down.

The MAX9670/MAX9671 features a low-noise charge pump that requires only two small ceramic capacitors. The 580kHz switching frequency is well beyond the audio range and does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients.

The SCART standard specifies $2V_{RMS}$ as the full-scale for audio signals. As the audio circuits process $0.5V_{RMS}$ full-scale audio signals internal to the MAX9670/MAX9671, the gain-of-4 output amplifiers restore the audio signals to a full-scale of $2V_{RMS}$.

To select which audio input source is routed to the TV SCART connector, write to bits 1 and 0 of the TV Audio Control register (01h). To select which audio input source is routed to the VCR SCART connector, write to bits 3 and 2 of the TV Audio Control register (01h). The power-on default is for the TV and VCR audio outputs to be muted (the inputs of the output amplifiers are connected to audio ground). See Tables 10 and 13.

Volume Control

Volume control is programmable from -62dB to 0dB in 2dB steps through I^2C interface. The block consists of a resistive ladder network to generate 31 2dB volume control steps, a unity gain buffer to isolate the input from the resistive ladder, switches (MPLx and MNLx) that select 1 of 32 nodes on the resistive ladder, and logic to decode the the I^2C volume control value. See Table 12.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

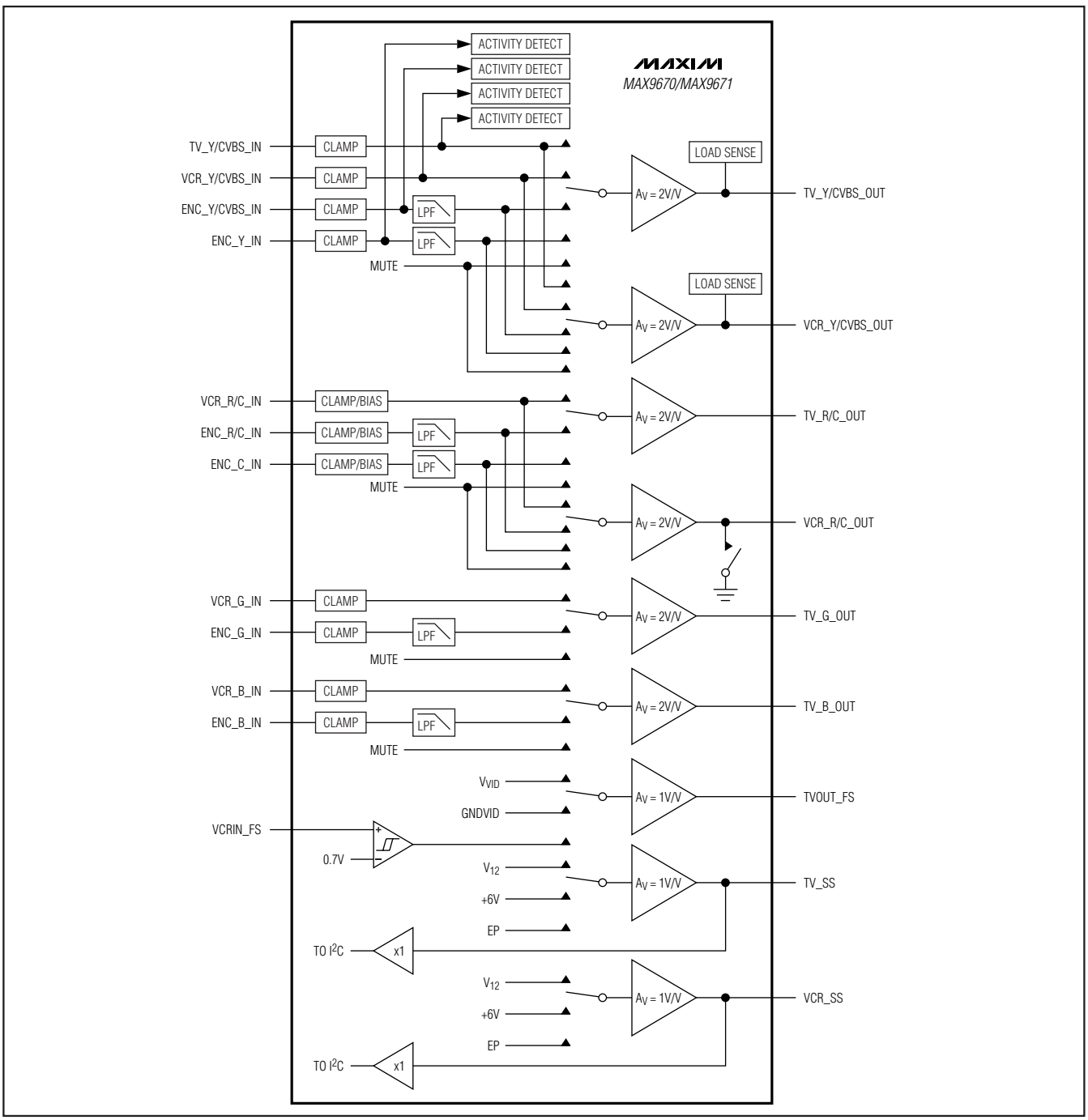


Figure 3. MAX9670/MAX9671 Video Section Function Diagram

Video Section

The video circuit routes different video formats between the set-top box decoder, the TV SCART connector, and the VCR SCART connector. It also routes slow-switch and fast-switch control information. See Figure 3.

Video Inputs

Whether the incoming video signal is AC-coupled or DC-coupled into the MAX9670/MAX9671 depends upon the origin, format, and voltage range of the video signal. Table 1 below shows the recommended connections. Always AC-couple an external video signal through a 0.1µF capacitor because its voltage is not well defined (see the *Typical Application Circuit*). For example, the video transmitter circuit might have a different ground than the video receiver, thereby level shifting the DC bias. 60Hz power line hum might cause the video signal to change DC bias slowly.

Internal video signals that are between 0 and 1V can be DC-coupled. Most video DACs generate video signals between 0 and 1V because the video DAC sources current into a ground-referenced resistor. For the minority of video DACs that generate video signals between 2.3V and 3.3V because the video DAC sinks current from a V_{VID}-referenced resistor, AC-couple the video signal to the MAX9670/MAX9671.

The MAX9670/MAX9671 restore the DC level of incoming, AC-coupled video signals with either transparent sync-tip clamps or bias circuits. When using an AC-coupled input, the transparent sync-tip clamp automatically clamps the input signal minimum to ground, preventing it from going lower. A small current of 1µA pulls down on the input to prevent an AC-coupled signal from drifting outside the input range of the part. Use sync-tip clamps with CVBS, RGB, and luma signals.

The transparent sync-tip clamp is transparent when the incoming video signal is DC-coupled and at or above ground. Under such conditions, the clamp never activates. Therefore, the outputs of video DACs that generate signals between 0 and 1V can be directly connected to the MAX9670/MAX9671 inputs.

The bias circuit accepts AC-coupled chroma, which is a subcarrier with the color information modulated onto it. The bias voltage of the bias circuits is around 600mV.

ENC_R/C_IN and VCR_R/C_IN can receive either a red video signal or a chroma video signal. Set the input configuration by writing to bits 7 and 3 of the VCR Video Input Control register (08h). See Tables 10 and 16.

The MAX9670/MAX9671 also have video input detection. When activated, activity detect circuits check if sync is present on incoming CVBS and luma (Y) signals. If so, then there is a valid video signal. Read bits 0, 2, 4, and 5 of the Video Activity Status register (0Fh) to determine the status of the CVBS and luma (Y) inputs. See Table 21.

In high-impedance mode, the inputs to the MAX9670/MAX9671 do not distort the video signal in case the outputs of the video DAC are also connected to another video circuit such as a high-definition video filter amplifier. See the *SCART Set-Top Box with Analog HD Outputs* section. The inputs in high-impedance mode are biased at $V_{VID}/3$, which is sufficiently above ground so that the ESD diodes never forward biases as the video signal changes. The input resistance is 222kΩ, which presents negligible loading on the video current DAC.

Video Reconstruction Filter

The video DAC outputs of the set-top box decoder chip need to be lowpass-filtered to reject the out-of-band noise. The MAX9670/MAX9671 integrate sixth-order, Butterworth filters. The filter passband (±1dB) is typically 5.5MHz, and the attenuation at 27MHz is 52dB. The filters are suited for standard-definition video.

Video Outputs

The video output amplifiers can both source and sink load current, allowing output loads to be DC- or AC-coupled. The amplifier output stage needs around 300mV of headroom from either supply rail. For video signals with a sync pulse, the sync tip is typically at 300mV, as shown in Figure 4. For a chroma signal, the blank level is typically at 1.5V, as shown in Figure 5.

If the supply voltage is greater than 3.135V (5% below a 3.3V supply), each amplifier can drive two DC-coupled video loads to ground. If the supply is less than 3.135V, each amplifier can drive only one DC-coupled or AC-coupled video load.

The SCART standard allows for video signals to have a superimposed DC component within 0 and 2V. Therefore, most video signals are DC-coupled at the output. In the unlikely event that the video signal needs to be AC-coupled, the coupling capacitors should be 220µF or greater to keep the highpass filter formed by the 37.5Ω equivalent resistance of the video transmission line to a corner frequency of 4.8Hz or below to keep it well below the 25Hz frame rate of the PAL standard.

The CVBS outputs have load sense circuits. If enabled, each load sense circuit checks for a load eight times per second by connecting an internal 15kΩ pullup resistor to the output for 1ms. If the output is pulled up, no load is present. If the output stays low, a load is connected. Read bits 1 and 3 of the Video Activity Status register (0Fh) to determine load status. See Table 21.

The selection of video sources that are sent to the TV SCART connector are controlled by bits 0 to 4 of the TV Video Input Control register (06h) while the selection of

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

video sources that are sent to the VCR SCART connector are controlled by bits 0 to 2 of the VCR Video Input Control register (08h). See Tables 10, 14, and 16. The video outputs can be enabled or disabled by bits 2 through 7 of the Output Enable register (0Dh). See Table 18.

Slow Switching

The MAX9670/MAX9671 support the IEC 933-1, Amendment 1, three-level slow switching that selects the aspect ratio for the display (TV). Under I²C control, the MAX9670/MAX9671 set the slow-switching output voltage level. Table 2 shows the valid input levels of the slow-switching signal and the corresponding operating modes of the display device.

Two bidirectional ports are available for slow-switching signals for the TV and VCR. The slow-switching input status is continuously read and stored in the Status register (0Eh). The slow-switching outputs can be set to a logic level or high impedance by writing to the TV Video Output Control register (07h) and the VCR Video Output Control register (09h). When enabled, $\overline{INT}$ becomes active low if the voltage level changes on TV_SS or VCR_SS. See Tables 10, 15, 17, and 20.

Fast Switching

The fast-switching signal was originally used to switch between CVBS and RGB signals on a pixel-by-pixel basis so that on-screen display (OSD) information could be inserted. Since modern set-top box decoder chips have integrated OSD circuitry, there is no need to create OSD information using the older technique. Now, the fast-switching signal is just used to switch between CVBS and RGB signal sources.

Set the source of the fast-switching signal by writing to bits 4 and 3 of the TV Video Output Control register (07h). The fast-switching signal to the TV SCART connector can be enabled or disabled by bit 1 of the Output Enable register (0Dh). See Tables 10, 15, and 18.

I²C Serial Interface

The MAX9670/MAX9671 feature an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9670/MAX9671 and the master at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9670/MAX9671 by transmitting a START (S) condition, the proper slave address with the R/$\overline{W}$ bit set to 0, followed by the register address and then the data word. Each transmit sequence is framed by a START and a STOP (P) condition. Each word transmitted to the MAX9670/MAX9671 is 8 bits long and is followed by an acknowledge clock pulse. A master reads from the MAX9670/MAX9671 by transmitting the slave address with the R/$\overline{W}$ bit set to 0, the register address of the register to be read, a REPEATED START (Sr) condition, the slave address with the R/$\overline{W}$ bit set to 1, followed by a series of SCL pulses. The MAX9670/MAX9671 transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or

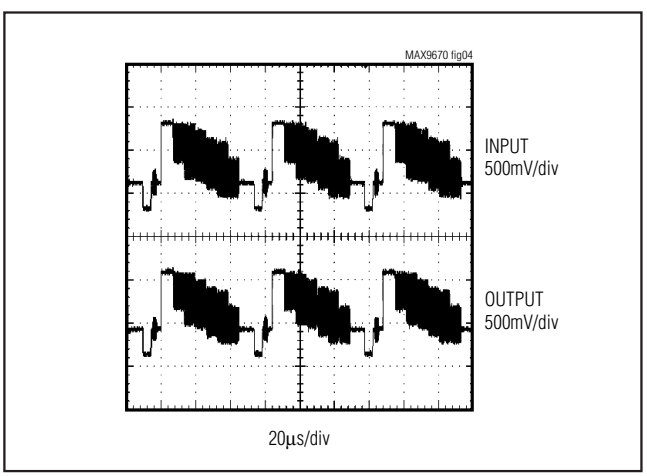


Figure 4. MAX9670/MAX9671 Video Output with CVBS Signal, Multiburst Video Test Signal Shown

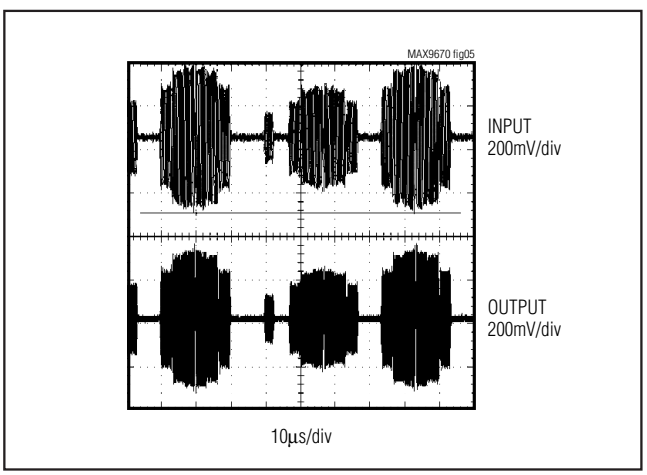


Figure 5. MAX9670/MAX9671 Video Output with Chroma (C) Signal, Multiburst Video Test Signal Shown

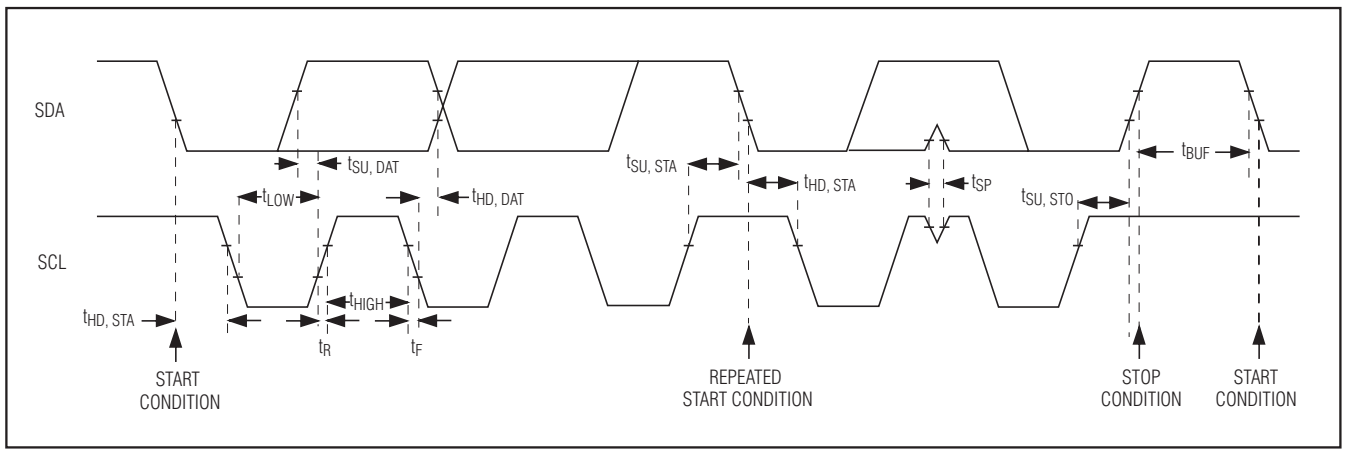


Figure 6. I²C Serial-Interface Timing Diagram

REPEATED START condition, an acknowledge or a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9670/MAX9671 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 7). A START condition from the master signals the beginning of a transmission to the MAX9670/MAX9671. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

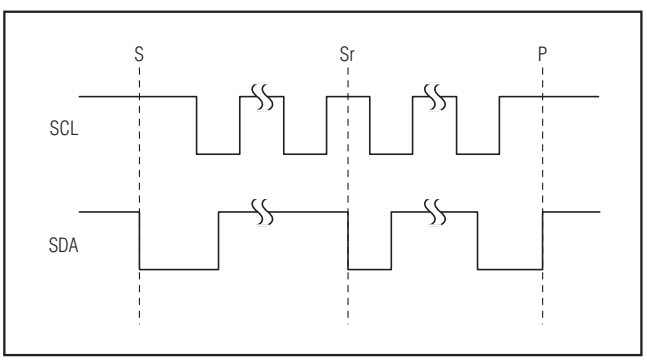


Figure 7. START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX9670/MAX9671 recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/$\overline{W}$) bit. Set the R/$\overline{W}$ bit to 1 to configure the MAX9670/MAX9671 to read mode. Set the R/$\overline{W}$ bit to 0 to configure the MAX9670/MAX9671 to write mode. The slave address is always the first byte of information sent to the MAX9670/MAX9671 after a START or a REPEATED START condition. The MAX9670/MAX9671 slave address is configurable with DEV_ADDR. Table 3 shows the possible slave addresses for the MAX9670/MAX9671.

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Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9670/MAX9671 use to handshake receipt of each byte of data when in write mode (see Figure 8). The MAX9670/MAX9671 pull down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9670/MAX9671 are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9670/MAX9671, followed by a STOP condition.

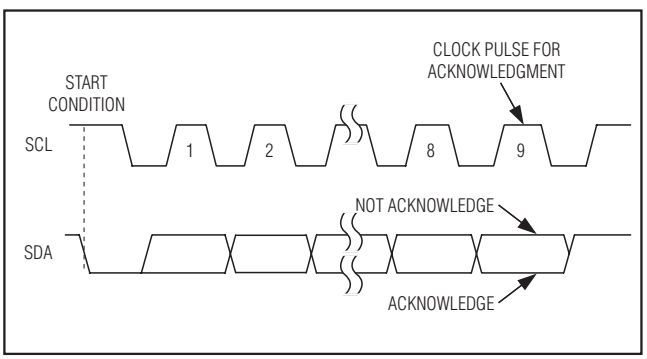

Figure 8. Acknowledge

Write Data Format

A write to the MAX9670/MAX9671 consists of transmitting a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one data byte to configure the internal register address pointer, one or more data bytes, and a STOP condition. Figure 9 illustrates the proper frame format for writing one byte of data to the MAX9670/MAX9671. Figure 10 illustrates the frame format for writing n bytes of data to the MAX9670/MAX9671.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9670/MAX9671. The MAX9670/MAX9671 acknowledge receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9670/MAX9671's internal register address pointer. The pointer tells the MAX9670/MAX9671 where to write the next byte of data. An acknowledge pulse is sent by the MAX9670/MAX9671 upon receipt of the address pointer data.

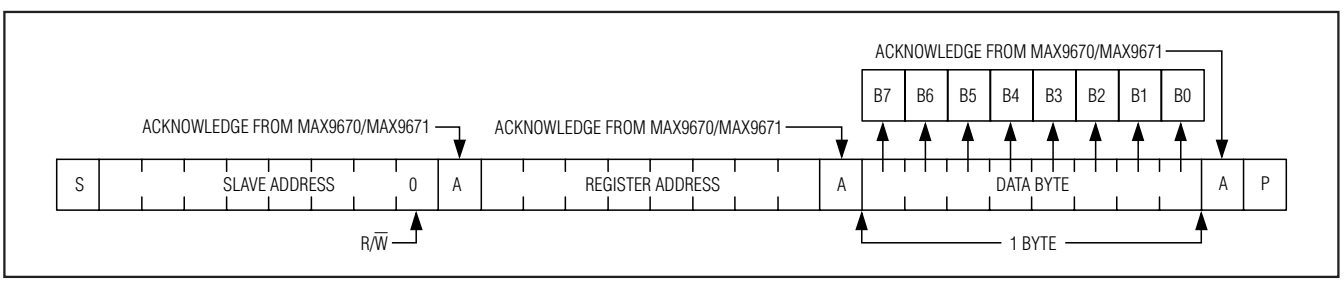

Figure 9. Writing a Byte of Data to the MAX9670/MAX9671

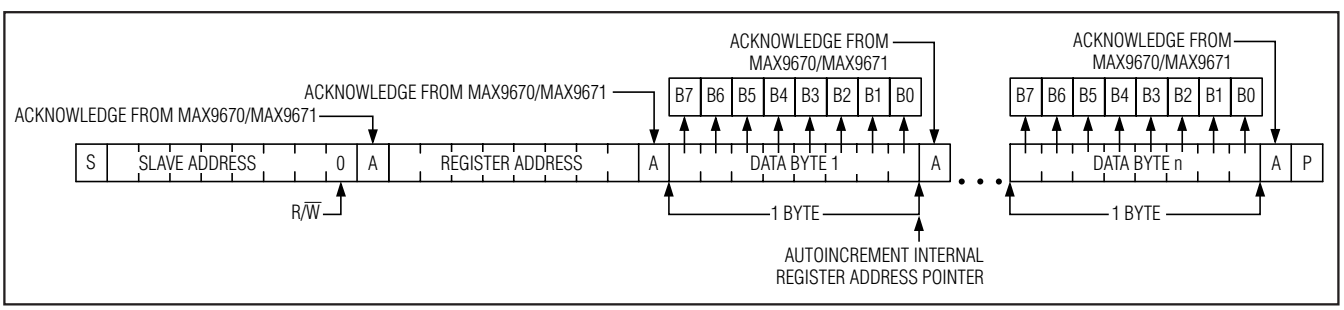

Figure 10. Writing n Bytes of Data to the MAX9670/MAX9671

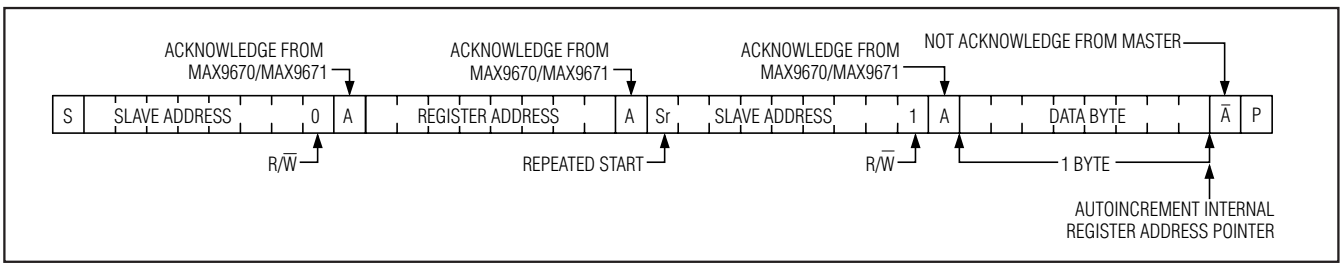

Figure 11. Reading One Indexed Byte of Data from the MAX9670/MAX9671

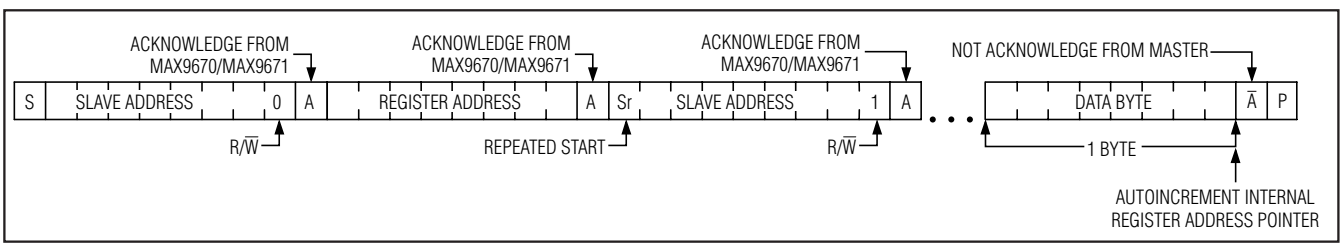

Figure 12. Reading n Bytes of Indexed Data from the MAX9670/MAX9671

The third byte sent to the MAX9670/MAX9671 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9670/MAX9671 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer by first sending the MAX9670/MAX9671's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address after a START condition. The MAX9670/MAX9671 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9670/MAX9671 transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from the register address location set by the previous transaction and not 00h and subsequent reads autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than 10h results in repeated reads from a dummy register containing FFh data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 11 and 12 illustrate the frame format for reading data from the MAX9670/MAX9671.

Interrupt Output

When interrupt is enabled in modes 1 and 2, $\overline{INT}$, which is an open-drain output, pulls low under the following conditions: slow-switch signals change value, CVBS input signals are detected or disappear, and CVBS output loads are added or removed.

When interrupt is enabled in mode 3, $\overline{INT}$ pulls low only when the slow-switch signal changes value.

Enable $\overline{INT}$ by writing a 1 into bit 4 of register 01h. See Table 13.

The interrupt can be cleared by reading register 0Eh and 0Fh.

Applications Information

Audio Inputs

The maximum full-scale audio signal that can be applied to the audio inputs is $0.5V_{RMS}$ biased at ground. The recommended application circuit to attenuate and bias an incoming audio signal is shown in Figure 13.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

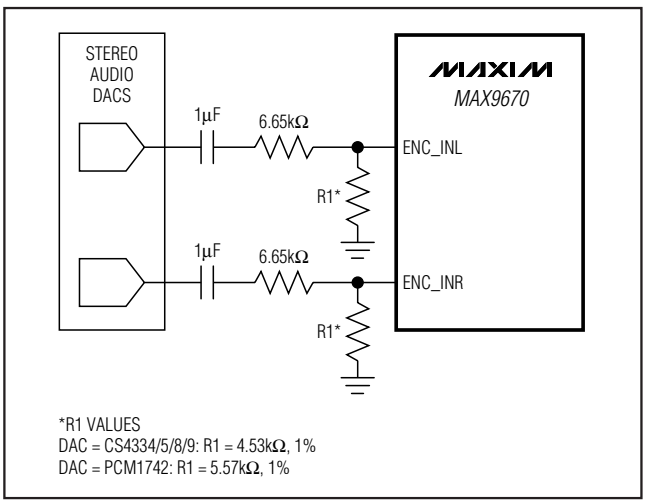

Figure 13. Application circuit to connect audio source to audio inputs. The 1µF capacitor connected to the ground-referenced resistors biases the audio signal at ground. The resistors attenuate the audio signal.

The audio path has a gain of 4V/V so that the full scale of the audio output signal is $2V_{RMS}$. If less than $2V_{RMS}$, full scale is desired at the audio outputs, and the full scale of the audio input signal should be proportionately decreased below $0.5V_{RMS}$.

Operating Modes

The MAX9670/MAX9671 has four operating modes, which can be set by writing to bits 6 and 7 of register 10h. See Table 19.

Shutdown

All circuitry is shutdown in the MAX9670/MAX9671 except for the I²C interface, which is designed with static CMOS logic. Except for register 10h, which sets the operating mode, the values in all of the other I²C registers are preserved while entering, during, and leaving shutdown mode.

Standby Mode

In standby mode, the MAX9670/MAX9671 monitor the slow-switch signals and decide whether to loop through the audio/video signals. If the VCR slow switch input has activity (6V or 12V at the input), the audio/video signals are looped through from the VCR SCART to the TV SCART. If the TV slow-switch input has activity, the audio/video signals are looped through from the TV SCART to the VCR SCART. If neither the VCR slow-switch input nor the TV slow switch input show activity, i.e., both inputs are at ground, no signals are looped through. If both the VCR slow-switch input and the TV slow-switch input have activity, the MAX9670/MAX9671 considers this condition to be illegal and does not loop through any signals.

A finite state machine (Figure 14) controls the operation of the MAX9670/MAX9671. State 0 is always the initial state when the MAX9670/MAX9671 enter standby mode. Table 4 shows the values of the I²C registers in state 0. The state machine sets the other I²C registers to the correct values to loop through the audio/video signals in states 1 and 2 (see Tables 5 and 6). When the MAX9670/MAX9671 leaves standby mode, the values in all of the I²C registers except register 10h are preserved so that the operation is not disturbed. For example, if in standby mode, the MAX9670 is looping through the audio/video signals from VCR SCART to TV SCART, and if the microcontroller changes the operating mode from standby mode to full-power mode, the audio/video signals continue to be looped through during and after the mode change. The user does not experience any disruption in audio or video service.

The microcontroller can be turned off in standby mode because the MAX9670/MAX9671 operate autonomously. Upon power-up, the default operating mode is standby mode.

Full-Power Mode with Video Input Detection and Video Load Detection

In this mode, the MAX9670/MAX9671 are fully on. If interrupt is enabled, $\overline{INT}$ goes active low whenever the slow-switch signal changes; a CVBS signal appears or disappears; or a CVBS load appears or disappears. The microcontroller can decide whether to change the routing configuration or operating mode of the MAX9670/MAX9671.

Full-Power Mode Without Video Input Detection and Video Load Detection

This mode is similar to the above mode except that video input detection and video load detection are not active. If interrupt is enabled, $\overline{INT}$ goes active low only when the slow-switch signal changes.

Power Consumption

The quiescent power consumption and average power consumption of the MAX9670/MAX9671 are very low because of 3.3V operation and low-power circuit design. Quiescent power consumption is defined when the MAX9670/MAX9671 are operating without loads and without any audio or video signals. Table 7 shows the quiescent power consumption in all 4 operating modes.

Average power consumption is defined when the MAX9670/MAX9671 drives typical signals into typical loads. Table 8 shows the average power consumption in full-power mode and Table 9 shows the input and output conditions.

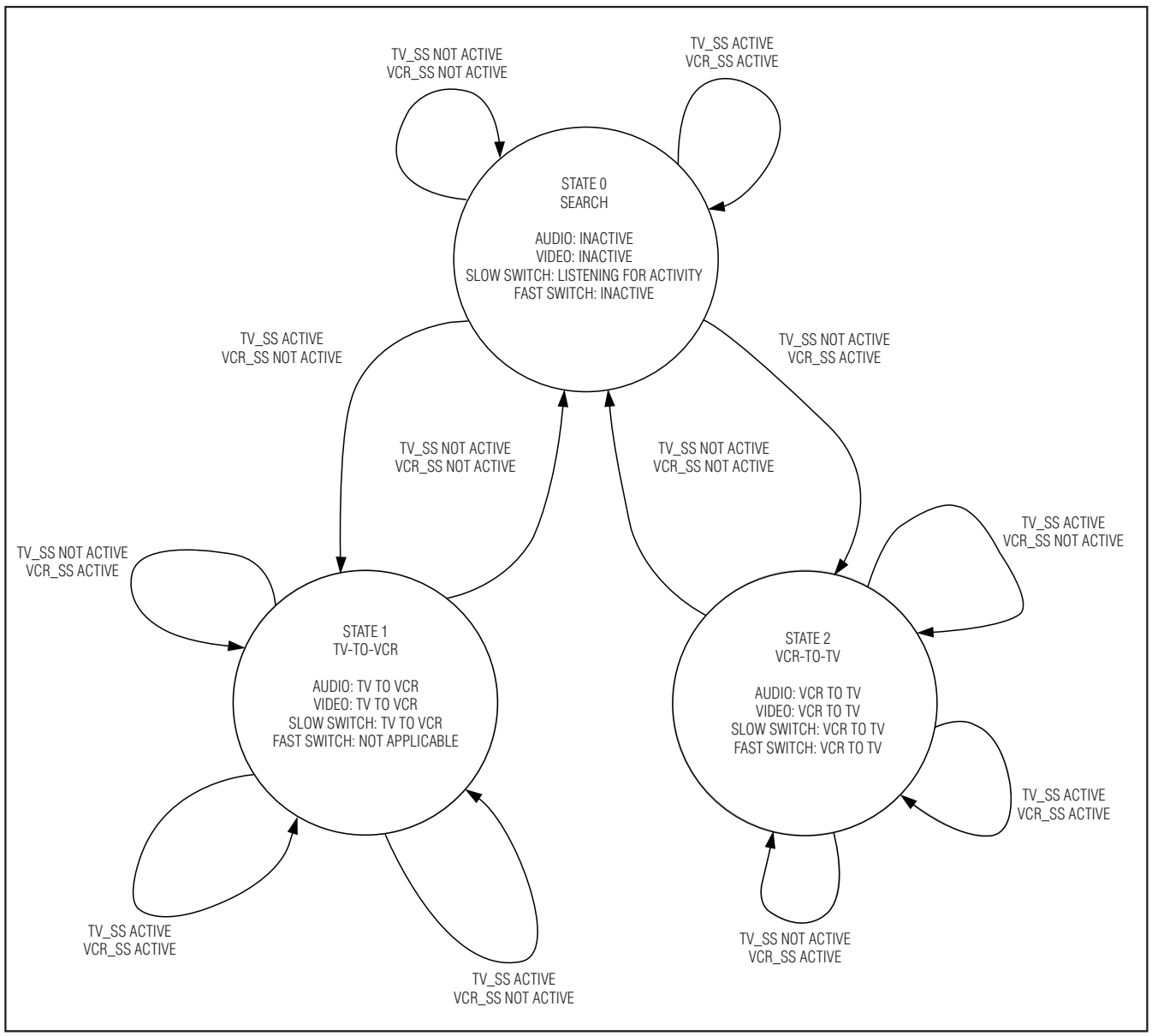

Figure 14. Standby mode finite state machine. TV_SS is active when either 6V or 12V are present. VCR_SS is active when either 6V or 12V are present.

S-Video

The MAX9670/MAX9671 support S-video from the set-top box to the TV, set-top box to the VCR, and VCR to the set-top box. S-video was not included in the original SCART specifications but was added afterwards. As a consequence, the luma (Y) signal of S-video shares the same SCART pin as the CVBS signal. Likewise, the chroma (C) signal shares the same SCART pin as the red signal. The pins that can carry both CVBS and luma have Y/CVBS in their names, and the pins that can carry red and chroma have R/C in their names.

Now, the Y/CVBS signals are full duplex while the R/C signals are half duplex. Therefore, S-video is limited to being half duplex. The MAX9670/MAX9671 have to transmit a chroma signal and receive a chroma signal

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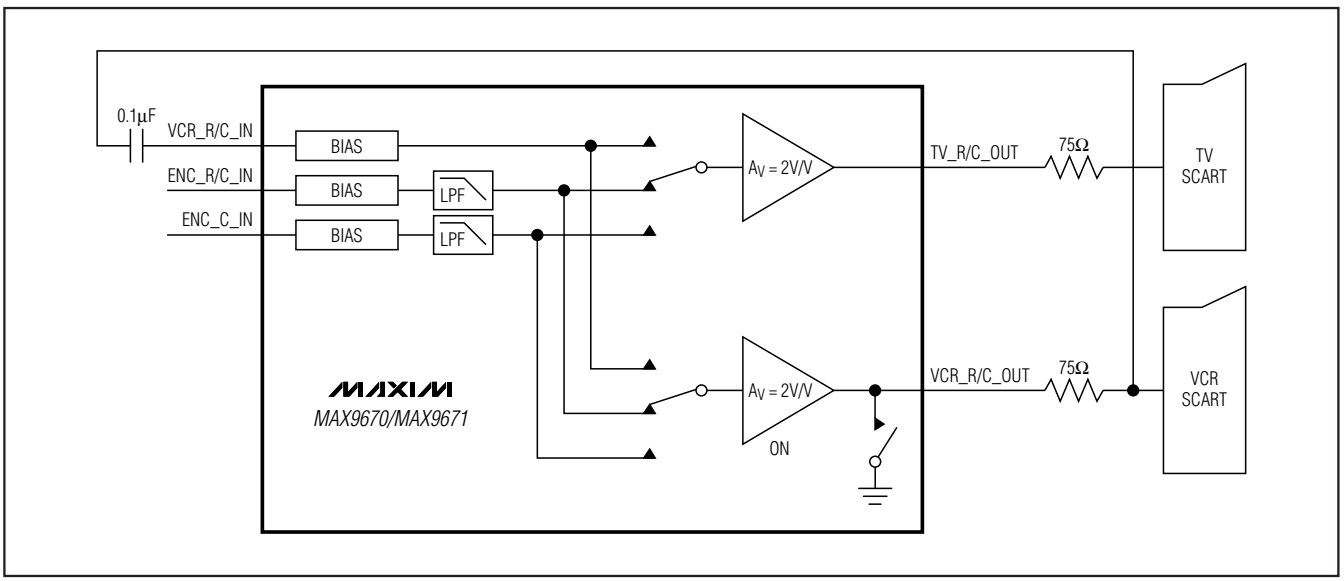

Figure 15. Gain-of-2 amplifier on VCR_R/C_OUT outputs chroma signal to VCR SCART connector. Notice that the pulldown switch on VCR_R/C_OUT is open.

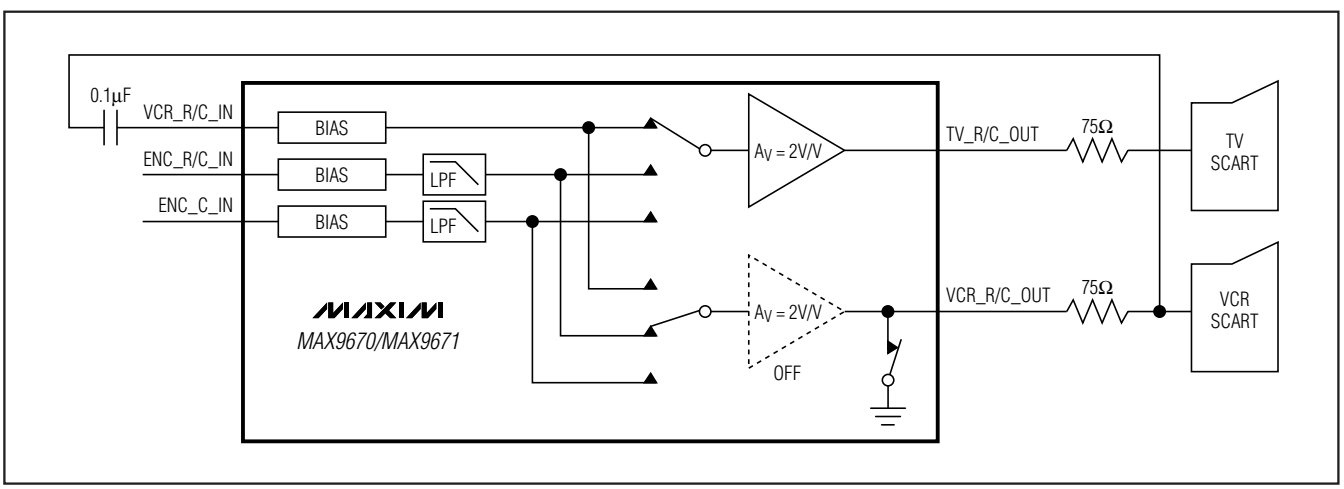

Figure 16. VCR_R/C_IN receives chroma signal from VCR SCART connector. Notice that the pulldown switch on VCR_R/C_OUT is closed and that the gain-of-2 amplifier is off. The chroma signal from VCR SCART is looped through to the TV SCART in the above configuration.

on the same SCART pin, but not at the same time. The 75Ω resistor connected to VCR_R/C_OUT must act as a back termination resistor when the MAX9670/MAX9671 is transmitting chroma signal and as an input termination resistor when it is receiving a chroma signal. Figure 15 shows how the MAX9670/MAX9671 transmits a chroma signal to the VCR SCART connector while Figure 16 shows how the MAX9670/MAX9671 receives a chroma from the VCR SCART connector.

Write a 0 into bit 2 of register 09h to open the pulldown switch at VCR_R/C_OUT. To close the pulldown switch, write a 0 into bit 6 of register 0Dh to turn off the output amplifier, and then write a 1 into bit 2 of register 09h. See Tables 17 and 18.

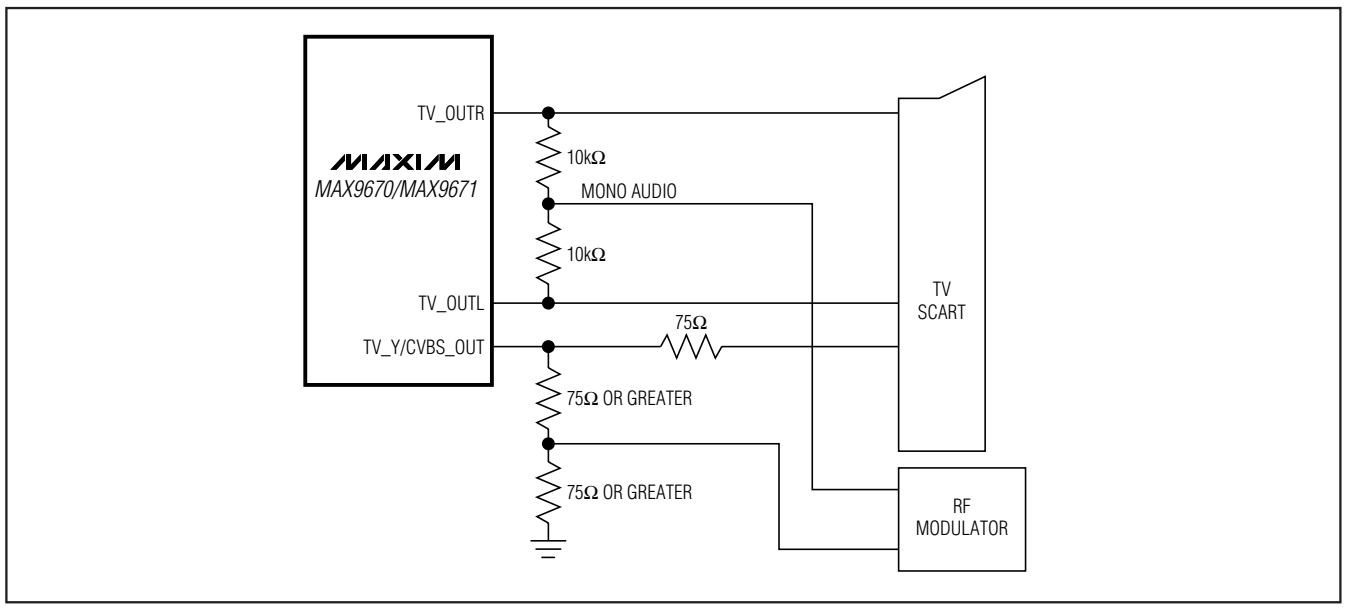

Figure 17. Application Circuit to Connect CVBS and Mono Audio from TV SCART to RF Modulator

Interfacing to an RF Modulator

If the set-top box modulates CVBS and mono audio onto an RF carrier (for example, channel 3), a simple application circuit can provide the needed signals (see Figure 17). 10kΩ resistor summer circuit between TV_OUTR and TV_OUTL creates the mono audio signal. The resistor-divider to ground on TV_Y/CVBS_OUT creates a video signal with normal amplitude. The unique feature of the MAX9670/MAX9671 that facilitates this application circuit is that the audio and video output amplifiers of the MAX9670/MAX9671 can drive multiple loads if V_{AUD} and V_{VID} are both greater than 3.135V.

Unconnected-Chassis Discharge Protection and ESD

Some set-top boxes are not connected to earth ground. As a result, the chassis can charge up to 500V. When a SCART cable is connected to the SCART connector, the charged chassis can discharge through a signal pin. The equivalent circuit is a 2200pF capacitor charged to 311V connected through less than 0.1Ω to a signal pin. The MAX9670/MAX9671 are soldered on the PCB when it experiences such a discharge. Therefore, the current spike flows through both external and internal ESD protection devices and is absorbed by the supply bypass capacitors, which have high capacitance and low ESR.

To better protect the MAX9670/MAX9671 against excess voltages during the cable discharge condition or ESD events, add series resistors to all inputs and outputs to the SCART connector if series resistors are not already present in the application circuit. Also, add external ESD protection diodes (for example, BAV99) on all inputs and outputs to the SCART connector.

SCART Set-Top Box with Analog HD Outputs

In set-top boxes with SCART connectors and cinch connectors for high-definition YPbPr outputs, a triple-video DAC usually outputs either standard-definition RGB signals that are routed to the MAX9670/MAX9671 or high-definition YPbPr signals that are routed through a high-definition filter amplifier like the MAX9653 (see Figure 19). The set-top box devices have a limited number of video DACs, and hence, one bank of triple-video DACs switches video format depending upon whether standard-definition RGB or high-definition YPbPr signals are required.

When RGB signals are desired, the high-definition filter amplifier should be turned off so that the RGB signals do not appear on the YPbPr connectors. The MAX9653/MAX9654 are well-suited for this application because their video inputs are in high-impedance mode when in shutdown.

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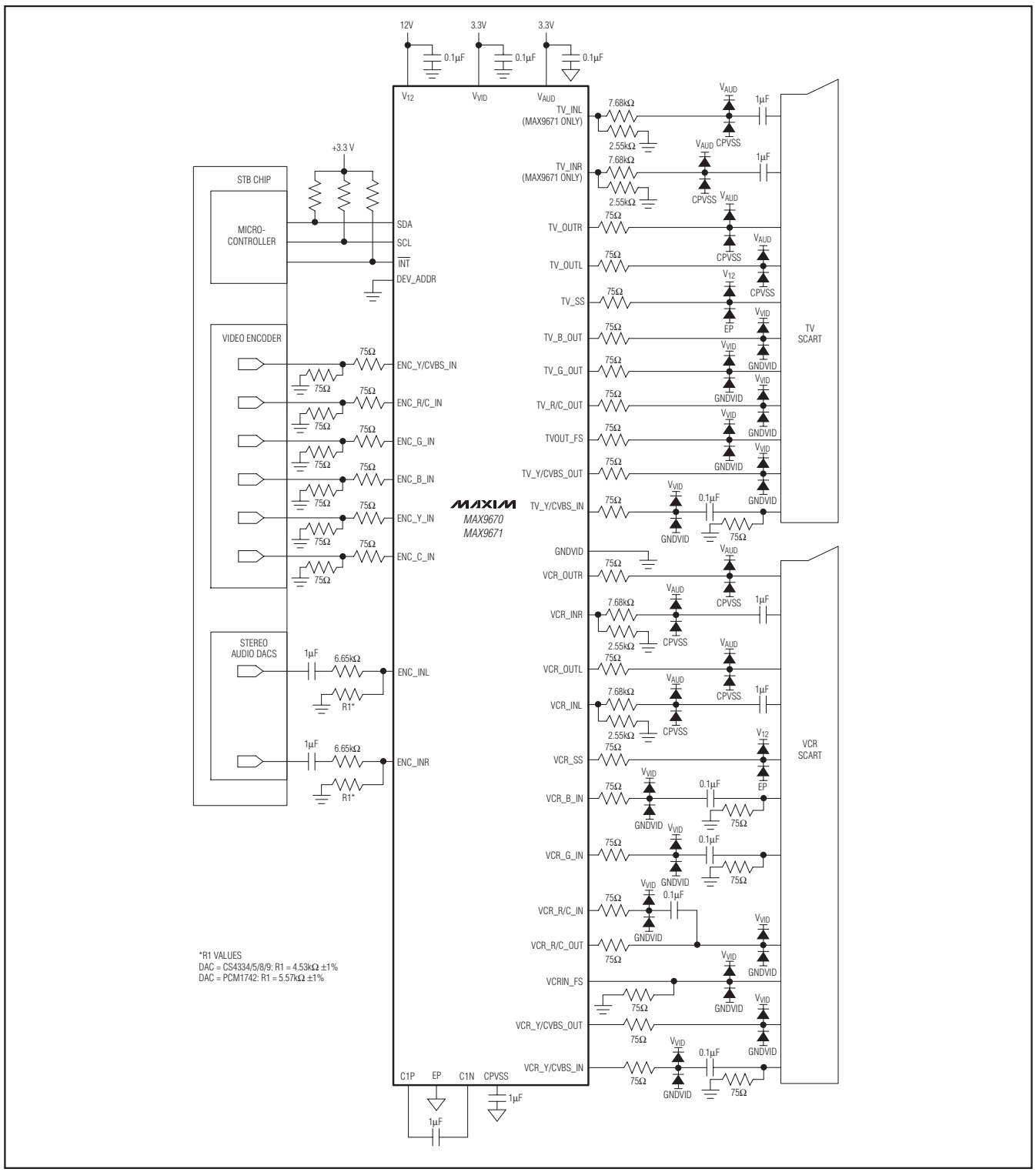

Figure 18. Application Circuit to Connect Series Resistors and External ESD Protection Diodes at MAX9670/MAX9671 Outputs

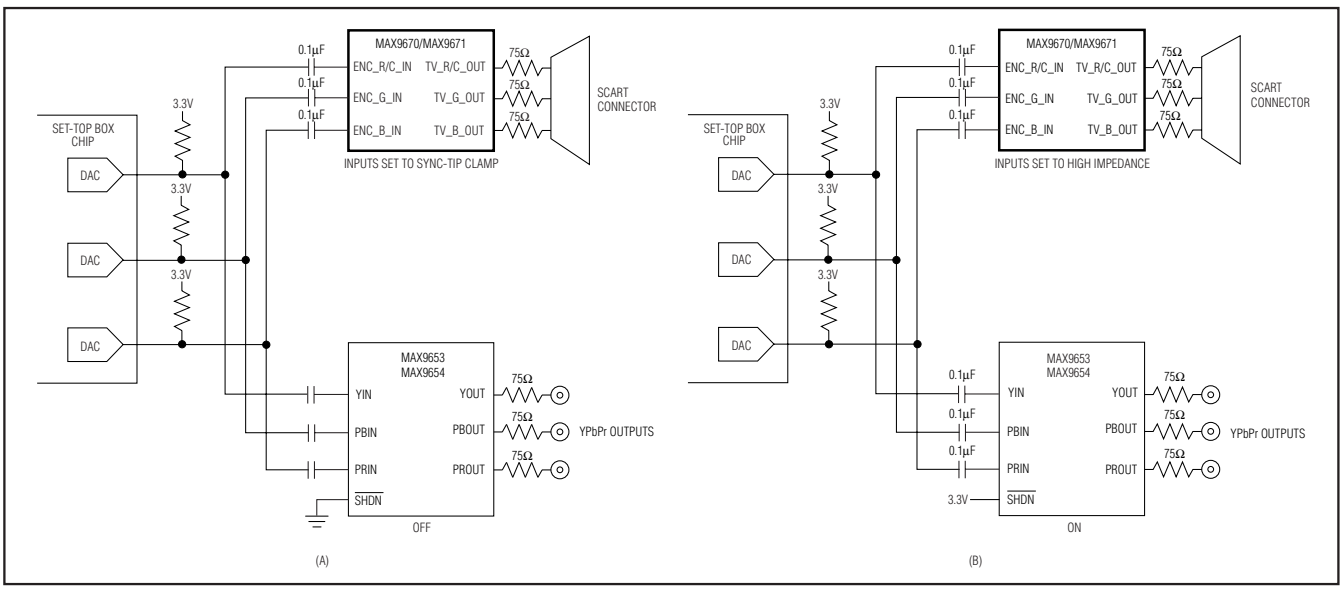

Figure 19. Triple DAC is connected to both a MAX9670/MAX9671 and a MAX9653/MAX9654 high-definition video-filter amplifier. (A) The MAX9670/MAX9671 are transmitting standard-definition RGB signals while the MAX9653/MAX9654 are in shutdown mode. (B) The MAX9670/MAX9671 are not transmitting RGB signals, but the MAX9653/MAX9654 are transmitting high-definition YPbPr signals.

Similarly, when YPbPr signals are desired, ENC_R/C_IN, ENC_G_IN, and ENC_B_IN of the MAX9670/MAX9671 should be set to high-impedance mode by setting bit 4 in register 08h to high if those video inputs are AC-coupled. The high-impedance mode has higher priority whether ENC_R/C_IN is in sync-tip clamp or bias circuit mode (set by bit 3 in register 08h). If ENC_R/C_IN, ENC_G_IN, and ENC_B_IN are DC-coupled, the inputs should be left in sync-tip clamp mode. The RGB outputs of the MAX9670/MAX9671 should be muted or shut down.

In either case, the inactive device should not distort the video signals generated by the DACs.

Power-Supply Bypassing

The MAX9670/MAX9671 feature single 3.3V and 12V supply operation and require no negative supply. The 12V supply V_{12} is for the SCART switching function. For V_{12}, place a 0.1µF bypass capacitor as close as possible. Connect all V_{AUD} pins together to 3.3V and bypass with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor to audio ground. Bypass each V_{VID} to video ground with a 0.1µF ceramic capacitor.

Using a Digital Supply

The MAX9670/MAX9671 are designed to operate from noisy digital supplies. The high PSRR (49dB at 100kHz) allows the MAX9670/MAX9671 to reject the noise from the digital power supplies (see the *Typical Operating Characteristics*). If the digital power supply is very noisy and stripes appear on the television screen, increase the supply bypass capacitance. An additional, smaller capacitor in parallel with the main bypass capacitor can reduce digital supply noise because the smaller capacitor has lower equivalent series resistance (ESR) and equivalent series inductance (ESL).

Layout and Grounding

For optimal performance, use controlled-impedance traces for video signal paths and place input termination resistors and output back-termination resistors close to the MAX9670/MAX9671. Avoid routing video traces parallel to high-speed data lines.

The MAX9670/MAX9671 provide separate ground connections for video and audio supplies. For best performance, use separate ground planes for each of the ground returns and connect all ground planes together at a single point. See the MAX9670/MAX9671 evaluation kit for a proven circuit board layout example.

If the MAX9670/MAX9671 are mounted using flow soldering or wave soldering, the ground via(s) for the EP pad should have a finished hole size of at least 14mils to insure adequate wicking of soldering onto the exposed pad. If the MAX9670/MAX9671 are mounted using solder mask technique, the via requirement does not apply. In either case, a good connection between the exposed pad and ground is required to minimize noise from coupling onto the outputs.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Table 1. Recommended Coupling for Incoming Video Signals and Input Circuit Configuration*

VIDEO ORIGIN	FORMAT	VOLTAGE RANGE	COUPLING	INPUT CIRCUIT CONFIGURATION
External	CVBS	Unknown	AC	Transparent sync-tip clamp
External	RGB	Unknown	AC	Transparent sync-tip clamp
External	Y	Unknown	AC	Transparent sync-tip clamp
External	C	Unknown	AC	Bias circuit
Internal	CVBS	0 to 1V	DC	Transparent sync-tip clamp
Internal	RGB	0 to 1V	DC	Transparent sync-tip clamp
Internal	Y/C	0 to 1V	DC	Transparent sync-tip clamp
Internal	YPbPr	0 to 1V	DC	Transparent sync-tip clamp
Internal	CVBS	2.3V to 3.3V	AC	Transparent sync-tip clamp
Internal	RGB	2.3V to 3.3V	AC	Transparent sync-tip clamp
Internal	Y	2.3V to 3.3V	AC	Transparent sync-tip clamp
Internal	C	2.3V to 3.3V	AC	Bias circuit

**Use a 0.1µF capacitor to AC-couple a video signal into the MAX9670/MAX9671.*

Table 2. Slow-Switching Modes

SLOW-SWITCHING SIGNAL VOLTAGE (V)	MODE
0 to 2	Display device uses an internal source such as a built-in tuner to provide a video signal.
4.5 to 7.0	Display device uses a video signal from the SCART connector and sets the display to 16:9 aspect ratio.
9.5 to 12.6	Display device uses a signal from the SCART connector and sets the display to 4:3 aspect ratio.

Table 3. Slave Address

DEV_ADDR	B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS (hex)	READ ADDRESS (hex)
GNDVID	1	0	0	1	0	1	0	R/$\overline{W}$	94h	95h
V_{VID}	1	0	0	1	0	1	1	R/$\overline{W}$	96h	97h
SCL	1	0	0	1	1	0	0	R/$\overline{W}$	98h	99h
SDA	1	0	0	1	1	0	1	R/$\overline{W}$	9Ah	9Bh

Table 4. I²C Register Values in State 0*

REGISTER ADDRESS (hexadecimal)	VALUE (binary)
00h	uuuu uuuu
01h	uuuu 1111
06h	uuuu uuuu
07h	uuuu uu10
08h	uuuu uuuu
09h	uuuu u010
0Dh	0000 000u

**u indicates that the bit is unchanged from its previous state.*

Table 5. I²C Register Values in State 1*

REGISTER ADDRESS (hexadecimal)	VALUE (binary)
00h	uuuu uuu0
01h	uuuu 1011
06h	uuuu uuuu
07h	uuu0 0u10
08h	uuuu u011
09h	uuuu u0MM
0Dh	1100 001u

**u indicates that the bit is unchanged from its previous state; MM = Register 0Eh (bit 1, bit 0)*

Table 6. I²C Register Values in State 2*

REGISTER ADDRESS (hexadecimal)	VALUE (binary)
00h	uuuu uuu0
01h	uuuu 1101
06h	uuu0 1010
07h	uuu0 0uNN
08h	uuuu uuuu
09h	uuuu u110
0Dh	0011 111u

**u indicates that the bit is unchanged from its previous state; NN = Register 0Eh (bit 3, bit 2)*

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Table 7. Quiescent Power Consumption

OPERATING MODE	POWER CONSUMPTION (mW)
Shutdown	0.13
Standby mode with no video activity (i.e., TV slow-switch and VCR slow-switch inputs are at ground). Standby mode is the power-on default.	2.83
Full-power mode with input video detection and video load detection active.	66
Full-power mode without input video detection and video load detection active.	65

Table 8. Average Power Consumption

OPERATING MODE	POWER CONSUMPTION (mW)
Full-power mode with input video detection and video load detection active.	300
Full-power mode without input video detection and video load detection active.	300

Table 9. Conditions for Average Power Consumption Measurement

PIN (MAX9670)	NAME	TYPE	SIGNAL	LOAD
5	V_{AUD}	Supply	3.3V	N/A
9	ENC_INL	Input	$0.25V_{RMS}$, 1kHz	N/A
10	ENC_INR	Input	$0.25V_{RMS}$, 1kHz	N/A
11	VCR_INL	Input	None	N/A
12	VCR_INR	Input	None	N/A
13	TV_OUTL	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
14	VCR_OUTL	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
15	VCR_OUTR	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
16	TV_OUTR	Output	$1V_{RMS}$, 1kHz	10kΩ to ground
17	TV_SS	Output	12V	10kΩ to ground
18	V_{12}	Supply	12V	N/A
19	VCR_SS	Input	0	N/A
20	TVOUT_FS	Output	3.3V	150Ω to ground
21	VCRIN_FS	Input	0	N/A
22	ENC_B_IN	Input	50% flat field	N/A
23	ENC_G_IN	Input	50% flat field	N/A
24	VCR_B_IN	Input	None	N/A
25	VCR_G_IN	Input	None	N/A
26	TV_B_OUT	Output	50% flat field	150Ω to ground
27	TV_G_OUT	Output	50% flat field	150Ω to ground
28	GNDVID	Supply	0	N/A
29	VCR_R/C_IN	Input	None	N/A
30	V_{VID}	Supply	3.3V	N/A

Table 9. Conditions for Average Power Consumption Measurement (continued)

PIN (MAX9670)	NAME	TYPE	SIGNAL	LOAD
31	ENC_C_IN	Input	None	N/A
32	ENC_R/C_IN	Input	50% flat field	N/A
33	TV_R/C_OUT	Output	50% flat field	150Ω to ground
34	VCR_R/C_OUT	Output	50% flat field	150Ω to ground
35	VCR_Y/CVBS_OUT	Output	50% flat field	150Ω to ground
36	TV_Y/CVBS_OUT	Output	50% flat field	150Ω to ground
37	VCR_Y/CVBS_IN	Input	None	N/A
38	TV_Y/CVBS_IN	Input	None	N/A
39	ENC_Y_IN	Input	None	N/A
40	ENC_Y/CVBS_IN	Input	50% flat field	N/A

Table 10. Data Format for Write Mode

REGISTER ADDRESS (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	Not used	TV ZCD	TV volume control					TV audio output mute
01h	Not used			Interrupt enable	VCR audio selection		TV audio selection	
02h	Not used							
03h	Not used							
04h	Not used							
05h	Not used							
06h	Not used			TV G and B video switch		TV video switch		
07h	Not used			Set TV fast switching		Not used	Set TV slow switching	
08h	VCR_R/C_IN clamp	Not used		ENC R/G/B high-impedance bias	ENC_R/C_IN clamp	VCR video switch		
09h	Not used					VCR_R/C_OUT ground	Set VCR slow switching	
0Ah	Not used							
0Bh	Not used							
0Ch	Not used							
0Dh	VCR_Y/ CVBS_OUT enable	VCR_R/ C_OUT enable	TV_R/ C_OUT enable	TV_G_OUT enable	TV_B_OUT enable	TV_Y/ CVBS_OUT enable	TVOUT_FS enable	Not used
10h	Operating mode		Not used					

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Table 11. Data Format for Read Mode

REGISTER ADDRESS (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0Eh	Not used	Power-on reset	Not used		VCR slow-switch input status		TV slow switch input status	
0Fh	Not used		ENC_Y_IN input video detection	ENC_Y/ CVBS_IN input video detection	VCR CVBS output load	VCR CVBS input video detection	TV CVBS output load	TV CVBS input video detection

Table 12. Register 00h: Audio Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Audio Mute								0	Off
								1	On (power-on default)
TV Volume Control			0	0	0	0	0		0dB gain (power-on default)
			0	0	0	0	1		-2dB gain
			0	0	0	1	0		-4dB gain
			0	0	0	1	1		-6dB gain
			0	0	1	0	0		-8dB gain
			0	0	1	0	1		-10dB gain
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
			1	1	1	1	0		-60dB gain
			1	1	1	1	1		-62dB gain
TV Zero-Crossing Detector		0							Off
		1							On (power-on default)

Table 13. Register 01h: TV Audio

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Input Source for TV Audio							0	0	Encoder audio
							0	1	VCR audio
							1	0	TV audio (MAX9671 only)
							1	1	Mute (power-on default)
Input Source for VCR Audio					0	0			Encoder audio
					0	1			VCR audio
					1	0			TV audio (MAX9671 only)
					1	1			Mute (power-on default)
Interrupt Enable				0					Disabled (power-on default)
				1					Enabled

Table 14. Register 06h: TV Video Input Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for TV Video									**TV_Y/CVBS_OUT**	**TV_R/C_OUT**
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	Mute
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
Input Sources for TV_G_OUT and TV_B_OUT									**TV_G_OUT**	**TV_B_OUT**
				0	0				ENC_G_IN	ENC_B_IN
				0	1				VCR_G_IN	VCR_B_IN
				1	0				Mute	Mute
				1	1				Mute (power-on default)	Mute (power-on default)

Table 15. Register 07h: TV Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set TV Slow Switching							0	0	Low (< 2V) internal source
							0	1	Medium (4.5V to 7V); external SCART source with 16:9 aspect ratio
							1	0	High impedance (power-on default)
							1	1	High (> 9.5V); external SCART source with 4:3 aspect ratio
Set TV Fast Switching				0	0				GNDVID (power-on default)
				0	1				Not used
				1	0				Same level as VCRIN_FS
				1	1				V_{VID}

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Table 16. Register 08h: ENC and VCR Video Input/Output Control

DESCRIPTION	BIT								COMMENTS	
	7	6	5	4	3	2	1	0		
Input Sources for VCR Video									**VCR_Y/CVBS_OUT**	**VCR_R/C_OUT**
						0	0	0	ENC_Y/CVBS_IN	ENC_R/C_IN
						0	0	1	ENC_Y_IN	ENC_C_IN
						0	1	0	VCR_Y/CVBS_IN	VCR_R/C_IN
						0	1	1	TV_Y/CVBS_IN	Mute
						1	0	0	Not used	Not used
						1	0	1	Mute	Mute
						1	1	0	Mute	Mute
						1	1	1	Mute (power-on default)	Mute (power-on default)
ENC_R/C_IN Clamp/Bias					0				DC restore clamp active at input (power-on default)	
					1				Chrominance bias applied at input	
ENC R/C, G, and B inputs high-impedance bias (in HD application)				0					High-impedance bias off (power-on default)	
				1					Biases the R/C, G, and B inputs to high impedance (overwrites the ENC_R/C_IN clamp and bias bit)	
VCR_R/C_IN Clamp/Bias	0								DC restore clamp active at input (power-on default)	
	1								Chrominance bias applied at input	

Table 17. Register 09h: VCR Video Output Control

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Set VCR Slow Switching							0	0	Low (< 2V) internal source
							0	1	Medium (4.5V to 7V); external SCART source with 16:9 aspect ratio
							1	0	High impedance (power-on default)
							1	1	High (> 9.5V); external SCART source with 4:3 aspect ratio
VCR_R/C_OUT Ground						0			Normal operation; pulldown on VCR_R/C_OUT is off (power-on default)
						1			Ground; pulldown on VCR_R/C_OUT is on; the output amplifier driving VCR_R/C_OUT is off

Table 18. Register 0Dh: Output Enable

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TVOUT_FS Enable							0		Off (power-on default)
							1		On
TV_Y/CVBS_OUT Enable						0			Off (power-on default)
						1			On
TV_B_OUT Enable					0				Off (power-on default)
					1				On
TV_G_OUT Enable				0					Off (power-on default)
				1					On
TV_R/C_OUT Enable			0						Off (power-on default)
			1						On
VCR_R/C_OUT Enable		0							Off (power-on default)
		1							On
VCR_Y/CVBS_OUT Enable	0								Off (power-on default)
	1								On

Table 19. Register 10h: Operating Modes

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
Operating Mode	0	0							Shutdown
	0	1							Standby mode (power-on default). Input video detection circuits are active. Audio circuitry is off unless video is detected. Once slow switch is detected, the signal paths between the VCR and TV SCART are connected.
	1	0							Full-power mode with input video detection and video-load detection active.
	1	1							Full-power mode without input video detection and video-load detection active.

Table 20. Register 0Eh: Status

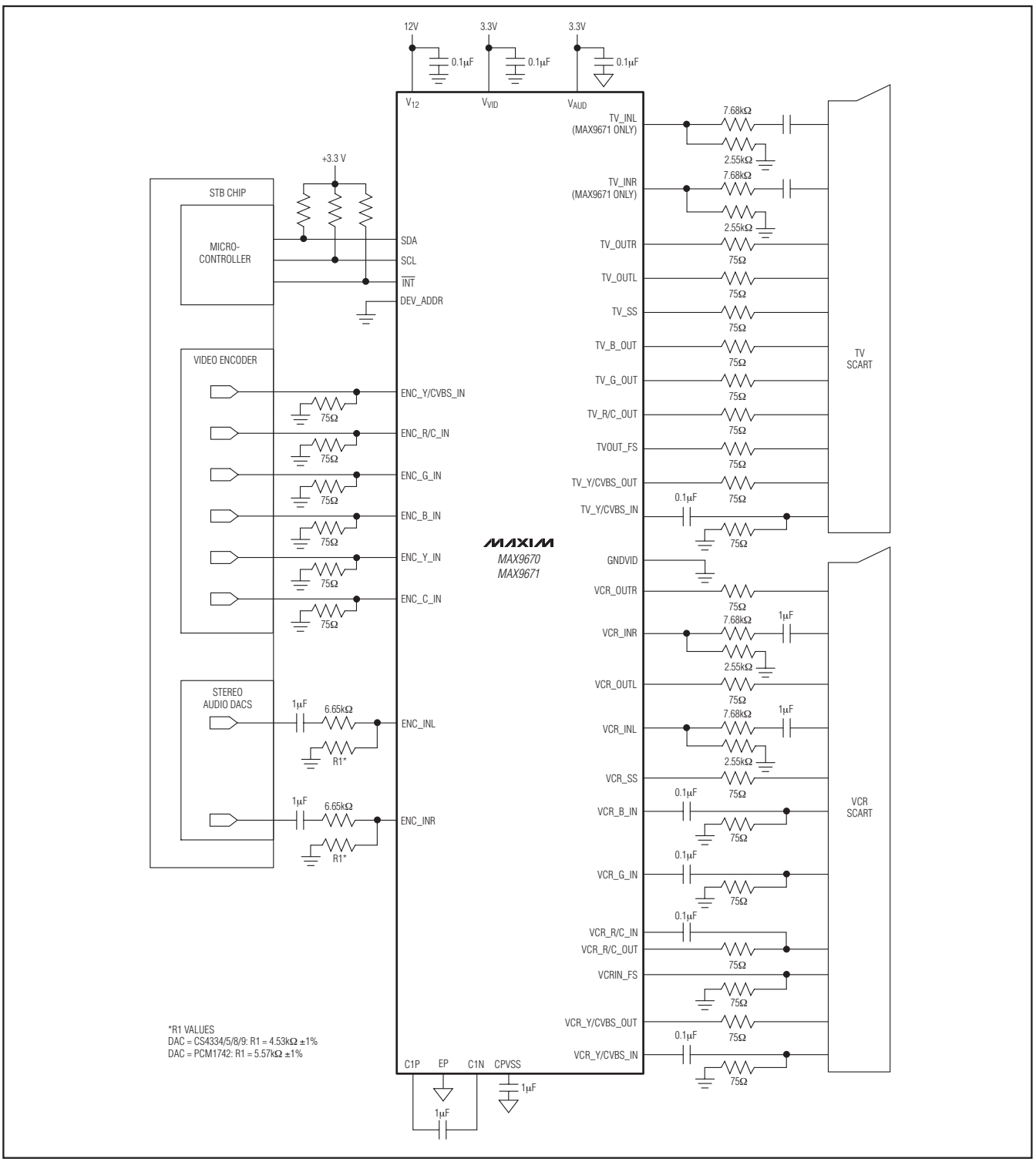
DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV Slow-Switching Input Status							0	0	0 to 2V; internal source
							0	1	4.5V to 7V; external source with 16:9 aspect ratio
							1	0	Not used
							1	1	9.5V to 12.6V; external source with 4:3 aspect ratio
VCR Slow-Switching Input Status					0	0			0 to 2V; internal source
					0	1			4.5V to 7V; external source with 16:9 aspect ratio
					1	0			Not used
					1	1			9.5V to 12.6V; external source with 4:3 aspect ratio
Power-On Reset		0							V_{VID} is too low for digital logic to operate
		1							V_{VID} is high enough for digital logic to operate

Table 21. Register 0Fh: Video Activity Status

DESCRIPTION	BIT								COMMENTS
	7	6	5	4	3	2	1	0	
TV CVBS Input Video Detection								0	No video detected.
								1	Video detected.
TV CVBS Output Load							0		No video detected.
							1		Video detected.
VCR CVBS Input Video Detection						0			No video detected.
						1			Video detected.
VCR CVBS Output Load					0				No load connected.
					1				Load connected.
ENC_Y/CVBS_IN Input Video Detection				0					No video detected.
				1					Video detected.
ENC_Y_IN Input Video Detection			0						No video detected.
			1						Video detected.

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Typical Application Circuit



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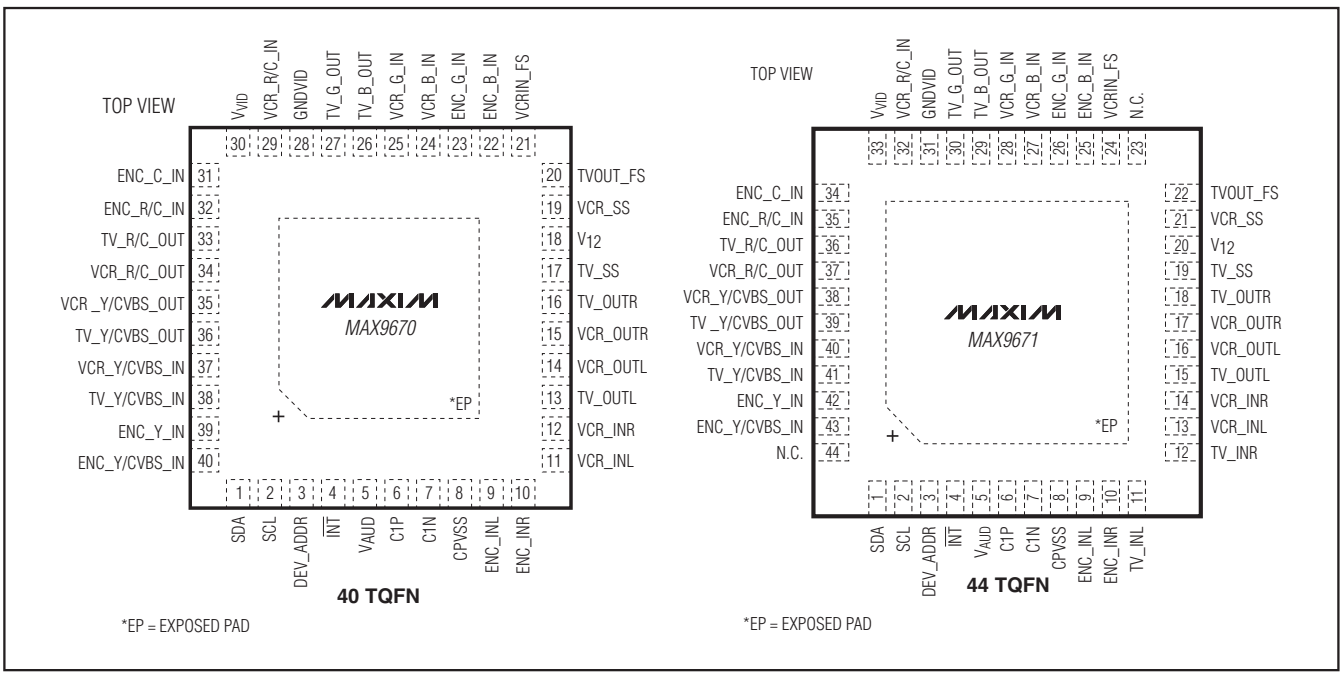
Pin Configurations



Chip Information

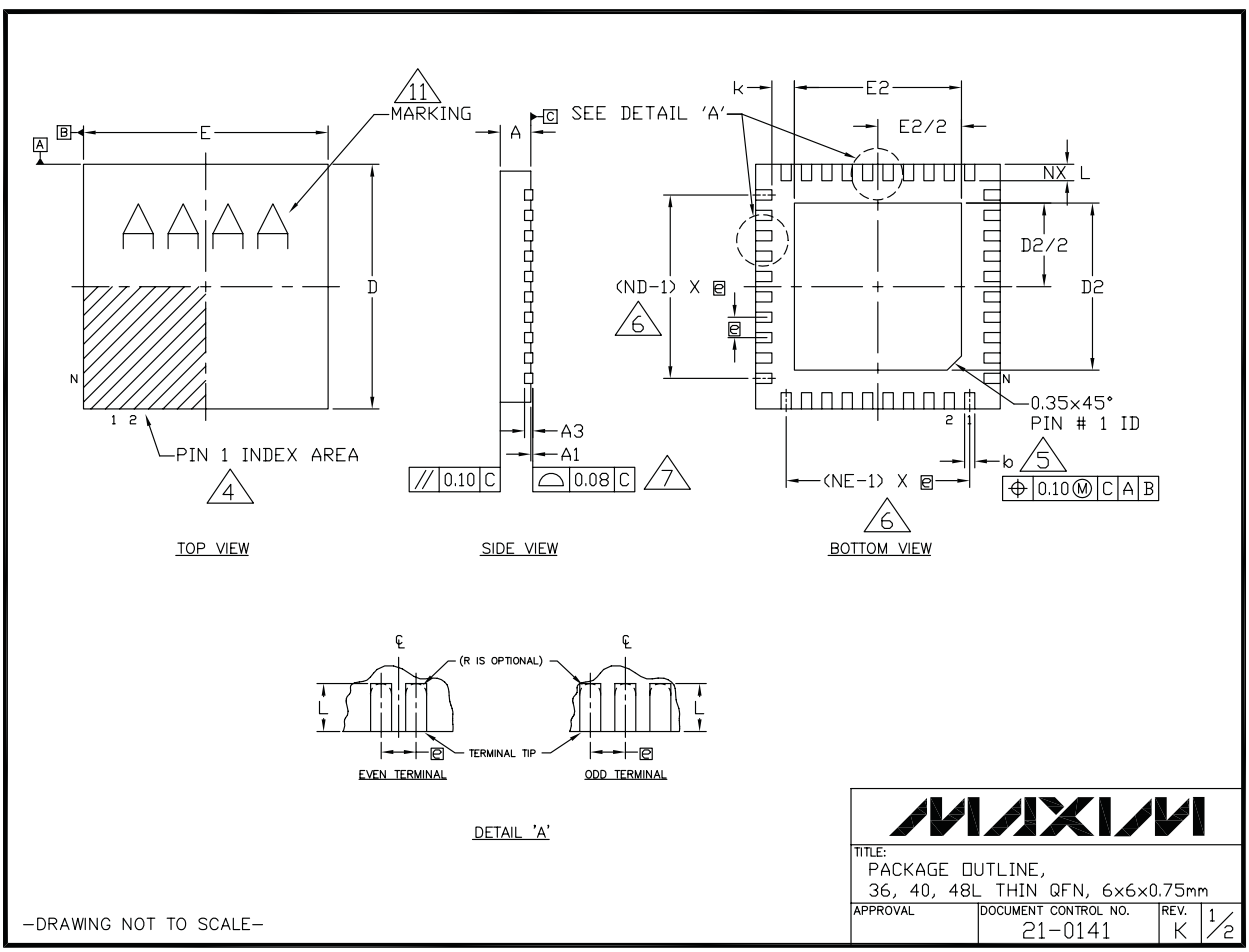
PROCESS: BiCMOS

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN	T4066+3	21-0141	90-0054
44 TQFN	T4477+2	21-0144	90-0127



Package Information (continued)

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COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60
T4066MN-5	4.00	4.10	4.20	4.00	4.10	4.20

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES IN DEGREES UNLESS OTHERWISE SPECIFIED
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH: PACKAGE T4866.
9. N IS THE TOTAL NUMBER OF TERMINALS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE:
PACKAGE OUTLINE,
36, 40, 48L THIN QFN, 6x6x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	K	2/2

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Package Information (continued)

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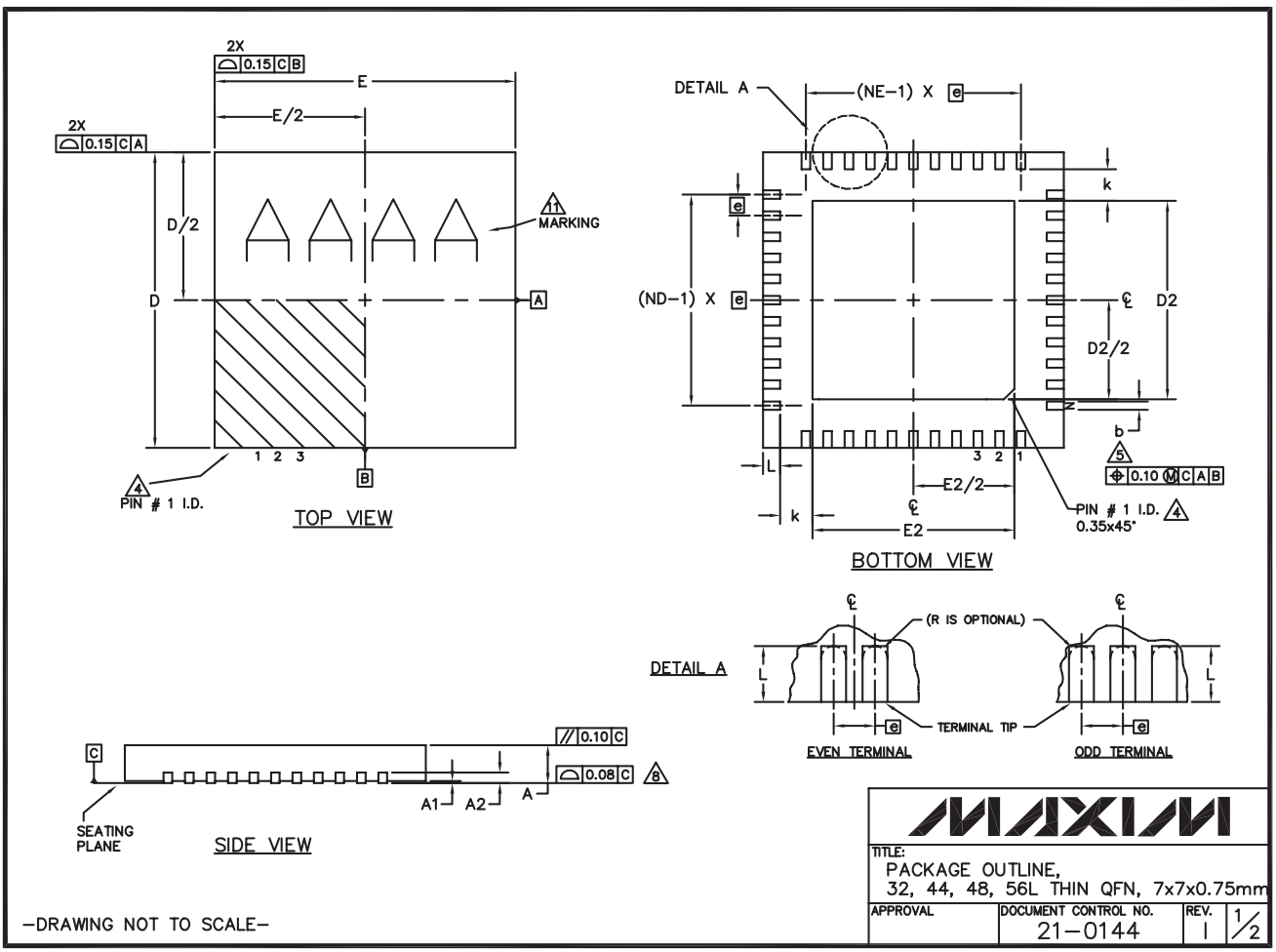

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Package Information (continued)

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COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877N-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677MN-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-3/-4/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 32, 44, 48, 56L THIN QFN, 7x7x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	I	2/2

Low-Power Audio/Video Switch with Audio Volume Control for Dual SCART Connectors

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	3/10	Added θ_{JA} and θ_{JC} information in the *Absolute Maximum Ratings* section, adjusted Note references, updated power consumption Figures, and made various corrections	1–8, 17, 20, 21, 22, 24–29, 33, 35, 36, 37
2	12/10	Updated Table 14	33

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