Product Change Notice (PCN)

Subject: Design and Mold Compound Change for the Intersil ISL78600ANZ* Products
Publication Date: 4/20/2016
Effective Date: 7/20/2016

Revision Description:
Initial Release

Description of Change:
All level and mold compound change to the ISL78600ANZ* to improve overall product performance.

Part numbers affected – ISL78600ANZ; ISL78600ANZ-T

Reason for Change:
The changes include several product performance improvements as listed below:

1. BGREF – implemented an amended secondary reference to improve performance post assembly of device onto printed circuit board.
2. Improved Latch-up performance

The mold compound change improves thermal stability of device post solder, for better precision performance.

The changes align the datasheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the changes are contained in Appendix B. the updated data sheet is available on the Intersil web site at:
http://www.intersil.com/content/dam/Intersil/documents/isl7/isl78600.pdf

Impact on fit, form, function, quality & reliability:
The change will have no other impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:
Product affected by this change is identifiable via Intersil's internal traceability system.

Qualification status: Complete, see Appendix A
Sample availability: 4/20/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Appendix A: Qualification Results

Qualification Results				
Stress	**Test Method**	**Sample Size (total)**	**# of Lots**	**Result**
High Temperature Operating Life (HTOL)	JESD22-A108	231	3	Pass
Early Life Failure Rate (ELFR)	AEC Q100-008	2400	3	Pass
Biased Hast (BHAST)	JESD22-A110	231	3	Pass
High Temperature Storage (HTS)	JESD22-A103	45	1	Pass
Unbiased HAST (UHAST)	JESD22-A118	231	3	Pass
Temperature Cycle (TC)	JESD22-A104	231	3	Pass

Appendix B: Datasheet Electrical Table Changes

From:

Absolute Maximum Ratings

Unless otherwise specified. With respect to VSS.

DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, ExTn, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n,
BASE, EN, VDDEXT ..... -0.2V to 4.1V
V2P5 ..... -0.2V to 2.9V
VBAT ..... -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 ..... -0.5V to (VBAT + 0.5V)
VC0 ..... -0.5V to +9.0V
VC1 ..... -0.5V to +18V
VC2 ..... -0.5V to +18V
VC3 ..... -0.5V to +27V
VC4 ..... -0.5V to +27V
VC5 ..... -0.5V to +36V
VC6 ..... -0.5V to +36V
VC7 ..... -0.5V to +45V
VC8 ..... -0.5V to +45V
VC9 ..... -0.5V to +54V
VC10 ..... -0.5V to +63V
VC11 ..... -0.5V to +63V
VC12 ..... -0.5V to +63V
VCn (for n = 0 to 12) ..... -0.5 to VBAT +0.5V
CBn (for n = 1 to 12) ..... -0.5 to VBAT +0.5V
CBn (for n = 1 to 9) ..... V(VCn-1) -0.5V to V(VCn-1) +9V
CBn (for n = 10 to 12) ..... V(VCn) -9V to V(VCn) +0.5V
Current into VCn, VBAT, VSS (Latch-up Test) ..... ±100mA
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Capacitive Discharge Model (Tested per JESD22-C101D) 500V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{DATA\ READY}$, and $\overline{FAULT}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(C/W)	θ_{JC}(C/W)
64 Ld TQFP Package (Notes 5, 6)	49	9

Max Continuous Package Power Dissipation 400mW
Storage Temperature ..... -55°C to +125°C
Max Operating Junction Temperature ..... +125°C
Pb-Free Reflow Profile ..... Refer to JEDEC J STD 020D

Recommended Operating Conditions

T_A, Ambient Temperature Range ..... -40°C to +105°C
V_{BAT} ..... 6V to 60V
V_{BAT} (Daisy Chain Operation) ..... 10V to 60V
VCn (for n = 1 to 12) ..... V(VCn-1) to V(VCn-1) + 5V
VC0 ..... -0.1V to 0.1V
CBn (for n = 1 to 9) ..... V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12) ..... V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN. ..... 0V to 3.6V
ExT1, ExT2, ExT3, ExT4 ..... 0V to 2.5V

To:

Absolute Maximum Ratings Unless otherwise specified. With respect to VSS.

BASE ..... -0.2V to 5.5V
DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, ExTn, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n,
EN, VDDEXT ..... -0.2V to 4.1V
V2P5 ..... -0.2V to 2.9V
VBAT ..... -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 ..... -0.5V to (VBAT + 0.5V)
VC0 ..... -0.5V to +9.0V
VC1 ..... -0.5V to +18V
VC2 ..... -0.5V to +18V
VC3 ..... -0.5V to +27V
VC4 ..... -0.5V to +27V
VC5 ..... -0.5V to +36V
VC6 ..... -0.5V to +36V
VC7 ..... -0.5V to +45V
VC8 ..... -0.5V to +45V
VC9 ..... -0.5V to +54V
VC10 ..... -0.5V to +63V
VC11 ..... -0.5V to +63V
VC12 ..... -0.5V to +63V
VCn (for n = 0 to 12) ..... -0.5 to VBAT +0.5V
CBn (for n = 1 to 12) ..... -0.5 to VBAT +0.5V
CBn (for n = 1 to 9) ..... V(VCn-1) -0.5V to V(VCn-1) +9V
CBn (for n = 10 to 12) ..... V(VCn) -9V to V(VCn) +0.5V
Current into VCn, VBAT, VSS (Latch-Up Test) ..... ±100mA
ESD Rating
Human Body Model (Tested per AECQ100-002) 2kV
Capacitive Discharge Model (Tested per AECQ100-011) 2kV
Latch-Up (Tested per AEC-Q100-004; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{DATA\ READY}$, and $\overline{FAULT}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(C/W)	θ_{JC}(C/W)
64 Ld TQFP Package (Notes 6, 7)	42	9

Maximum Continuous Package Power Dissipation 400mW
Storage Temperature ..... -55°C to +125°C
Maximum Operating Junction Temperature ..... +125°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

T_A, Ambient Temperature Range ..... -40°C to +105°C
V_{BAT} ..... 6V to 60V
V_{BAT} (Daisy Chain Operation) ..... 10V to 60V
VCn (for n = 1 to 12) ..... V(VCn-1) to V(VCn-1) + 5V
VC0 ..... -0.1V to 0.1V
CBn (for n = 1 to 9) ..... V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12) ..... V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN. ..... 0V to 3.6V
ExT1, ExT2, ExT3, ExT4 ..... 0V to 2.5V

From:

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 56 on page 84 or equivalent.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.8	5.1	5.6	V
Power-Up Condition Hysteresis	V_{PORhys}			400		mV

To:

Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.8	5.1	5.6	V
Power-Up Condition Hysteresis	V_{PORhys}			460		mV

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Supply Current	I_{VBAT}	Non Daisy Chain configuration. Device enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	7	35	80	µA
		39.6V	0	64	241	µA
		60V	0	90	250	µA
		-40°C to +105°C (Note 9)	0		280	µA
	$I_{VBATMASTER}$	Daisy Chain configuration – master device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	400	530	660	µA
		39.6V	500	680	900	µA
		60V	550	750	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak current when Daisy Chain transmitting		18		mA
	$I_{VBATMID}$	Daisy Chain configuration – MIDDLE stack device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	700	1020	1210	µA
		39.6V	900	1250	1560	µA
		60V	1000	1400	1700	µA
		-40°C to +105°C (Note 9)			1850	µA
		Peak current when Daisy Chain transmitting		18		mA
	$I_{VBATTOP}$	Daisy Chain configuration – top device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.				
		6V	400	530	660	µA
		39.6V	500	680	900	µA
		60V	550	750	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak Current when Daisy Chain transmitting		18		mA
	$I_{VBATSLEEP1}$ (Note 9)	Sleep mode (EN = 1, Daisy Chain configuration)				
		6V	14	18	23	µA
		39.6V	18	23	29	µA
		60V	20	25	30	µA
		-40°C to +105°C			41	µA
	$I_{VBATSLEEP2}$ (Note 9)	Sleep mode (EN = 1, Stand-alone, non-Daisy Chain)	3.5	6	16	µA
		-40°C to +105°C	3		70	µA
	$I_{VBATSHDN}$ (Note 9)	Shutdown, device "off" (EN = 0) (Daisy Chain and Non-Daisy Chain configurations)				
		6V	1.5	7	15.5	µA
		39.6V	3	7	18	µA
		60V	5	7	23	µA
		-40°C to +105°C	1		77	µA

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Supply Current Specifications						
V_{BAT} Supply Current	I_{VBAT}	Non-daisy chain configuration. Device enabled. No communications, ADC, measurement, balancing or open-wire detection activity.				
		6V		70	90	µA
		39.6V		73	95	µA
		60V		73	96	µA
		-40°C to +105°C (Note 9)			105	µA
	$I_{VBATMASTER}$	Daisy chain configuration – master device. Enabled. No communications, ADC, measurement, balancing or open-wire detection activity.				
		6V	400	550	660	µA
		39.6V	500	650	900	µA
		60V	550	710	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATMID}$	Daisy chain configuration – Middle stack device. Enabled. No communications, ADC, measurement, balancing or open-wire detection activity.				
		6V	700	1020	1210	µA
		39.6V	900	1210	1560	µA
		60V	1000	1340	1700	µA
		-40°C to +105°C (Note 9)			1850	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATTOP}$	Daisy chain configuration – top device. Enabled. No communications, ADC, measurement, balancing or open-wire detection activity.				
		6V	400	550	660	µA
		39.6V	500	650	900	µA
		60V	550	710	1000	µA
		-40°C to +105°C (Note 9)			1150	µA
		Peak current when daisy chain transmitting		18		mA
	$I_{VBATSLEEP1}$ (Note 9)	Sleep mode (EN = 1, daisy chain configuration)				
		6V	13	28	44	µA
		39.6V	18	33	48	µA
		60V	20	35	50	µA
		-40°C to +105°C			120	µA
	$I_{VBATSLEEP2}$ (Note 9)	Sleep mode (EN = 1, stand-alone, non-daisy chain)	13.2	19	34.1	µA
		-40°C to +105°C	13.5		109	µA
	$I_{VBATSHDN}$ (Note 9)	Shutdown, device "off" (EN = 0) (Daisy chain and non-daisy chain configurations)				
		6V	6	13	28	µA
		39.6V	7	15	29	µA
		60V	7	16	30	µA
		-40°C to +105°C			101	µA

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Supply Current Tracking, Sleep Mode.	$I_{VBAT\Delta SLEEP}$ (Note 9)	EN = 1, Daisy Chain Sleep Mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.	0	4	8	µA
		-40°C to +105°C	0		17	µA

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{BAT} Supply Current Tracking, Sleep Mode.	$I_{VBAT\Delta SLEEP}$ (Note 9)	EN = 1, daisy chain sleep mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.	0		18	µA
		-40°C to +105°C	0		56	µA

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to nonbalancing V_{BAT} current. V_{BAT} = 39.6V	250	300	350	µA
		-40°C to +105°C (Note 9)	200	300	400	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, Load current range 0 to 5mA. V_{BAT} = 39.6V	3.25	3.35	3.45	V
		-40°C to +105°C (Note 9)	3.2		3.5	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, Load current range. No load. (SLEEP). V_{BAT} = 39.6V	2.45	2.7	2.95	V
		-40°C to +105°C (Note 9)	2.4		3.05	V
V3P3 Regulator Control Current	I_{BASE}	Current sourced from BASE output. V_{BAT} = 6V	1	1.5		mA
		-40°C to +105°C (Note 9)	1			mA
V3P3 Supply Current	I_{V3P3}	Device Enabled No measurement activity, Normal Mode	0.8	1	1.2	mA
		-40°C to +105°C (Note 9)	0.8		1.3	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, No Load, Normal Mode		2.5		V
VDDEXT Switch Resistance	R_{VDDEXT}	Switch "On" resistance, V_{BAT} = 39.6V	8	12	17	Ω
		-40°C to +105°C (Note 9)	5		22	Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-Alone or Daisy Configuration. No ADC or Daisy Chain communications active.	2.0	3.25	4.5	mA
		-40°C to +105°C (Note 9)	2.0		5.0	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Stand-Alone or Daisy Configuration. Average current during 16ms Scan Continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		2.4		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	0	1.2	4.1	µA
		-40°C to +105°C (Note 9)			9.0	µA

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to non-balancing V_{BAT} current. V_{BAT} = 39.6V	250	300	350	µA
		-40°C to +105°C (Note 9)	200	300	400	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, Load current range 0 to 5mA. V_{BAT} = 39.6V	3.25	3.35	3.45	V
		-40°C to +105°C (Note 9)	3.2		3.5	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, Load current range. No load. (SLEEP). V_{BAT} = 39.6V		2.8		V
V3P3 Regulator Control Current	I_{BASE}	Current sourced from BASE output. V_{BAT} = 6V	1			mA
		-40°C to +105°C (Note 9)	1			mA
V3P3 Supply Current	I_{V3P3}	Device enabled No measurement activity, Normal mode	0.8	1	1.2	mA
		-40°C to +105°C (Note 9)	0.8		1.3	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, normal mode		2.5		V
VDDEXT Switch Resistance	R_{VDDEXT}	Switch "ON" resistance, V_{BAT} = 39.6V		12		Ω
		-40°C to +105°C (Note 9)	5		22	Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-alone or daisy configuration. No ADC or daisy chain communications active.	2.00	3.25	4.50	mA
		-40°C to +105°C (Note 9)	2.0		5.0	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Stand-alone or daisy configuration. average current during 16ms scan continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		0.5		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	0	0.5	3.5	µA
		-40°C to +105°C (Note 9)			9.0	µA

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 Input				
		VC0 ≥ 0.5 and VC0 ≤ 4.0V	-1.5	-1	-0.5	µA
		VC0 > 4.0V	-1.75		-0.5	µA
		-40°C to +105°C (Note 9)	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 Inputs				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-2.7	-2	-1.3	µA
		VCn - VC(n-1) > 4.0V	-2.85		-1.0	µA
		-40°C to +105°C (Note 9)	-3.0	-2	-0.84	µA
		VC4 Input				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-0.6	0	0.71	µA
		VCn - VC(n-1) > 4.0V	-0.8		1.15	µA
		-40°C to +105°C (Note 9)	- 0.84	0	1.31	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 Inputs				
		VCn - VC(n-1) < 2.6V	0.5	2	2.7	µA
		VCn - VC(n-1) ≥ 2.6V and VCn-VC(n-1) ≤ 4.0V	1.32	2	2.89	µA
		VCn - VC(n-1) > 4.0V	1.16	2	3.33	µA
		-40°C to +105°C (Note 9)	0.5	2	3.43	µA
		VC12 Input				
		VC12 - VC11 ≥ 0.5 and VC12-VC11 ≤ 4.0V	0.37	1	1.85	µA
		VC12 - VC11 > 4.0V	0.19		2.3	µA
		-40°C to +105°C (Note 9)	0.15	1	2.47	µA

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 Input				
		VC0 ≥ 0.5 and VC0 ≤ 4.0V	-1.5	-1	-0.5	µA
		VC0 > 4.0V	-1.75		-0.50	µA
		-40°C to +105°C (Note 9)	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 Inputs				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-2.7	-2	-1.3	µA
		VCn - VC(n-1) > 4.0V	-2.85		-1.00	µA
		-40°C to +105°C (Note 9)	-3.0	-2	-1.0	µA
		VC4 Input				
		VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-0.6	0	0.6	µA
		VCn - VC(n-1) > 4.0V	-0.7		0.7	µA
		-40°C to +105°C (Note 9)	- 0.8	0	0.8	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 Inputs				
		VCn - VC(n-1) < 2.6V	0.5	2	2.7	µA
		VCn - VC(n-1) ≥ 2.6V and VCn-VC(n-1) ≤ 4.0V	1.5	2	2.7	µA
		VCn - VC(n-1) > 4.0V	1.50	2	2.85	µA
		-40°C to +105°C (Note 9)	0.5	2	3.0	µA
		VC12 Input				
		VC12 - VC11 ≥ 0.5 and VC12 - C11 ≤ 4.0V	0.6	1	1.7	µA
		VC12 - VC11 > 4.0V	0.60		1.75	µA
		-40°C to +105°C (Note 9)	0.6	1	2.0	µA

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Initial V_{BAT} monitor Voltage Error (Note 10)	ΔV_{BAT}	Measured at V_{BAT} = 36V to 43.2V	-100		100	mV
		Measured at V_{BAT} = 31.2V to 48V	-125		125	mV
		Measured at V_{BAT} = 31.2V to 59.4V	-250		250	mV
		Measured at V_{BAT} = 6V to 59.4V	-320		332	mV
		Measured at V_{BAT} = 6V to 59.4V -40°C to +105°C (Note 9)	-490		490	mV
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	2.475	2.5	2.525	V
External Temperature Output Impedance	R_{TEMP}	Output Impedance at TEMPREG pin. (Note 9)	0	0.1	0.2	Ω
External Temperature Input Range	V_{EXT}	Effective ExTn input voltage range. For design reference. This is the input voltage range that does not trigger an open input condition.	0		2344	mV
External Temperature Input Pull-up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	-7.0		7.0	mV
		V_{BAT} = 39.6V, -40°C to +105°C (Note 9)	-10		10	mV
External Temperature Input INL	V_{EXTINL}	(Note 9)	-0.65		0.65	mV
External Temperature Input Gain Error	V_{EXTG}	Error at 2.5V input	-7.5		11	mV
		-40°C to +105°C (Note 9)	-13.4		19.3	mV

To:

Measured @ V_{BAT} = 31.2v to 59.4V removed from datasheet

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Initial V_{BAT} monitor Voltage Error (Note 10)	ΔV_{BAT}	Measured at V_{BAT} = 36V to 43.2V	-100		100	mV
		Measured at V_{BAT} = 31.2V to 48V	-125		125	mV
		Measured at V_{BAT} = 6V to 59.4V	-320		322	mV
		Measured at V_{BAT} = 6V to 59.4V -40°C to +105°C (Note 9)	-490		490	mV
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	2.475	2.500	2.525	V
External Temperature Output Impedance	R_{TEMP}	Output Impedance at TEMPREG pin. (Note 9)	0	0.1	0.2	Ω
External Temperature Input Range	V_{EXT}	Effective ExTn input voltage range. For design reference. This is the input voltage range that does not trigger an open input condition.	0		2344	mV
External Temperature Input Pull-Up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	-7.0		7.0	mV
		V_{BAT} = 39.6V, -40°C to +105°C (Note 9)	-10		10	mV
External Temperature Input INL	V_{EXTINL}	(Note 9)		±0.61		mV
External Temperature Input Gain Error	V_{EXTG}	Error at 2.5V input	-7.5		11	mV
		-40°C to +105°C (Note 9)	-8		18.5	mV

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V2P5 Power-good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V	2.62	2.7	2.766	V
		-40°C to +105°C (Note 9)	2.616		2.77	V
	V_{2PL} (Note 9)	2.5V power-good window low threshold. V_{BAT} = 39.6V	1.96	2.02	2.08	V
		-40°C to +105°C	1.90		2.14	V

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V2P5 Power-Good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V	2.65	2.70	2.90	V
		-40°C to +105°C (Note 9)	2.53		2.90	V
	V_{2PL} (Note 9)	2.5V power-good window low threshold. V_{BAT} = 39.6V	1.85	2.03	2.24	V
		-40°C to +105°C	1.76		2.28	V

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V (Note 9)	0.6	0.7	0.8	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1))-V(VCn), n = 2 to 12 V_{BAT} = 39.6V (Note 9)	-2	-1.5	0	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V (Note 9)	-100	-30	50	mV

To:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V (Note 9)	0.6	0.7	0.8	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1))-V(VCn), n = 2 to 12 V_{BAT} = 39.6V (Note 9)	-1.5	-1.2	-0.9	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V (Note 9)	-100	-39	10	mV

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
MEASUREMENT FUNCTION TIMING (Note 8)						
Cell Sample Time Start		Time to sample the first cell (CELL12) following $\overline{CS}$ going High. Scan voltages command		65	71.5	µs
Cell Sample Time Duration		Time to scan all 12 cells (sample of CELL12 to sample of CELL1) scan voltages command.		233	257	µs
Scan Voltages Processing Time		Time from start of scan to registers loaded to $\overline{DATA}$ $\overline{READY}$ going low		770	847	µs
Scan Temperatures Processing Time		Time from start of scan to registers loaded to $\overline{DATA}$ $\overline{READY}$ going low		2690	2959	µs
Scan Mixed Processing Time		Time from start of scan to registers loaded to $\overline{DATA}$ $\overline{READY}$ going low		830	913	µs
Scan Wires Processing Time		Time from start of scan to registers loaded to $\overline{DATA}$ $\overline{READY}$ going low		59.4	65.3	ms
Scan All Processing Time		Time from start of scan to registers loaded to $\overline{DATA}$ $\overline{READY}$ going low		63.2	69.5	ms
Measure Cell Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA}$ $\overline{READY}$ going low		180	198	µs
Measure V_{BAT} Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA}$ $\overline{READY}$ going low		130	143	µs
Measure Internal Temperature Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA}$ $\overline{READY}$ going low		110	121	µs
Measure External Temperature Input Processing Time		Time from start of measurement to register(s) loaded to $\overline{DATA}$ $\overline{READY}$ going low		2520	2772	µs
Measure Secondary Voltage Reference Time		Time from start of measurement to register(s) loaded to $\overline{DATA}$ $\overline{READY}$ going low		2520	2772	µs

8. Scan and Measurement start times are synchronised by the receiver to the falling edge of the 24th clock pulse (Daisy Chain systems) or to the falling edge of the 16th clock pulse (non-Daisy Chain, single device systems) of the Scan or *Measure* command. Clock pulses are at the SCLK pin for Master and Stand-alone devices, and at the DHI/DLo1 pins for middle and top Daisy Chain devices. Maximum values are based on characterization of the internal clock and are not 100% tested.

To: Removed from new datasheet

From:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
$\overline{\text{DATA READY}}$ Start Delay Time	$t_{DR:ST}$	Chip select high to $\overline{\text{DATA READY}}$ low. (Note 9)	100			ns
$\overline{\text{DATA READY}}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{\text{DATA READY}}$ high. (Note 9)			750	ns
$\overline{\text{DATA READY}}$ High Time	$t_{DR:WAIT}$	Time between bytes. (Note 9)	0.6			µs

To:

$t_{DR:ST}$ – removed from datasheet

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
$\overline{\text{DATA READY}}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{\text{DATA READY}}$ high		750		ns
$\overline{\text{DATA READY}}$ High Time	$t_{DR:WAIT}$	Time between bytes		1.0		µs