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Automotive High-Current Step-Down Converter with USB Protection/Host Charger Adapter Emulator

MAX16984

General Description

The MAX16984 combines a 5V automotive-grade step-down converter capable of driving up to 2.5A, a USB host charger adapter emulator, and USB protection switches for automotive USB host applications. The USB protection switches provide high-ESD, short-circuit protection and feature integrated host-charger port-detection circuitry adhering to the USB 2.0 Battery Charging Specification BC1.2 battery charging specification and Chinese Telecommunication Industry Standard YD/T 1591-2009. They also include circuitry for iPod®/iPhone® 1.0A and iPad® 2.1A dedicated charging modes. The HVD+ and HVD- ESD protection features include protection to ±15kV Air/±8kV Contact on the HVD+ and HVD- outputs to the IEC 61000-4-2 model and 330Ω, 330pF ESD model.

The high-efficiency step-down DC-DC converter operates from a voltage up to 28V and is protected from load dump transients up to 42V. The device is optimized for high-frequency operation and includes resistor-programmable frequency selection from 220kHz to 2.2MHz to allow optimization of efficiency, noise, and board space based on application requirements. The converter has an internal high-side n-channel switch and uses a low forward-drop freewheeling Schottky diode for rectification. There is a small low-side n-channel switch to maintain fixed frequency under light loads. For lower quiescent current operation requirements, the low side n-channel switch can be disabled to allow skip mode operation under light loads. The converter can deliver up to 2.1A of continuous current at 105°C. The MAX16984S has an integrated spread-spectrum oscillator to improve EMI performance.

The MAX16984 also includes a USB load current-sense amplifier and configurable feedback adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications. The MAX16984 limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter and a user-configurable external USB load current-sense amplifier threshold.

Applications

- Automotive Radio and Navigation
- USB Port for Host and Hub Applications
- Automotive Connectivity
- Telematics
- Dedicated USB Power Charger

Benefits and Features

- Integrated DC-DC and USB Host Charge Emulator Enables 1-Chip Solution Directly from Car Battery to Portable Device
  - 4.5V to 28V (42V Load Dump) Operating Voltage
  - 5V, 2.5A Output Current Capability
  - Low-Q Current Skip and Shutdown Modes
  - Soft-Start Reduces Inrush Current
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 220kHz to 2.2MHz Operation
  - Forced-PWM Option at No Load
  - Spread Spectrum for EMI Reduction
  - SYNC Input for Frequency Parking
- Optimal USB Power and Communication for Portable Devices
  - User-Adjustable Voltage Gain Adjusts Output Between 5V and 6.15V for Cable Compensation
  - ±3% Accuracy User-Adjustable USB Current Limit
  - 4Ω USB 2.0 480Mbps/12Mbps Data Switches
  - Integrated iPod/iPhone/iPad Charge-Detection Termination Resistors
  - Supports USB BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) Modes
  - Supports Chinese Telecommunication Industry Standard YD/T 1591-2009
  - Compatible with USB On-the-Go Specification
  - High-Speed Pass-Through Mode
- Robust Design Keeps Vehicle System and Portable Devices Safe in Automotive Environment
  - Short-to-Battery Protection on DC-DC Converter
  - Short-to-Battery Protection on USB Pins
  - ±25kV Air/±8kV Contact ISO 10605
  - ±15kV Air/±8kV Contact IEC 61000-4-2
  - ±15kV Air/±8kV Contact (330Ω, 330pF)
  - Fault-Indication Active-Low, Open-Drain Output
  - Reduced Inrush Current with Soft-Start
  - Overtemperature Protection
  - -40°C to +125°C Operating Temperature Range
  - 28-Pin, 5mm x 5mm, TQFN and Side-Wettable QFND Packages
  - 4mm x 4mm, 28-Pin CPQFN and Side-Wettable version available

Ordering Information and *Typical Operating Circuit* appear at end of data sheet.

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Absolute Maximum Ratings

IN, D+, D-, CD0, CD1, FBPER, FBMAX, SENSO, FBCAP to GND .....-0.3V to +6V
$\overline{FAULT}$, FOSC, BIAS, SYNC to GND .....-0.3V to +6V
D+, D- to IN .....+0.3V
HVD+, HVD- to GND .....-0.3V to +18V
SENSN, SENSP to GND .....-0.3V to +30V
SENSP to SENSN .....-6.0V to +6.0V
SUP, SUPSW, ENBUCK to GND .....-0.3V to +42V
LX (Note 1) .....-0.3V to +42V
SUP to SUPSW .....-0.3V to +0.3V
BST to GND .....-0.3V to +47V
BST to LX (Note 1) .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Output Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = 70°C)
Side-Wettable QFND (derate 33.3mW/°C above +70°C) .. 2666.7mW
TQFN (derate 34.5mW/°C above +70°C) 2759mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Side-Wettable QFND
Junction-to-Ambient Thermal Resistance (θ_{JA}).....30°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W

CPQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....3°C/W

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY AND ENABLE						
Supply Voltage Range	V_{SUP}	Normal operation	4.5		28	V
Load Dump Event Supply Voltage Range	V_{SUP_LD}	t < 1s (Note 4)			42	V
Supply Current	I_{SUP}	V_{IN} = 0V		6	20	µA
		V_{SYNC} = 0V, no load, skip mode		620	950	µA
		V_{SYNC} = 3.3V, no load, FPWM mode (Note 4)		9		mA
BIAS Voltage	V_{BIAS}	5.75V ≤ V_{SUP} = V_{SUPSW} ≤ 28V	4.71	5	5.31	V
BIAS Current Limit			40	120		mA
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} rising	3.93	4.2	4.46	V
BIAS Undervoltage Lockout Hysteresis				0.36		V
IN Voltage Range	V_{IN}		3.0		3.6	V
IN Enable High	V_{IN_IH}		1.6			V
IN Enable Low	V_{IN_IL}				0.5	V

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Overvoltage Lockout	V_{IN_OVLO}	V_{IN} rising	3.85	4.0	4.15	V
IN Input Current	I_{IN}			5	10	µA
ENBUCK Enable High	V_{ENBUCK_IH}		2.4			V
ENBUCK Enable Low	V_{ENBUCK_IL}				0.6	V
ENBUCK Hysteresis				0.15		V
ENBUCK Input Leakage		V_{ENBUCK} = 42V		0.01	1	µA
D+, D- ANALOG USB SWITCHES						
Analog Signal Range		Guaranteed by R_{ON} measurement (Note 4)	0		3.6	V
Protection Trip Threshold	V_{OV_D}		3.7	3.85	4.15	V
Protection Response Time	t_{FP_D}	V_{IN} = 4.0V, $V_{HVD±}$ = 3.3V to 4.3V step, R_L = 15kΩ on D±, delay to $V_{D±}$ < 3V		5		µs
Overvoltage Blanking Timeout Period	t_{B,OV_D}	From overvoltage condition to FAULT asserted		18	30	ms
On-Resistance Switch A	R_{ON_SA}	I_L = 5mA, 0V ≤ $V_{D±}$ ≤ 3.6V		4		Ω
On-Resistance Match Between Channels Switch A	DR_{ON_SA}	I_L = 5mA, $V_{D_}$ = 1.5V or 3.0V		10	150	mΩ
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	I_L = 5mA,$V_{D_}$ = 0V or 0.4V		10		mΩ
On-Resistance of HVD+/HVD- Short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD±}$ = 0V	-0.1	0	+0.1	µA
		$V_{HVD±}$ = 3.6V		2.5		
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	$V_{HVD±}$ = 18V, $V_{D±}$ = 0V		12		µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD±}$ = 18V, $V_{D±}$ = 0V	-1		+1	µA
On-Channel -3dB Bandwidth	BW	R_L = 50Ω, source impedance 50Ω (Figure 3)		400		MHz
Crosstalk	V_{CT}	R_L = 50Ω, f = 480MHz (Figure 3)		-14		dB
On-Capacitance Switch A	C_{ON}	f = 240MHz, V_{BIAS} = 250mV, V = 500mV_{P-P}		15		pF
Rise-Time Propagation Delay	t_{PLH}	R_S = R_L = 50Ω		200		ps
Fall-Time Propagation Delay	t_{PHL}	R_S = R_L = 50Ω		200		ps
Output Skew Between Switches	$t_{SK(O)}$	Skew between D+ and D- switch, R_L = 50Ω		50		ps
Output Skew Same Switch	$t_{SK(P)}$	Skew between opposite transitions in same switch, R_L = 50Ω		50		ps
CURRENT-SENSE AMP (SENSP, SENSN, FBMAX, SENSO)						
FBMAX, SENSO Transconductance	G_{SENSO}, G_{FBMAX}	I/(V_{SENSP} - V_{SENSN}), V_{SENSP} = 5.25V		2.50		mA/V

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSO, FBMAX Voltage Range	V_{SENSO}, V_{FBMAX}		0		1.2	V
Input Differential Voltage Range	ΔV_{SENSO}, ΔV_{FBMAX}	V_{SENSP} - V_{SENSN}	0		120	mV
Bandwidth of Transconductance		Determined by external RC time constant; assumed R = 10kΩ, and C = 10pF		1		MHz
SENSP Pulldown Resistance	R_{SENSP_DIS}	V_{SENSP} = 5.05V, V_{ENBUCK} = 0V or CD1 toggle; going into and out of auto-detection modes		300	600	Ω
SENSP Discharge Time Upon CD1 Toggle	t_{SENSP_DIS}	CD1 toggle; going into and out of auto-detection modes	0.5	1.1	2	s
SENSP Input Bias Current	t_{SENSP_LK}	V_{SENSP} = 5.05V		130	230	µA
SENSN Input Bias Current	t_{SENSN_LK}	V_{SENSN} = 5.05V		70	120	µA
SENSP Voltage Range			3.2		28	V
SENSN Overvoltage Threshold	V_{OV_SENSN}		6.8	7	7.1	V
SENSP Undervoltage Threshold	V_{UV_SENSP}		4.64	4.75	4.81	V
SENSN Protection Response Time	t_{OV_SENSN}			8		µs
SENSN Overvoltage Fault Blanking Timeout Period	t_{B,OV_SENSN}	From overvoltage condition to FAULT asserted	3	10	20	ms
SENSO CURRENT LIMIT RELATIONSHIP						
SENSO ILIMIT Threshold	V_{TH_ILIM}	SENSO rising, threshold used to set DC current limit		1.20		V
Continuous Current-Limit Fault Blanking Timeout	$t_{B,ILIM}$	From overcurrent condition to FAULT asserted	9	16.5	27	ms
ANALOG FEEDBACK ADJ						
SENSP Analog Adjustment Gain $\Delta V_{SENSP}/\Delta V_{FBMAX}$	A_{SENSP}	V_{FBPER} = 3.3V		0.535		V/V
		V_{FBPER} = 0V		1.069		V/V
Maximum Feedback Adjustment (compared to SENSP)		V_{FBPER} = 0V, V_{FBMAX} = 1.2V		25		%
Maximum Feedback Adjustment (compared to SENSP)		V_{FBPER} = 3.3V, V_{FBMAX} = 1.2V		12.5		%
FBMAX Maximum Adjustment Threshold				1.2		V
CD0, CD1, FBPER INPUT						
Input Current		V_{PIN} = 5.5V, internal 2MΩ pulldown to GND		2.8	5.6	µA
Logic-High	V_{IH}		1.6			V
Logic-Low	V_{IL}				0.5	V

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB 2.0 HOST CHARGER DETECTION, D+/D-						
Input Logic-High	V_{IH}		2.0			V
Input Logic-Low	V_{IL}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	100	160	µA
Data Detect Voltage High	V_{DAT_REFH}		0.4			V
Data Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data Detect Voltage Hysteresis	V_{DAT_HYST}			55		mV
Data Source Voltage	V_{DAT_SRC}		0.5		0.7	V
Data Source Load Current	I_{DAT_SRC}				200	µA
iPhone/iPad/DCP CHARGER DETECTION						
HVD+/HVD- Short Pulldown	R_{PD}		300	500	750	kΩ
RP1/RP2 Ratio	RT_{RP}		1.485	1.5	1.515	Ratio
RM1/RM2 Ratio	RT_{RM}		0.857	0.866	0.875	Ratio
DM1 Comparator Threshold	V_{DM1F}	iPhone mode, DM falling (in % of V_{BIAS})	45	46	47	%
		iPad mode, DM falling (in % of V_{BIAS})	29	30	31	
DM2 Comparator Threshold	V_{DM2F}	DM falling (in % of V_{BIAS})	6	7	8	%
DP Comparator Threshold	V_{DPR}	iPhone mode, DP rising (in % of V_{BIAS})	45	46	47	%
		iPad mode, DP rising (in % of V_{BIAS})	55.9	57.2	58.5	
DM1 Comparator Debounce Time	t_{DM1}	V_{DM1} step from 2.8V to 1.5V	4	9	15	ms
DM2 Comparator Debounce Time	t_{DM2}	V_{DM2} step from 2.0V to 0.2V	1	2	4	s
DP Comparator Debounce Time	t_{DP}	V_{DP} step from 1.5V to 2.5V	600	1100	1800	µs
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
PWM Output Voltage Accuracy	V_{SENSP}	7V ≤ V_{SUPSW} ≤ 18V, no load, V_{SYNC} = 3.3V or V_{SYNC} = 0V and FPWM mode (see TOC 24)		5.05		V
Skip Mode Output Voltage Accuracy	V_{SENSP_SKIP}	7V ≤ V_{SUPSW} ≤ 18V, no load, V_{SYNC} = 0V, not in FPWM mode (Note 4)	4.96	5.05	5.25	V
Load Regulation		7V ≤ V_{SUPSW} ≤ 18V, 0A < I_{LOAD} < 2.1A, V_{FBMAX} = GND (Note 4)		1.2		%/A
Output Voltage Accuracy	V_{SENSP}	V_{SUPSW} = 16V, I_{LOAD} = 2.1A; V_{FBPER} = 0V, V_{FBMAX} = 1.2V, V_{SYNC} = 0V and FPWM mode (Note 4)	6	6.15	6.3	V
		V_{SUPSW} = 8V, I_{LOAD} = 2.1A; V_{FBPER} = 0V, V_{FBMAX} = 1.2V, V_{SYNC} = 0V and FPWM mode (Note 4)	6	6.15	6.3	
Oscillator Frequency	f_{SW}	R_{FOSC} = 68kΩ	380	440	480	kHz
		R_{FOSC} = 12kΩ	2.0	2.2	2.4	MHz

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spread-Spectrum Range		MAX16984S only		6.5		%
SYNC Switching Threshold Hi	V_{SYNC_HI}	Rising	1.4			V
SYNC Switching Threshold Lo	V_{SYNC_LO}	Falling			0.4	V
SYNC Internal Pulldown				200	550	kΩ
SYNC Input Clock Acquisition Time	t_{SYNC}	(Note 4)		1		Cycle
High-Side Switch On Resistance	R_{ONH}	I_{LX} = 1A		200	450	mI
Low-Side Switch On Resistance	R_{ONL}	I_{LX} = 500mA		1	2	Ω
BST Input Current	I_{BST}	V_{BST} - V_{LX} = 5V, high side on		1.2	2	mA
LX Current-Limit Threshold		Peak Inductor current	2.7	3.6	4.7	A
Skip Mode Peak Current Threshold	I_{SKIP_TH}			300		mA
Negative Current Limit			0.65	0.85	1.1	A
Soft-Start Ramp Time	t_{SS}			9		ms
FAULT OUTPUT						
Output-High Leakage Current		V_{FAULT} = 5.5V	-5		+5	µA
Output Low Level		Sinking 1mA		0.03	0.4	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature				+174		°C
Thermal Shutdown Hysteresis				30		°C
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION (HVD+, HVD-)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap		±25		kV
		ISO 10605 Contact		±8		kV
		IEC 61000-4-2 Air Gap		±15		kV
		IEC 61000-4-2 Contact		±8		kV
		330I, 330pF Air Gap		±15		kV
		330I, 330pF Contact		±8		kV

Note 3: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Note 4: Guaranteed by design and bench characterization; not production tested.

Timing Diagrams

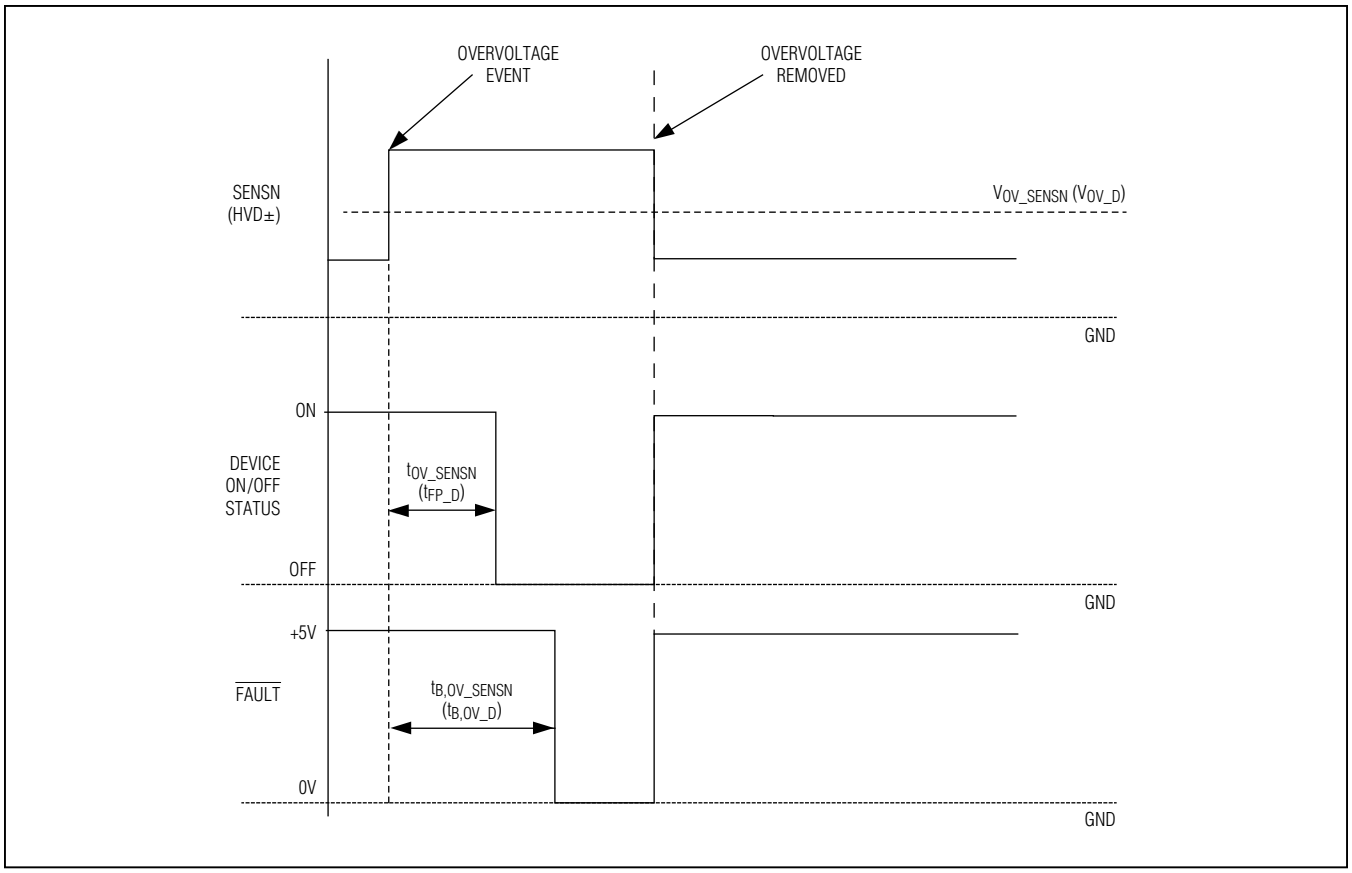


Figure 1. Overvoltage Detection on SENSN, HVD+, HVD- Timing Diagram

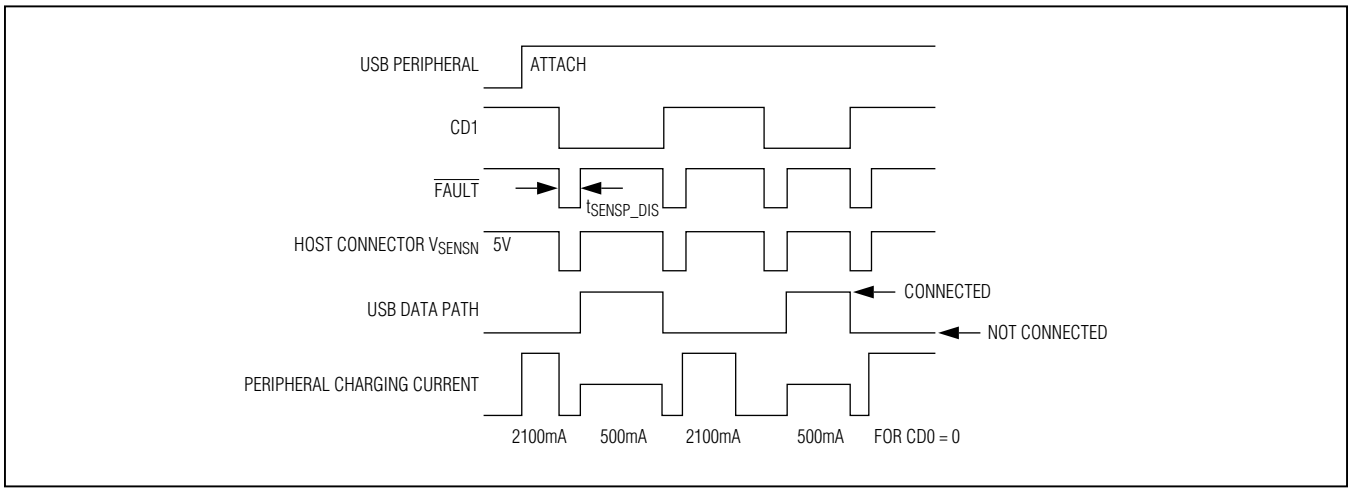


Figure 2. Peripheral Reset Timing Diagram

Timing Diagrams (continued)

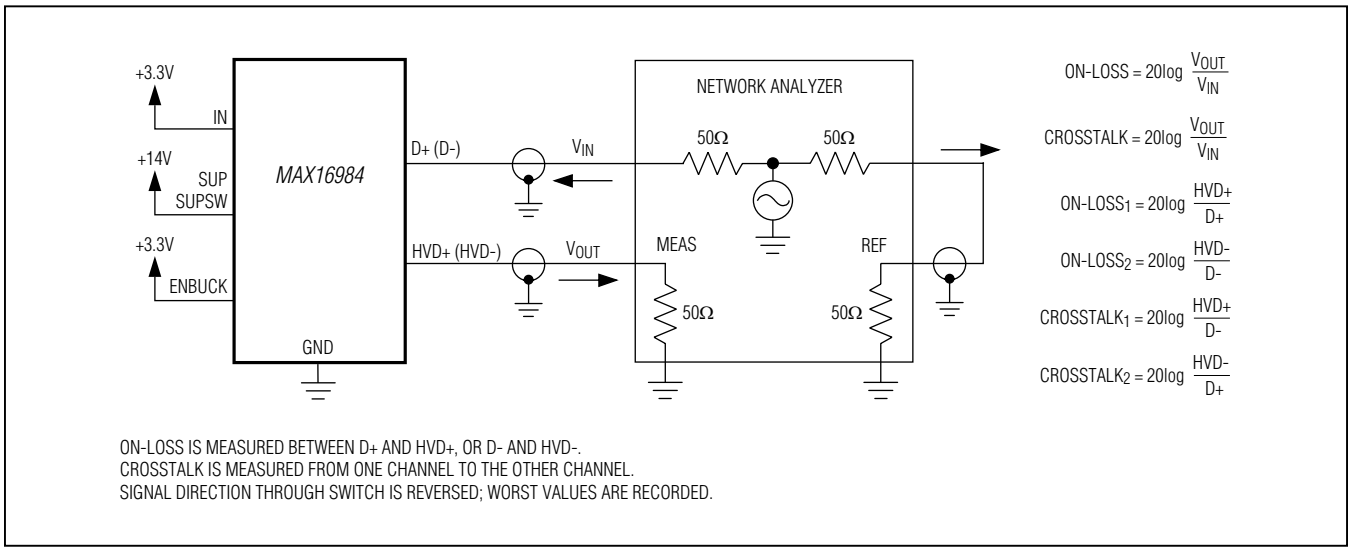


Figure 3. On-Channel -3dB Bandwidth and Crosstalk

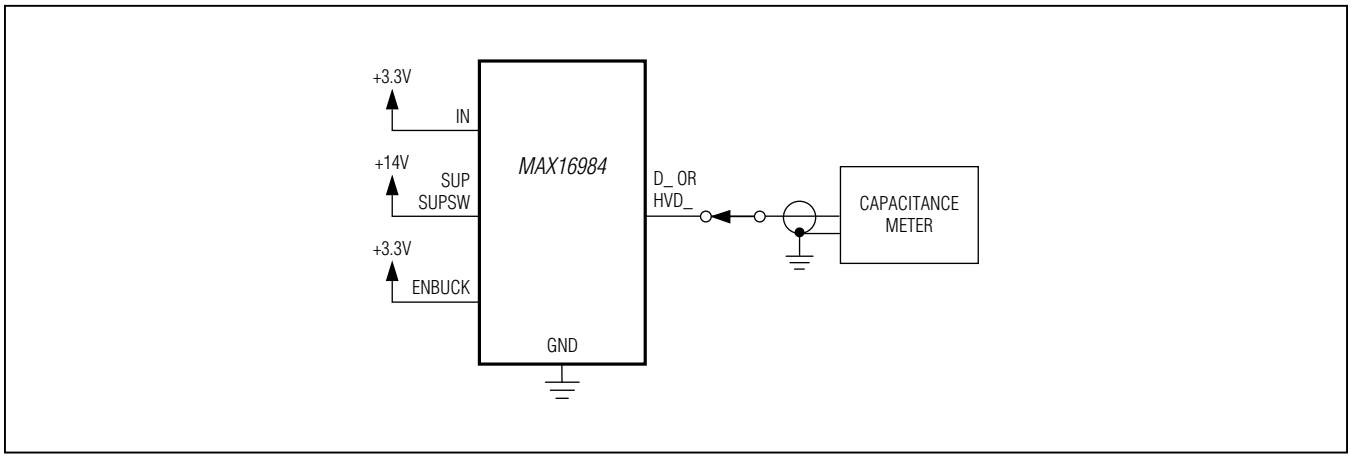


Figure 4. On-Capacitance

Timing Diagrams (continued)

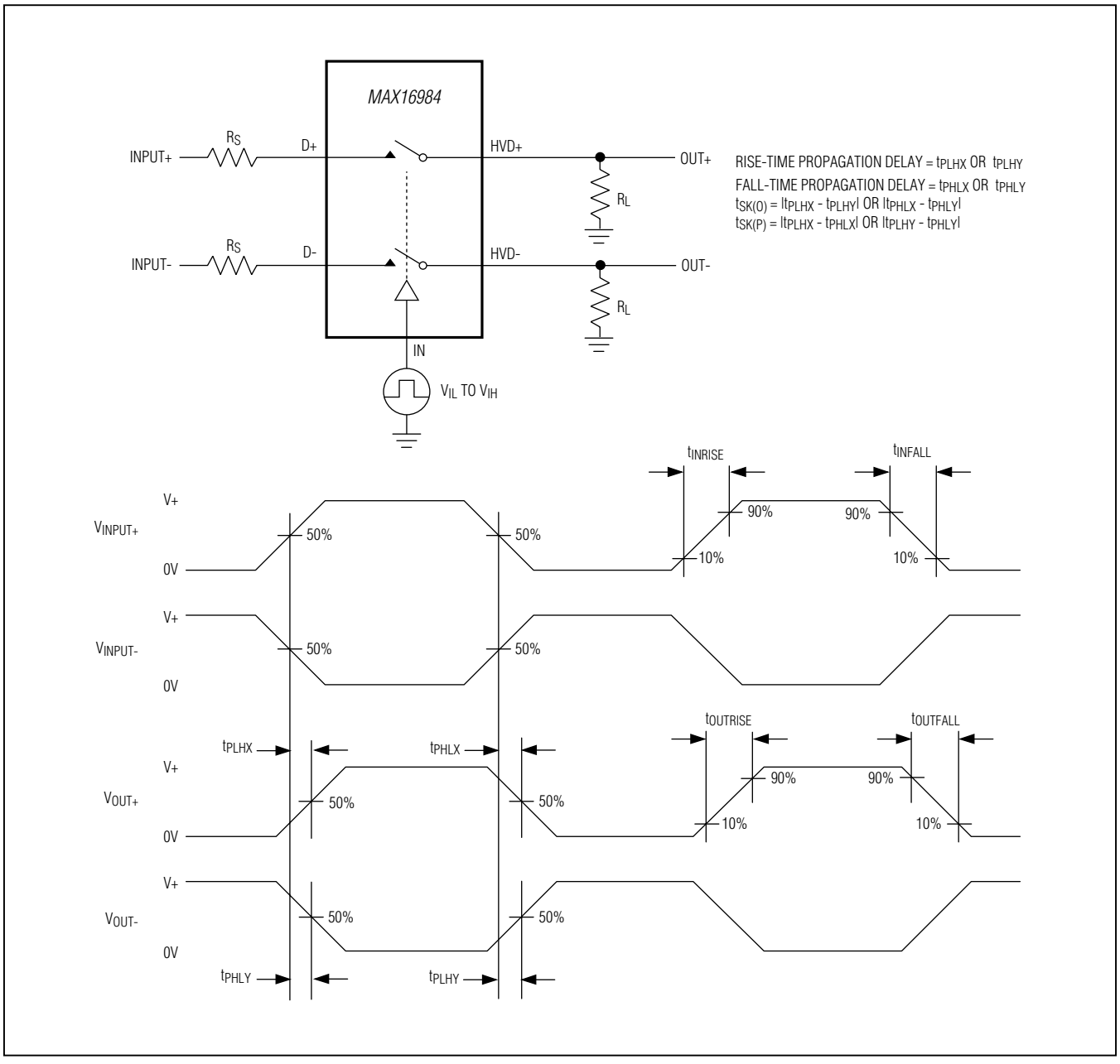
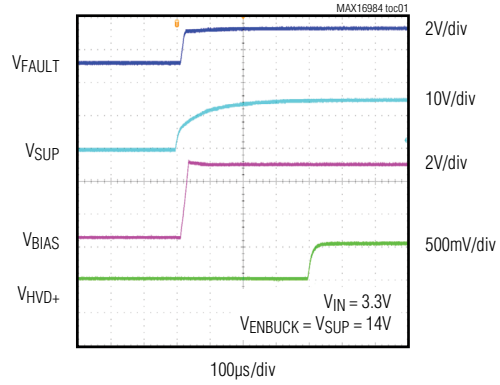


Figure 5. Propagation Delay and Output Skew

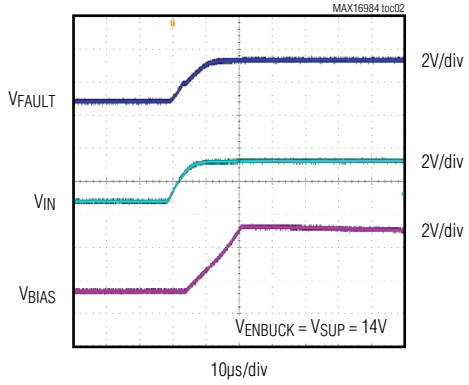
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

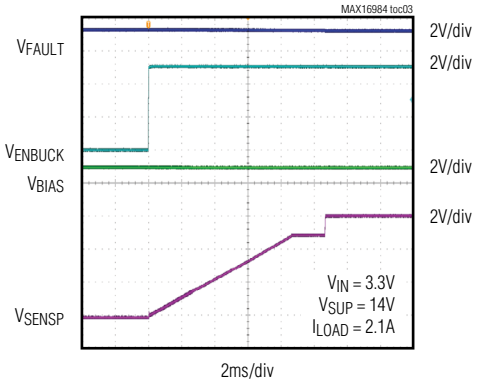
STARTUP
V_{SUP} RISING



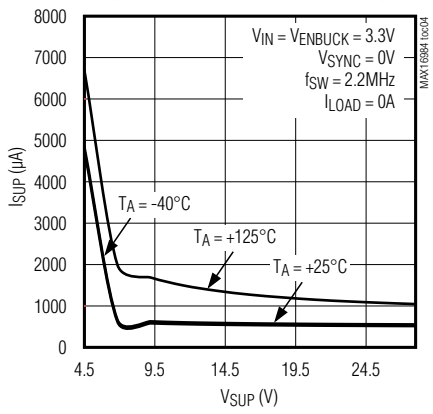
STARTUP
V_{IN} RISING



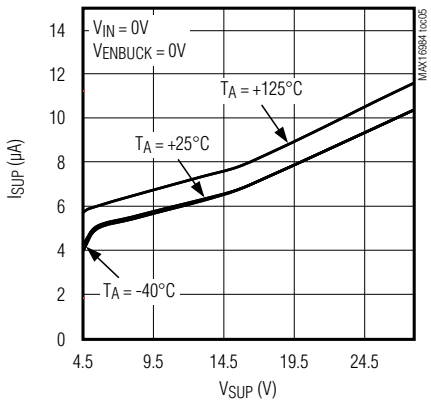
STARTUP
ENBUCK RISING



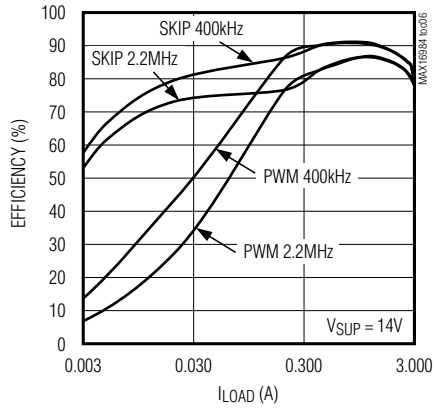
SUPPLY CURRENT vs. VOLTAGE
(SKIP MODE, NO LOAD, 2.2MHz)



SUPPLY CURRENT
vs. VOLTAGE (SHUTDOWN)



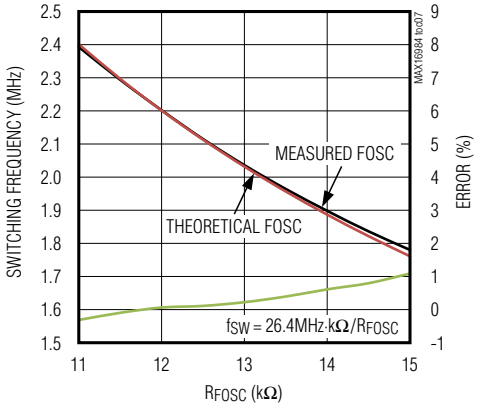
EFFICIENCY vs. LOAD CURRENT



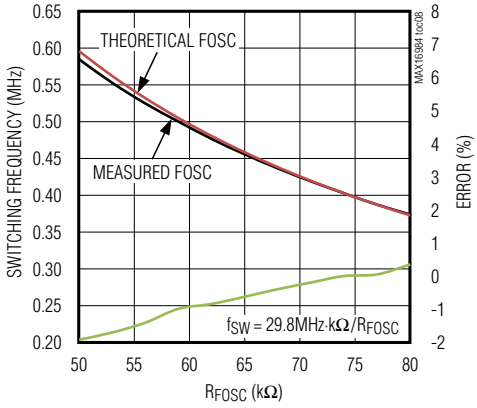
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

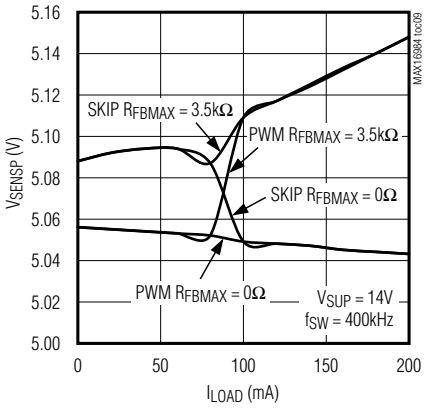
fSW vs. RFOSC



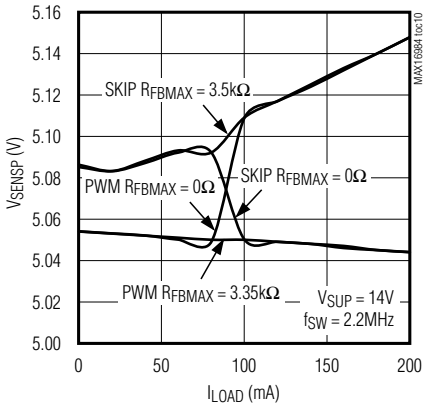
fSW vs. RFOSC



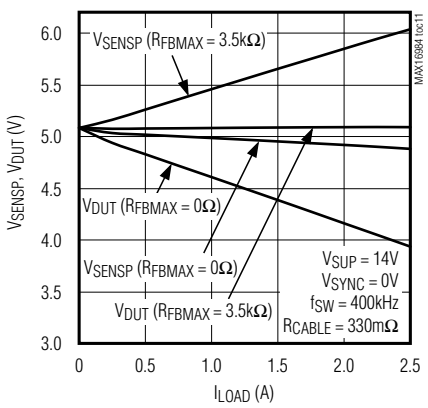
SENSP LOAD REGULATION



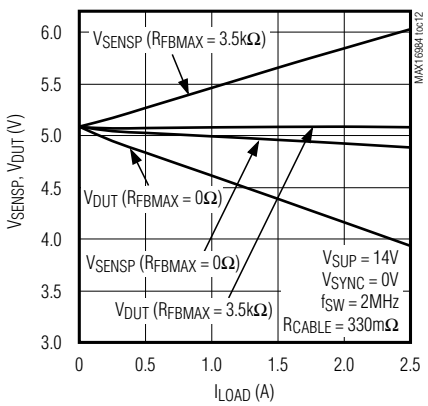
SENSP LOAD REGULATION



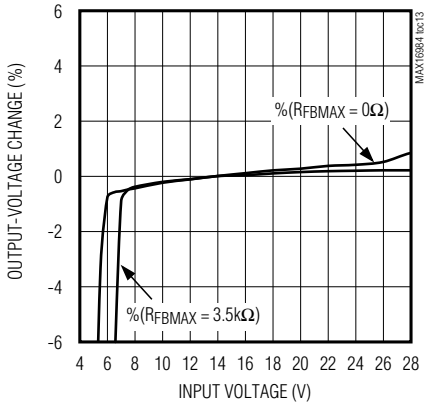
VSENSP, VDUT LOAD REGULATION



VSENSP, VDUT LOAD REGULATION



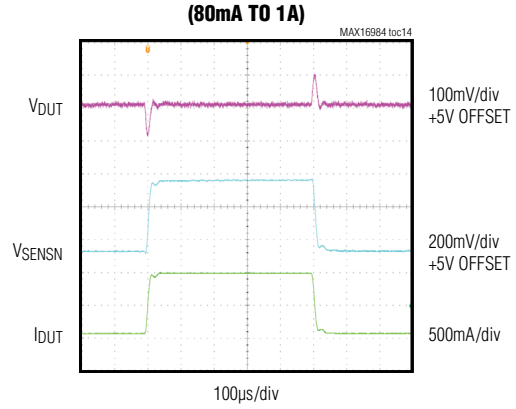
SENSP LINE REGULATION (ILOAD = 2.1A)



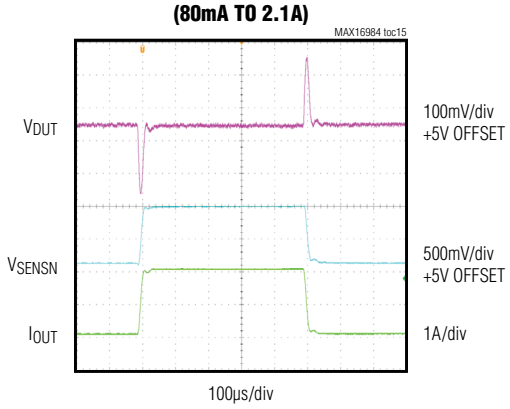
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

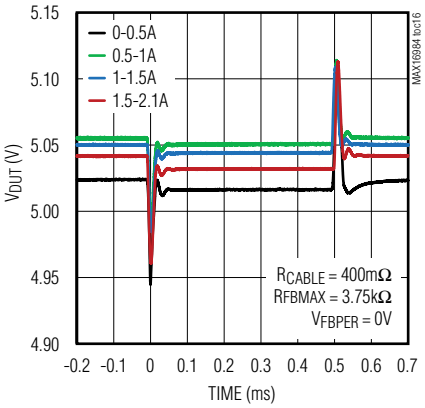
LOAD STEP RESPONSE (80mA TO 1A)



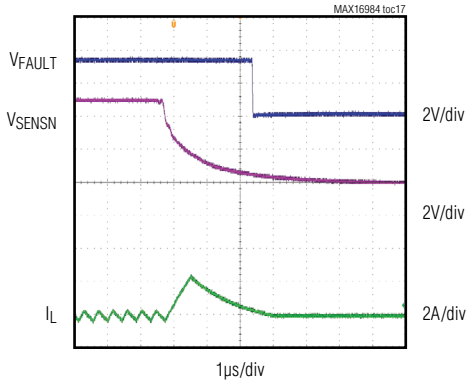
LOAD STEP RESPONSE (80mA TO 2.1A)



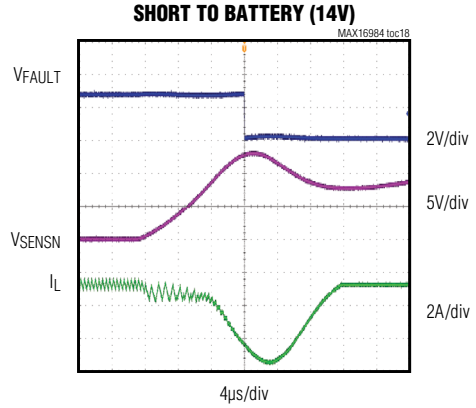
LOAD STEP RESPONSE (END OF CABLE)



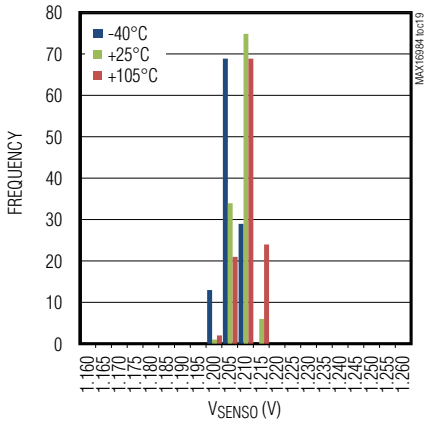
SENSN SHORT TO GND



SENSN SHORT TO BATTERY (14V)



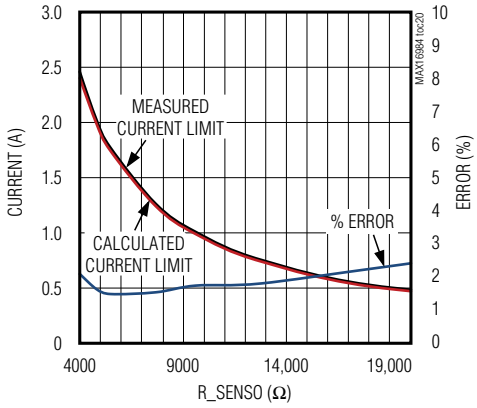
SENSO THRESHOLD RISING



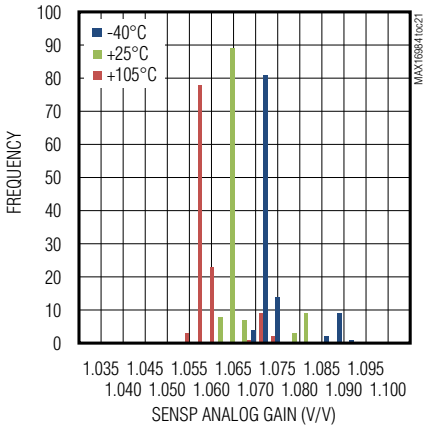
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

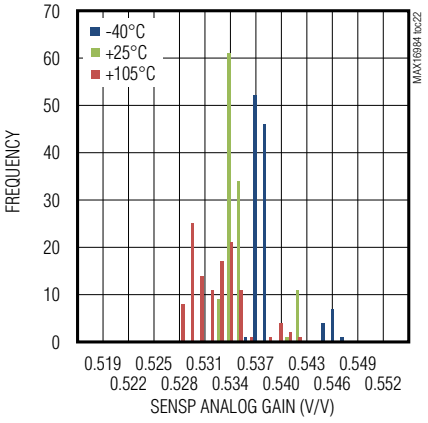
R_SENSO vs. USB CURRENT LIMIT



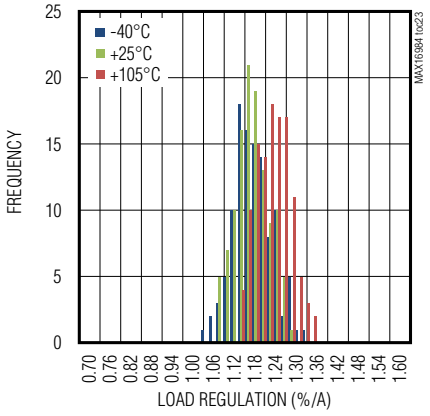
SENSP ANALOG ADJUST GAIN (A_{SENSP})
V_{FBPER} = 0V



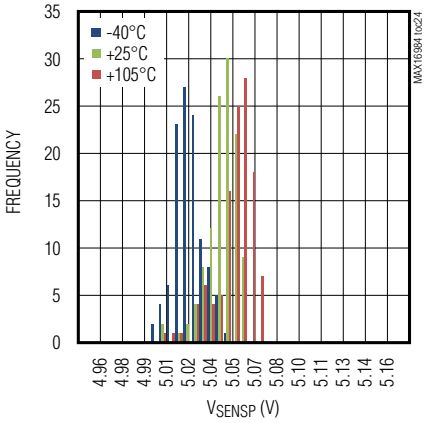
SENSP ANALOG ADJUST GAIN (A_{SENSP})
V_{FBPER} = 3.3V



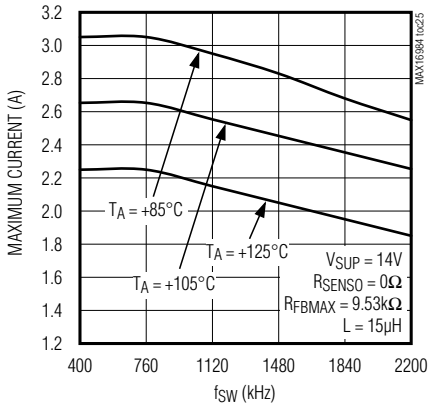
LOAD REGULATION
V_{SUP} = 14V



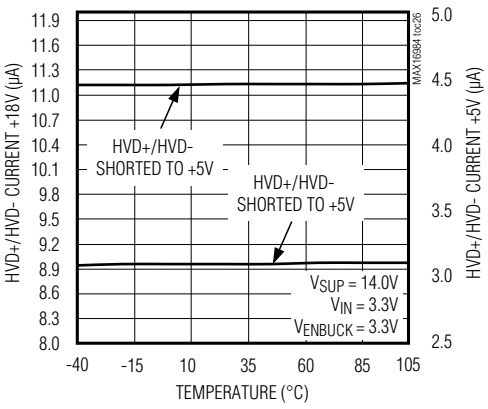
NO-LOAD OUTPUT VOLTAGE (V_{SENSP})
V_{SUP} = 14V



MAXIMUM USB LOAD CURRENT vs. f_{SW}



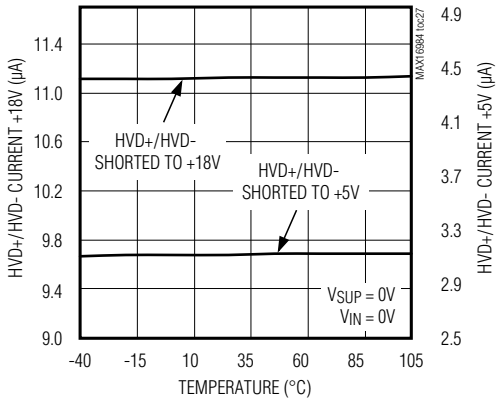
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



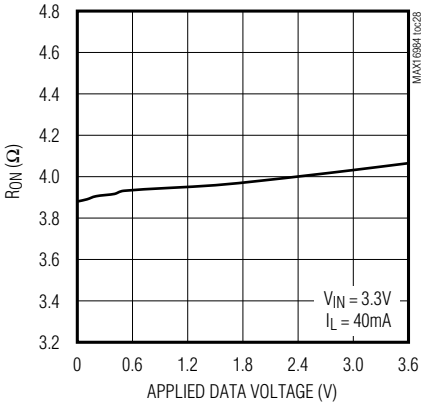
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

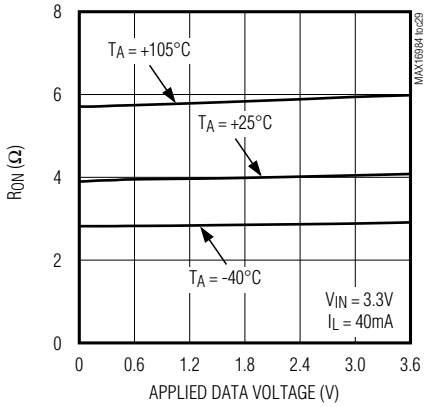
HVD+/HVD- LEAKAGE CURRENT vs. TEMPERATURE



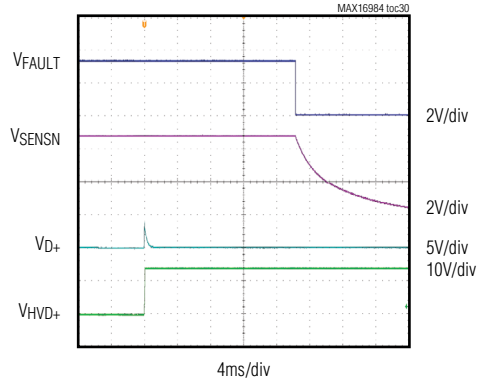
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



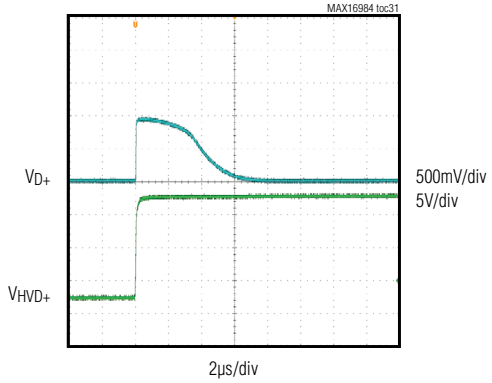
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



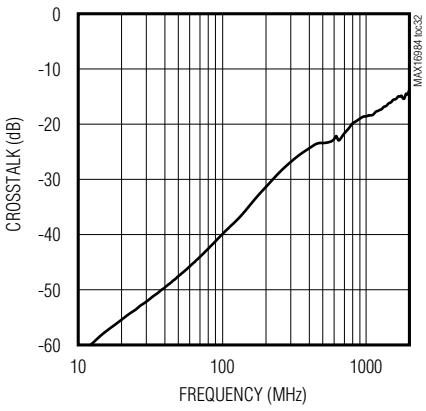
HVD+/HVD- SHORT TO BATTERY (14V) POWERED AND ENABLED



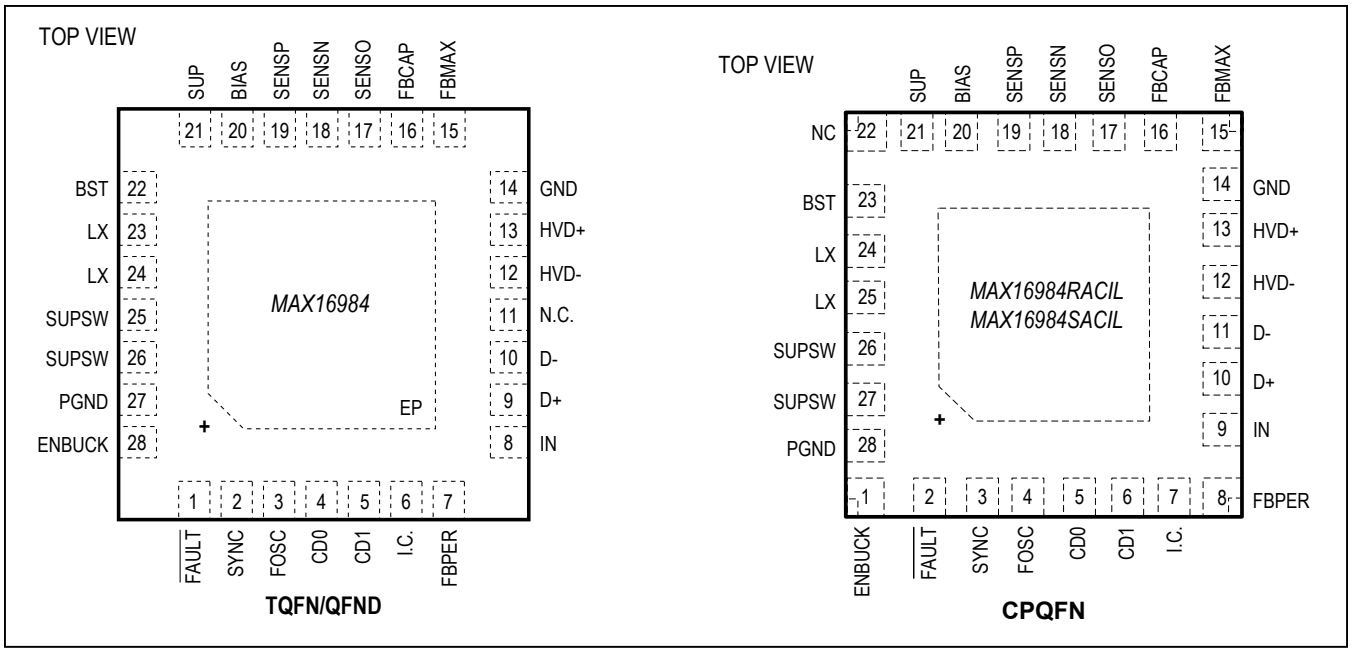
HVD+/HVD- SHORT TO BATTERY (14V) UNPOWERED



CROSSTALK vs. FREQUENCY



Pin Configuration



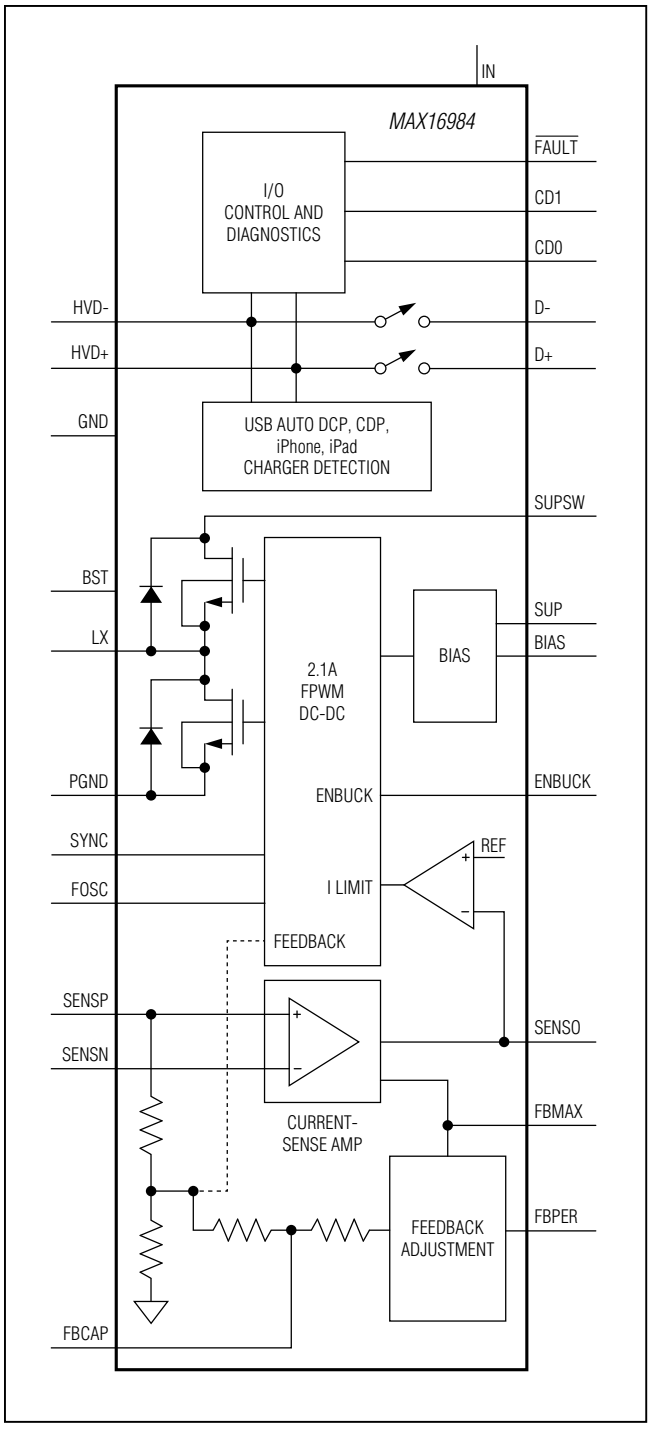
Pin Description

PIN		NAME	FUNCTION
TQFN/ QFND	CPQFN		
1	2	FAULT	Active-Low Open-Drain Fault Indicator Output. Connect a 100kΩ pullup resistor to IN.
2	3	SYNC	Synchronization Input. The device synchronizes to an external signal applied to SYNC. When connected to GND or unconnected, skip mode is allowed under light loads. See Table 1. When connected to a clock source or IN, forced-PWM (FPWM) mode is enabled.
3	4	FOSC	Resistor-Programmable Switching-Frequency Setting Control Input. Connect a resistor from FOSC to GND to set the switching frequency.
4	5	CD0	Charger Detection Configuration Bit 0
5	6	CD1	Charger Detection Configuration Bit 1
6	7	I.C.	Internal Connection. Must be connected to external GND.
7	8	FBPER	Digital Input. Used to select voltage feedback adjustment percentage.
8	9	IN	Logic Enable Input. Connect to I/O voltage of USB transceiver. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 1µF ceramic capacitor from IN to GND.
9	10	D+	USB Differential Data D+ Input. Connect D+ to low-voltage USB transceiver D+ pin.
10	11	D-	USB Differential Data D- Input. Connect D- to low-voltage USB transceiver D- pin.
11	22	N.C.	No Connection

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN/ QFND	CPQFN		
12	12	HVD-	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- directly to the USB connector D- pin.
13	13	HVD+	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ directly to the USB connector D+ pin.
14	14	GND	Analog Ground
15	15	FBMAX	Current-Sense Amp Output. Connect a resistor and capacitor to GND to set the voltage-adjustment bandwidth and the USB DC current level at which maximum voltage-feedback adjustment is reached.
16	16	FBCAP	External Capacitor Connection. Connect a 10pF capacitor to GND.
17	17	SENSO	Current-Sense Amp Output. Connect a resistor and capacitor to GND to set the maximum USB DC current limit.
18	18	SENSN	Current-Sense Amp Negative Input. Connect to negative terminal of current-sense resistor.
19	19	SENSP	DC-DC Converter Feedback Input and Current-Sense Amp Positive Input. Connect to positive terminal of current-sense resistor and the main output of the converter. Used for internal voltage regulation loop.
20	20	BIAS	5V Linear Regulator Output. Connect a 1µF ceramic capacitor from BIAS to GND. BIAS powers up the internal circuitry.
21	21	SUP	Voltage Supply Input. SUP is the supply pin for the internal linear regulator. Connect a minimum of 4.7µF capacitor from SUP to GND close to the IC.
22	23	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
23, 24	24, 25	LX	Inductor Connection. Connect a rectifying Schottky diode between LX and GND. Connect an inductor from LX to the DC-DC converter output (SENSP).
25, 26	26, 27	SUPSW	Internal High-Side Switch-Supply Input. SUPSW provides power to the internal switch. Connect a 4.7µF ceramic capacitor in parallel with a 47µF capacitor from SUPSW to PGND. See the *DC-DC Input Capacitor Selection* section.
27	28	PGND	Power Ground
28	1	ENBUCK	Battery-Compatible Enable Input. Drive ENBUCK low/high to disable/enable the switching regulator.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Functional Diagram



Detailed Description

The MAX16984 combines a 5V/2.1A automotive grade step-down converter, a USB host charger adapter emulator, and USB protection switches. It is designed for high-power USB ports in automotive radio, navigation, connectivity, and USB hub applications.

The USB protection switches provide high-ESD and short-circuit protection for the low-voltage internal data lines of the multimedia processor's USB transceiver and support USB Hi-Speed (480Mbps) and USB Full-Speed (12Mbps) pass-through operation. The MAX16984 features integrated host-charger port-detection circuitry adhering to the USB 2.0 Battery Charging Specification BC1.2 and also includes dedicated bias resistors for iPod/iPhone 1.0A and iPad 2.1A dedicated charging modes.

The high-efficiency step-down DC-DC converter operates from a voltage up to 28V and is protected from load-dump transients up to 42V. The device includes resistor-programmable frequency selection from 220kHz to 2.2MHz to allow optimization of efficiency, noise, and board space based on the application requirements. The converter can deliver up to 2.1A of continuous current at 105°C.

The MAX16984 also includes a high-side current-sense amplifier and configurable feedback-adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications.

Power-Up and Enabling

System Enable (IN)

IN is used as the main enable to the MAX16984 and is also used to clamp the D+ and D- pins during an ESD and short-to-battery on the HVD+ and HVD- pins. This clamping protects the downstream USB transceiver. The IN pin contains an overvoltage lockout that disables the data switches if IN is above V_{IN_OVLO}. Bypass IN with a 1FF capacitor and connect it to the same 3.3V supply as shared with the multimedia processor's USB transceiver. If IN is logic-high, the protection switches are enabled and the USB switches operate in one of four modes per the CD0 and CD1 inputs. If IN is at a logic-low level, SUP power consumption is reduced and the device enters a standby low-quiescent level.

Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal circuitry for the MAX16984. BIAS is internally powered from SUP and automatically powers up when IN is high and V_{SUP} exceeds approximately 2.7V. The BIAS output contains an under voltage lockout that keeps the internal circuitry disabled when BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when IN is low and a low 6µA (typ) shutdown current mode is entered. Bypass BIAS to GND with a 1µF ceramic capacitor.

DC-DC Enable (ENBUCK)

The buck regulator on MAX16984 is activated by driving ENBUCK high and disabled by driving ENBUCK low. ENBUCK is compatible with inputs from automotive battery level down to 3.3V. Connect ENBUCK to the enable output of the USB transceiver controller in a typical application. This allows the USB controller to enable and disable the USB power port via software commands (see the *Functional Diagram*). ENBUCK can be directly connected to SUP for dedicated USB power port applications that do not have the USB transceiver controlling ENBUCK.

Power-On Sequence

For typical radio and navigation applications, the SUP and SUPSW are connected together and connected to the vehicle battery. SUP and IN have no power-up sequence requirements, however, IN is typically enabled after SUP.

Step-Down DC-DC Regulator

Step-Down Regulator

The switching regulator is a high input voltage, constant-frequency, current-mode step-down DC-DC converter delivering output current up to 2.1A. The converter has an internal high-side n-channel switch and uses a low forward-drop freewheeling Schottky diode for rectification. There is a small low-side n-channel switch to maintain fixed frequency under light loads. For lower quiescent current operation requirements, the low-side n-channel switch can be disabled to allow skip mode operation under light loads.

Wide Input Voltage Range

The device includes two separate supply inputs, SUP and SUPSW, specified for a wide 4.5V to 28V input voltage range. SUP provides power to the internal BIAS linear regulator, and SUPSW provides power to the internal power switch. Certain conditions such as cold crank can cause the voltage at output to drop below the programmed output voltage of 5.05V. As the input voltage approaches the output voltage, the device enters dropout and the effective duty cycle of the high-side FET approaches 97%. When the switching regulator is in dropout, the switching frequency is reduced.

Output Voltage (SENSP)

The MAX16984 has a precision internal feedback network connected to SENSP that is used to set the output voltage of the DC-DC converter. The network nominally sets the average DC-DC converter output voltage to 5.05V when in forced-PWM (FPWM) operation and to 5.09V when operating in skip mode.

Soft-Start

When the DC-DC converter is enabled, the regulator soft-starts by gradually ramping up the output voltage from 0 to 5.05V in approximately 9ms. This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads (see the *USB Loads* section).

Switching Frequency (FOSC, SYNC)

The MAX16984 DC-DC switching frequency can be set by either its internal oscillator or by synchronization to an external clock on the SYNC pin. The internal oscillator frequency (f_{SW}) is set by a resistor connected from FOSC to GND (see the *Applications Information* section). When operating from its internal oscillator and at no load, the MAX16984 can be operated in FPWM mode or is allowed to enter skip mode operation. See Table 1. When syncing to an external clock, duty cycle must be between 40% and 60%, clock input frequency must be within ±20% of the resistor-set frequency, and frequency cannot exceed 2.3MHz.

Forced-PWM Operation

While operating from a clocked signal on the SYNC pin, the MAX16984 is in FPWM mode operation at all times. While operating from its internal oscillator, FPWM operation can be entered by connecting the SYNC logic-high. The MAX16984 maintains fixed-frequency PWM operation over all load conditions with the SYNC pin logic-high or being clocked by an external clock source. Additionally, the MAX16984 can intelligently enter FPWM mode and exit skip mode (Table 1) if a portable device is plugged in by determining if the portable device is actively consuming more than 4% of the programmed current limit on SENSO (see the *Current Limit* section).

Table 1. DC-DC Converter Forced-PWM Mode and Skip Mode Operation Truth Table

SYNC	CD1	CD0	CDP DETECTION	USB LOAD CURRENT	DCP DETECTION	DC-DC CONVERTER OPERATION
1	X	X	X	X	X	FPWM Mode: Continuous
0	X	X	X	V_{SENSO} < 48mV	X	Allow Skip Mode: No USB load detected
0	X	X	X	V_{SENSO} > 48mV	X	FPWM Mode: USB load detected
0	0	1	(HVD+ or HVD-) > V_{IH}	X	X	FPWM Mode: USB device connected to port
0	0	1	(HVD+ and HVD-) < V_{IL}	V_{SENSO} < 48mV	X	Allow Skip Mode: USB device not connected to port
0	1	X	X	V_{SENSO} < 48mV	(HVD- > V_{DM1F}) & (HVD+ < V_{DPR})	Allow Skip Mode: No USB load detected
0	1	X	X	V_{SENSO} > 48mV	(HVD- > V_{DM1F}) & (HVD+ < V_{DPR})	FPWM Mode: USB load detected
0	1	X	X	X	(HVD- > V_{DM1F}) & (HVD+ > V_{DPR})	FPWM Mode: USB device detected
0	1	X	X	X	(HVD- < V_{DM1F})	FPWM Mode: USB device detected

Intelligent Skip Mode Operation

If the SYNC pin is logic-low, the MAX16984 is allowed to leave FPWM mode and enter skip mode operation (Table 1). While in skip mode, the high-side FET is turned on until the current in the inductor is ramped up to 300mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1.2V typ). At this point, both the high-side and low-side FETs are turned off. Depending on the choice of the output capacitor and the load current, the high-side FET turns on again when SENSP drops below 5.05V (typ).

Spread-Spectrum Option

Spread spectrum is offered to improve EMI performance of the MAX16984. The MAX16984S has an integrated spread-spectrum oscillator, and the internal operating frequency modulates up to ±3.25% relative to the internally generated operating frequency, resulting in a total spread-spectrum range of 6.5%. The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the MAX16984 is running with internally generated switching frequency.

Current Limit

The MAX16984 limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter and a user-configurable external USB load current-sense amplifier threshold (see the *Current-Sense Output (SENSO)* section). This allows the current limit to be adjusted between 500mA and 2.1A, depending on the application requirements, and protects the DC-DC converter in the event of a fault. Upon exceeding either the internal or user-programmable current-limit thresholds, the high-side FET is immediately turned off and current-limit algorithms are initiated. When the external current limit lasts for longer than 16.5ms, $\overline{FAULT}$ asserts. If both the USB current limit is detected and the output voltage exceeds 4.75V for longer than 16.5ms, the DC-DC converter resets. If the internal peak current threshold is exceeded for four consecutive cycles and the output voltage is less than 2.0V, the high-side FET is turned off for 16ms to allow the inductor current to discharge and a soft-start sequence is then initiated.

Output Short-Circuit Protection

The output of the DC-DC converter (SENSP, SENSN) is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage is encountered on SENSP, the device is disabled for 16ms (typ) and then reattempts soft-start. This pattern repeats until the short circuit has been removed.

If a short-to-battery is encountered (V_{SENSN} > $V_{OV-SENSN}$), the device stops switching and the $\overline{FAULT}$ pin is asserted after 8µs. The host system should monitor the $\overline{FAULT}$ output and disable the ENBUCK if multiple $\overline{FAULT}$ events occur to minimize operating current.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the MAX16984. A thermal-protection circuit monitors the die temperature. If the die temperature exceeds +174°C, the device shuts down, allowing it to cool. Once the device has cooled by 30°C, the device is enabled again. This results in a pulsed output during continuous thermal-overload conditions. The thermal-overload protection protects the device in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C.

USB Current Limit and Captive Cable-Voltage Adjustment

Current-Sense Amplifier (SENSP, SENSN)

The MAX16984 features an internal USB load current-sense amplifier to monitor the load current being pulled by the USB port. The (V_{SENSP} - V_{SENSN}) voltage sets an output current at both SENSO and FBMAX equal to 2.5mA/V. Choose a sense resistor from SENSP to SENSN to limit the differential voltage across SENSP-SENSN to 120mV.

Current-Sense Output (SENSO)

A resistor to ground on the SENSO pin results in a voltage representing the USB load current. Upon crossing the fixed internal threshold of 1.2V, the high-side FET is immediately turned off, the low-side FET is turned on, and the USB load current is reduced until the voltage at SENSO falls below the 1.2V threshold. If the load current exceeds the USB current limit for longer than 16.5ms, a $\overline{FAULT}$ is asserted. For proper functionality, limit the voltage at SENSO to 2.0V.

Current Feedback Adjustment

The MAX16984 has multiple user-configurable features to adjust the DC-DC converter output voltage higher to help overcome voltage drops associated with captive cables in automotive applications. The feature set allows for the user to set the maximum amount the voltage can be raised and set the desired operating bandwidth of the adjustment.

Feedback Percentage (FBPER)

The FBPER pin allows the user to set the maximum allowable percentage to either +25% (V_{FBPER} = 0V) or +12.5% (V_{FBPER} = 3.3V). Set the FBPER pin such that the percentage of voltage adjustment needed is minimized for the application in the event of a fault.

Maximum Feedback Adjustment (FBMAX)

A resistor to ground on the FBMAX pin results in a voltage representing the USB load current. The output voltage of the DC-DC converter increases linearly as the voltage at FBMAX increases up to 1.2V to maintain voltage at the portable device (V_{DUT}) that meets USB specification. Upon crossing the fixed internal threshold of 1.2V, the DC-DC output voltage remains unchanged. For proper functionality, limit the voltage at FBMAX to 2.0V. A capacitor to GND is also needed on the FBMAX pin to limit the bandwidth of the feedback adjustment. See Figure 6.

USB Protection Switches

HVD+ and HVD- Protection

The MAX16984 provides automotive grade ESD and short-circuit protection for the low-voltage internal USB data lines of high-integration multimedia processors. HVD+/HVD- protection consists of ESD and OVP (overvoltage protection) for both 12Mbps and 480Mbps USB transceiver applications. This is accomplished with an extremely low-capacitance, high-voltage FET in series with the D+ and D- data paths.

No external ESD protection diodes are required when using the MAX16984. The HVD+ and HVD- ESD protection features include protection to ±15kV Air/±8kV Contact on the HVD+ and HVD- outputs to the IEC 61000-4-2 model and 330Ω, 330pF ESD model.

The HVD+ and HVD- short-circuit protection features include short to +18V battery as well as short to +5V on the protected HVD+ and HVD- outputs. This is provided to protect against shorted conditions in the vehicle harness and prevent damage to the low-voltage USB transceiver. Short-to-GND protection is provided by the upstream USB transceiver.

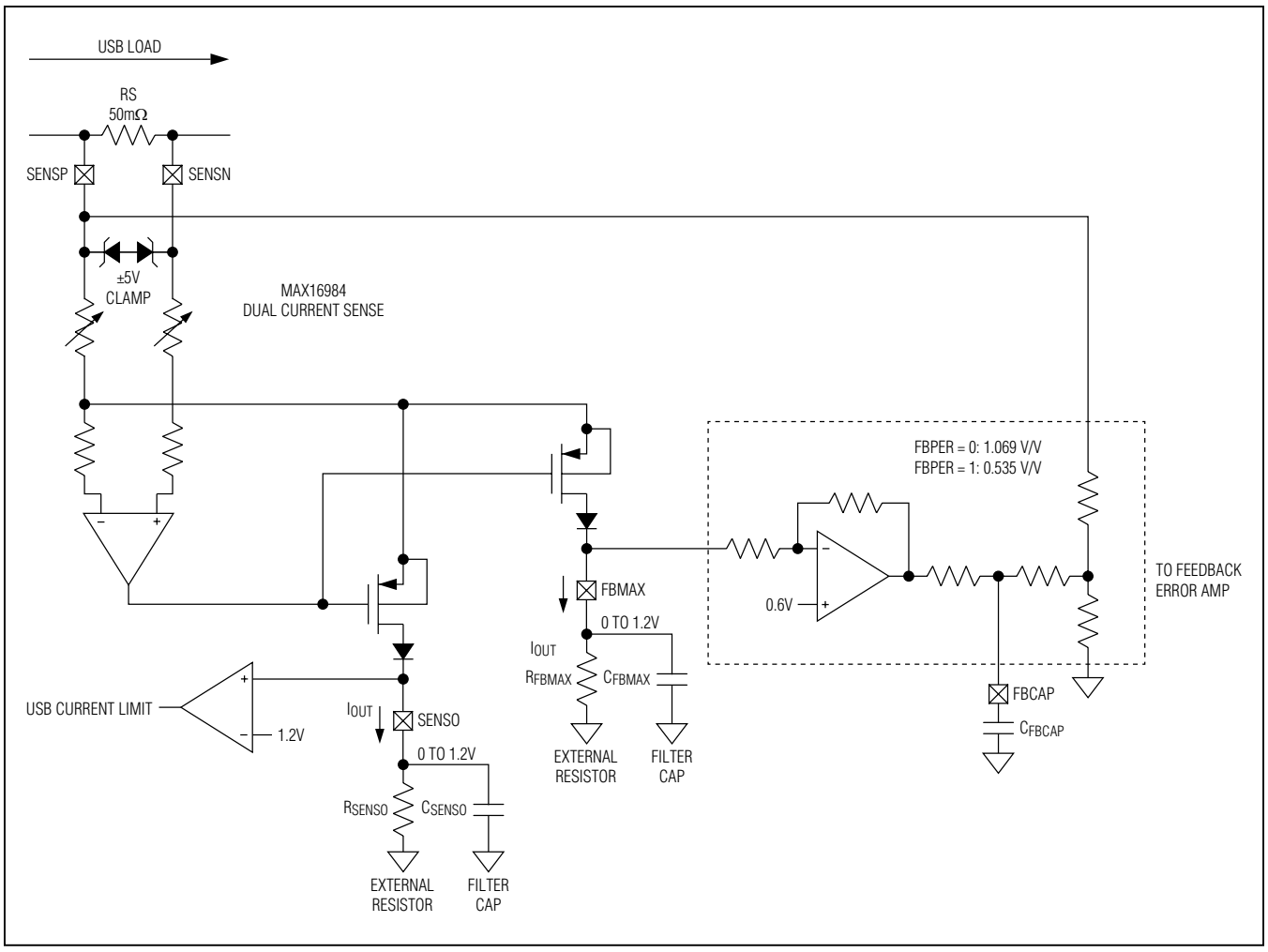


Figure 6. USB Current-Sense Amplifier, USB Current Limit, and USB Voltage Feedback Adjustment

USB Host Adapter Emulator

The Hi-Speed USB protection switches integrate the latest USB-IF Battery Charging Specification Revision 1.2 CDP and DCP circuitry, both the 1.0A and 2.1A resistor bias options for Apple-compliant devices, and the industry legacy USB D+ short to D- charge detection using data line pullup.

HVD+ and HVD- Operation (CD1, CD0)

The MAX16984 features dual digital inputs, CD1 and CD0, for mode selection of the HVD+ and HVD- pins (Table 2). Connect CD1/CD0 to a logic-level low for normal USB Hi-Speed (HS) pass-through mode. Connect CD1/CD0 to a logic-level low/high for USB low-speed (LS) and USB full-speed (FS) data transmission and charging downstream port (CDP) mode. See Table 1 for CDP mode and Figure 7 for a detailed description of all modes.

Hi-Speed Pass-Through Mode (CD1/CD0 = low/low)

HS pass-through mode provides true pass-through operation for USB HS (480Mbps) data signals and disables the CDP circuitry. Place the device into this mode when the USB transceiver requests to enter HS mode. See Table 2.

Table 2. Data Switch Mode Truth Table

DEVICE INPUTS			INTERNAL LOGIC				DATA SWITCH MODE
IN	CD1	CD0	SA	SB	ENAUTO	ENHOST	
0	X	X	X	X	X	X	Off
1	0	0	1	0	0	0	HS Pass-Through
1	0	1	1	0	0	1	FS/LS with CDP
1	1	0	0	1	1	0	DCP/Apple 2.1A with Auto Detection
1	1	1	0	1	1	0	DCP/Apple 1.0A with Auto Detection

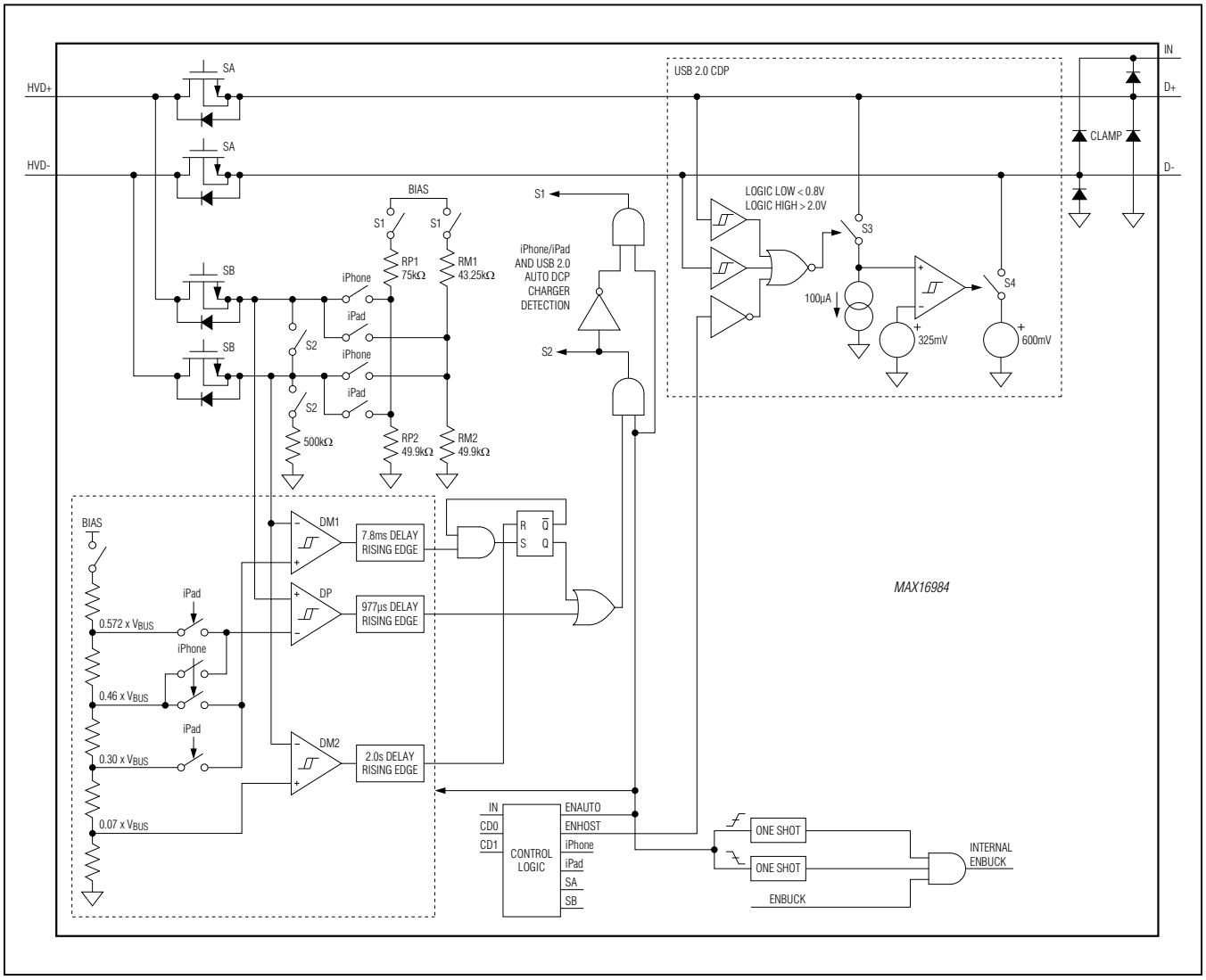


Figure 7. Data Switches and Host Adapter Emulator

Low-Speed/Full-Speed Mode with Charging Downstream Port (CD1/CD0 = low/high)

After a USB-compliant portable device detects V_{BUS}, it is allowed to check if the host device is a CDP by applying a voltage to HVD+ and checking the voltage on HVD-. At this time, it is assumed that HVD+ and HVD- are logic-low, which means that the voltage is less than 0.8V. Then the port-detection circuit is enabled and switch 3 is on (Figure 7). The portable device then drives HVD+ to 0.6V (typ). The comparator closes switch 4 and the HVD- line is then driven to 0.6V (typ). The portable device can now detect that it is connected to a charging port.

When an FS device connects, it pulls the HVD+ line logic-high to a voltage greater than 2V. Then switch 3 opens, the positive input of the comparator is forced to zero, and switch 4 is also opened. Because HVD- is low, the portable device detects that it is connected to a CDP.

When a LS device connects, it pulls the HVD- line logic-high (after it has stopped driving HVD+ to 0.6V). Because HVD+ stays low, the portable device detects that it is connected to a CDP.

When the portable device has connected in LS or FS mode, either D+ or D- is logic-high upon enumeration, which disables the charger-detect circuit. A delay is implemented that closes switch 3 after HVD+ and HVD- are logic-low longer than 100µs. This ensures that switch 3 stays off when the logic-high states of D+ and D- do not overlap.

If a Hi-Speed-capable device connects to the port and CD1/CD0 = low/high, it can detect that it is connected to a CDP. Upon enumeration, and before entering HS mode, the host system microprocessor must query the USB transceiver to determine if HS mode is needed. If so, it must drive the CD0 input low to disable the port-detection circuit and enter USB HS mode. The host system microprocessor must also query the USB transceiver to detect when the HS portable device is disconnected or no longer in HS mode. Once detected, it must drive the CD0 input high to re-enable the port-detection circuit for the next connection sequence. This is needed as the HS differential logic levels on HVD+ and HVD- are below 500mV.

USB-IF Dedicated Charging Port and Apple 2.1A with Auto Detection (CD1/CD0 = high/low)

The MAX16984 features an iPad/DCP auto-detection mode for emulating dedicated iPad 2.1A charging and USB-IF DCPs. CD1/CD0 must be set high/low to activate iPad/DCP auto-detection mode. In this mode, the high-voltage-protected HVD+ and HVD- pins are disconnected from the low-voltage D+ and D- pins and are initially connected to internal resistor-dividers to provide the proper Apple-compliant iPad bias voltage. Data switches SA are opened and switches SB are closed (Figure 7). Initially, the iPad termination resistors are presented on the HVD+/- pins, the MAX16984 then monitors the voltages at HVD+ and HVD- to determine the type of device attached.

If the voltage at HVD- is +1.5V (typ) (V_{BUS} x 0.3) or higher, and the voltage at HVD+ is +2.86V (typ) (V_{BUS} x 0.572) or lower, the state remains unchanged and the iPad termination resistors remain present.

If the voltage at HVD- is forced below the +1.5V (typ) (V_{BIAS} x 0.3) threshold or if the voltage at HVD+ is forced higher than the +2.86V (typ) (V_{BIAS} x 0.572) threshold, the internal switch disconnects HVD- and HVD+ from the resistor-divider (iPad switch open) and HVD+ and HVD- are shorted together for dedicated charging mode (S2 closed).

Once the charging voltage is removed, the short between HVD+ and HVD- is disconnected and the operation is restarted with the internal resistor-divider bias voltages appearing on HVD+ and HVD-.

USB-IF Dedicated Charging Port and Apple 1A with Auto Detection (CD1/CD0 = high/high)

The MAX16984 features an iPhone/DCP auto-detection mode for emulating dedicated iPhone 1.0A charging and USB-IF DCPs. CD1/CD0 must be set high/high to activate iPhone/DCP auto-detection mode. In this mode, the high-voltage-protected HVD+ and HVD- pins are disconnected from the low-voltage D+ and D- pins and are initially connected to internal resistor-dividers to provide the proper Apple-compliant iPhone bias voltage. Data switches SA are opened and switches SB are closed (Figure 7). Initially, the iPhone termination resistors are presented on the HVD+/- pins. The MAX16984 then monitors the voltages at HVD+ and HVD- to determine the type of the device attached.

If the voltage at HVD- is +2.3V (typ) (V_{BIAS} x 0.46) or higher, and the voltage at HVD+ is +2.3V (typ) or lower, the state remains unchanged and the iPhone termination resistors remain present. If the voltage at HVD- is forced below the +2.3V (typ) threshold, or if the voltage at HVD+ is forced higher than the +2.3V (typ) threshold, the internal switch disconnects HVD- and HVD+ from the resistor-divider (iPhone switch open) and HVD+ and HVD- are shorted together for dedicated charging mode (S2 closed). Once the charging voltage is removed, the short between HVD+ and HVD- is disconnected and the operation is restarted with the internal resistor-divider bias voltages appearing on HVD+ and HVD-.

Fault Output ($\overline{FAULT}$)

The MAX16984 features an open-drain, active low $\overline{FAULT}$ output. Table 3 summarizes the conditions that generate a fault and actions taken by the MAX16984. The output remains asserted until the fault condition is removed. The MAX16984 is designed to eliminate false $\overline{FAULT}$ reporting by using an internal deglitch, fault blanking, timer. This ensures $\overline{FAULT}$ is not accidentally asserted during normal operation such as starting into heavy capacitive loads.

Applications Information

DC-DC Switching-Frequency Selection

The switching frequency (f_{SW}) for the MAX16984 is resistor programmable by connecting resistor (R_{FOSC}) from FOSC to GND. Select the correct R_{FOSC} value for the desired switching frequency. For operation between 1.8MHz and 2.2MHz: f_{SW} [MHz] = 26.4/R_{FOSC}, and for operation between 220kHz and 500kHz: f_{SW} [MHz] = 29.8/R_{FOSC}, where R_{FOSC} is in kΩ. For example, a 2.2MHz switching frequency is set with R_{FOSC} = 12kΩ. Higher switching frequencies allow for smaller PCB area designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase. Operation between 500kHz and 1.8MHz is not recommended to avoid AM band interference.

DC-DC Input Capacitor Selection

The MAX16984 has two main power supply pins to support multiple power architectures. Bypass SUP with a 4.7FF ceramic capacitor to GND for proper operation of the internal BIAS linear regulator. The selection of the input filter capacitor from SUPSW to PGND reduces the peak currents drawn from the upstream power source and reduces noise and voltage ripple on the input caused by the circuits switching. The input capacitor RMS current rating requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{SENSP}(V_{SUPSW} - V_{SENSP})}}{V_{SUPSW}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{SUPSW} = 2V_{SENSP}), so $I_{RMS(MAX)}$ = $I_{LOAD(MAX)}$/2.

Table 3. Fault Conditions

EVENT	ACTION TAKEN
Thermal Fault	• If the device is over the thermal limit, the step-down DC-DC regulator is disabled immediately and $\overline{FAULT}$ goes low. • When the thermal fault is removed, the fault is cleared immediately and $\overline{FAULT}$ goes high. • After the fault is removed, the soft starts begins
Overvoltage on Pins (HVD+, HVD-, IN)	• An overvoltage at one of these pins immediately switches off all power and data switches. The step-down DC-DC regulator turns off and the blanking timer turns on. • If overvoltage persists for 18ms or longer, $\overline{FAULT}$ goes low. • When the overvoltage is removed, the fault is cleared immediately and $\overline{FAULT}$ goes high. • After the fault is removed, the soft starts begins.
Undervoltage on BIAS	• A BIAS UVLO immediately switches off all power and data switches and resets the digital logic. • During BIAS UVLO, $\overline{FAULT}$ is high impedance.
Undervoltage on SENSP or Overcurrent	• If SENSP is less than 4.75V for more than 10ms, $\overline{FAULT}$ goes low. • If USB current limit is high for more than 16.5ms, $\overline{FAULT}$ goes low. • If USB current limit is high and SENSP is less than 4.75V for more than 16.5ms, the step-down DC-DC regulator will reset for 16ms then try to start up again. • If the USB current limit is high and if SENSP is less than 2V, $\overline{FAULT}$ goes low and the part resets. • If the step-down DC-DC regulator high-side current limit is high for 4 clock cycles, and if SENSP is less than 2V, $\overline{FAULT}$ goes low and the part resets.
Overvoltage on SENSN	• If overvoltage persists for 8µs, $\overline{FAULT}$ goes low and the step-down DC-DC regulator is disabled. • After the fault is removed, the soft starts begins.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of V_Q (caused by the capacitor discharge) and V_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUPSW} - V_{SENSP}) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

where I_{OUT} is the maximum output current and D is the duty cycle.

Bypass SUPSW with a 4.7µF ceramic and 47µF electrolytic capacitor close to the SUPSW and PGND pins. Minimize PCB loop area for minimal EMI. Use small footprint components, such as an 0805 or smaller, to reduce total parasitic inductance.

DC-DC Output Capacitor Selection

The minimum capacitor required depends on output voltage, maximum device current capability, and the error-amplifier voltage gain. Use the following formula to determine the required output capacitor value:

$$C_{OUT(MIN)} = \frac{V_{REF} \times G_{CS} \times G_{EAMP}}{2\pi \times f_{CO} \times V_{OUT}}$$

where V_{REF} = 1.2V, G_{CS} = 2.5, f_{CO} = 0.125 x f_{SW}, and G_{EAMP} = 37.5V/V.

Table 4 lists the recommended inductor and capacitor values for several different switching frequencies. For proper functionality, a minimum amount of ceramic capacitance must be used regardless of f_{SW}. Additional capacitance for lower switching frequencies can be of the low-ESR electrolytic type (< 0.25ω).

DC-DC Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16984: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select the proper inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected. A good compromise between size and loss is a 35% LIR. The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{SENSP} \times (V_{SUPSW} - V_{SENSP})}{V_{SUPSW} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{SUPSW}, V_{SENSP}, and I_{OUT} are typical values (such that efficiency is optimum for nominal operating conditions). Table 4 shows recommended inductor values at various switching frequencies.

Table 4. Output Inductor and Capacitor Value vs. f_{SW}

f_{SW} (kHz)	L (µH)	MINIMUM C_{OUT} (µF)	RECOMMENDED C_{OUT}
2200	2.2	13	22µF ceramic
440	10	65	3 x 22µF ceramic*
440	10	65	22µF ceramic + low-ESR 68µF electrolytic (< 0.25Ω)
220	20	130	22µF ceramic + low-ESR 120µF electrolytic (< 0.25Ω)

**Use only ceramic capacitance when possible.*

DC-DC Diode Selection

The device requires an external Schottky diode rectifier as a freewheeling diode. Connect this rectifier close to the MAX16984 using short PCB traces. In FPWM mode, the Schottky diode helps minimize efficiency losses by diverting the inductor current that would otherwise flow through the low-side MOSFET. Choose a rectifier with a reverse voltage rating greater than the maximum expected input voltage (V_{SUPSW}), while minimizing forward-voltage drop. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Choose a Schottky rectifier with a low diode capacitance at the reverse voltage operating point to minimize EMI caused from the diode ringing at turn-off.

USB-Voltage Adjustment

The precision, all internal, feedback-adjustment circuitry is designed to be used for adjusting the MAX16984 +5V DC-DC output voltage higher as the USB load current increases. This is required in automotive applications that use a permanently embedded and attached captive cable from the USB Host in the module, to the user-accessible USB connectors. These cables can be from 30cm to 3m in length. As the USB portable load currents increase for CDP/DCP (1.5A) and iPad (2.1A) applications, these captive cables experience even higher voltage drops.

Determining System Requirements

The nominal cable resistance (with tolerance) for both the USB power wire (BUS) and return GND wire should be determined from the cable manufacturer. In addition, be sure to include the resistance from any inline or PCB connectors. Determine the desired operating temperature range for the application.

A typical application presents a 200mΩ BUS resistance in the captive cable and also the same 200mΩ in the ground path. For this application, the detected voltage drop at the end of a captive cable with a load current of 2A will be 800mV. This voltage drop requires the voltage-adjustment circuitry of the MAX16984 to adjust the USB +5V and compensate for the drop in voltage to allow the voltage at the end of the cable to comply with either the USB 2.0, USB-IF BC1.2, or Apple requirements.

USB Loads

The MAX16984 is compatible with both USB-compliant and non-compliant loads. For compliant USB loads, when a USB device is physically plugged (ATTACHED) into the USB connector, it is not allowed to pull more than 30mA and must not present a capacitance to GND of more than 10µF. The device then begins its D+/D- connection and enumeration process. After completion of the CONNECT process, the device can pull 100mA/150mA and must not present a capacitance greater than 10µF. This is considered the compliant, hot inserted, USB load of 44ω || 10µF.

For noncompliant USB loads, the MAX16984 can also support both a hot insertion and soft start into a USB load of 2ω || 500µF.

Configure USB Output Current Limit

The current that the DC-DC converter is supplying to the USB load is monitored by the internal current-sense amplifier (SENSP, SENSN), and the MAX16984 integrates a configurable USB current-limit threshold. Connect a resistor from SENSO to GND to set the desired current limit. See Figure 8. To calculate the R_{SENSO} value:

- Choose desired current limit: I_{LIMIT}
- Calculate resistance required on SENSO:

$$R_{SENSO} = \frac{1.2}{I_{LIMIT} \times R_{SENSE} \times 0.0025}$$

Note: 0.0025 is SENSO transconductance value, G_{SENSO} (typ).

Configure DC-DC Output-Voltage Adjustment

The DC-DC output voltage increases linearly as the voltage on FBMAX increases. To calculate the R_{FBMAX} value:

- Choose current-sense resistor used for sensing current (R_{SENSE}).
- Choose the load current to correct for I_{LOAD}.
- Calculate the total cable resistance to correct for R_{CABLE}.
- Calculate the required voltage (V_{ADJUST}) to increase the DC-DC output voltage.

$$V_{ADJUST} = I_{LOAD} \times (R_{SENSE} + R_{CABLE})$$

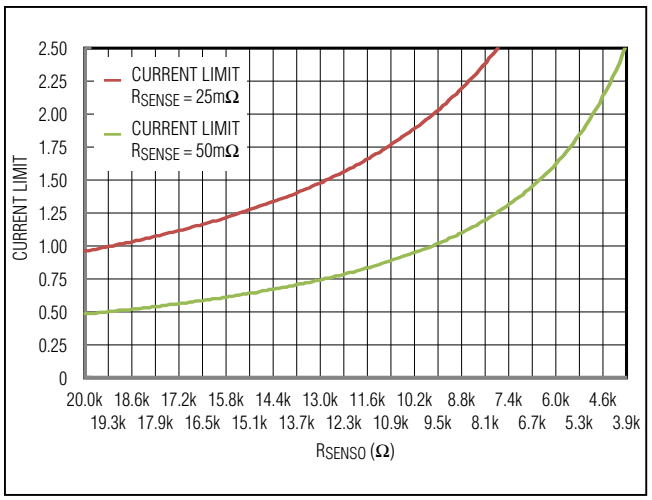


Figure 8. USB Current Limit: R_{SENSO} vs. Current Limit

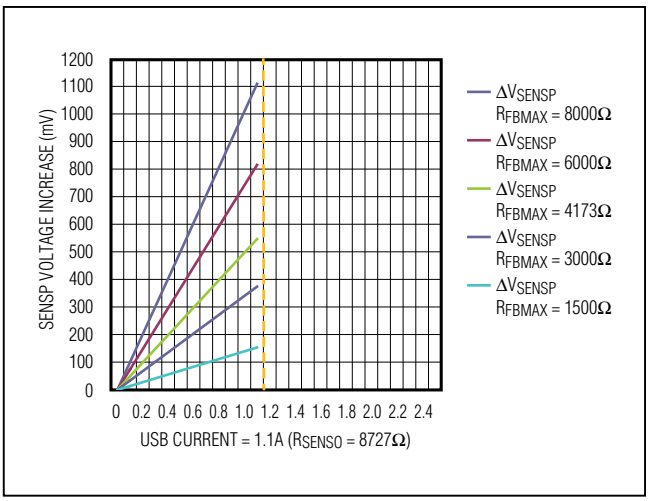


Figure 10. Increase in SENSP vs. USB Current

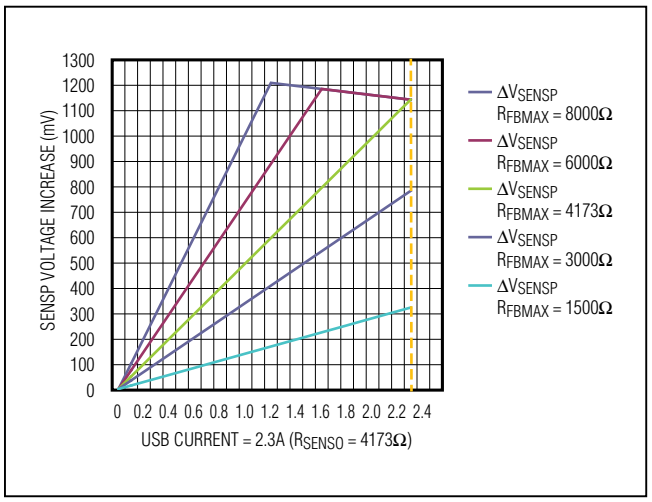


Figure 9. Increase in SENSP vs. USB Current

- Determine the setting needed for FBPER. This selects the SENSP Analog Adjustment Gain (A_{SENSP}) to increase the DC-DC converter for the application and minimizes/optimizes the DC-DC adjustment range. See Figure 9 and Figure 10.

If $\frac{V_{ADJUST}}{5.05V} \geq 12.5\%$

Then V_{FBPER} = 0V, else V_{FBPER} = 3.3V.

$V_{FBPER} = 0V \rightarrow A_{SENSP} = 1.069$

$V_{FBPER} = 3.3V \rightarrow A_{SENSP} = 0.535$

The voltage at FBMAX follows the equation below.

$$V_{FBMAX} = I_{LOAD} \times R_{SENSE} \times 0.0025 \times R_{FBMAX}$$

Note: 0.0025 is FBMAX transconductance value, G_{FBMAX} (typ).

Calculate the R_{FBMAX} resistor, such that at I_{LOAD}, the DC-DC output is increased by V_{ADJUST}.

$$R_{FBMAX} = \frac{V_{ADJUST} + (5.05 \times I_{LOAD} \times 0.012)}{I_{LOAD} \times R_{SENSE} \times 0.0025 \times A_{SENSP}}$$

With this R_{FBMAX}, maximum adjustment occurs as V_{FBMAX} crosses the internal 1.2V threshold.

Therefore:

$$V_{SENSP(MAX)} = 1.2 \times A_{SENSP}$$

Tuning of USB Data Lines

USB HS mode requires careful PCB layout with 90Ω controlled differential-impedance matched traces of equal lengths with no stubs or test points. For optimal eye diagram with maximum peaking at the end of the captive cable, insert a tuning capacitor and tuning inductor on either side of MAX16984 as close as possible to the HVD+/- and D+/- pins. These values are layout dependent. Initial target values are shown in Figure 11. Figure 12 to Figure 16 show performance of the MAX16984 with and without tuning for both near and far USB test locations. Contact Maxim's applications team for assistance with the tuning process.

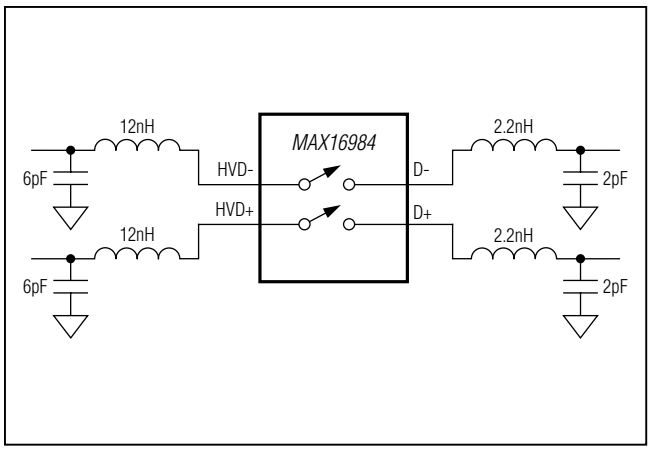


Figure 11. Tuning of Data Lines

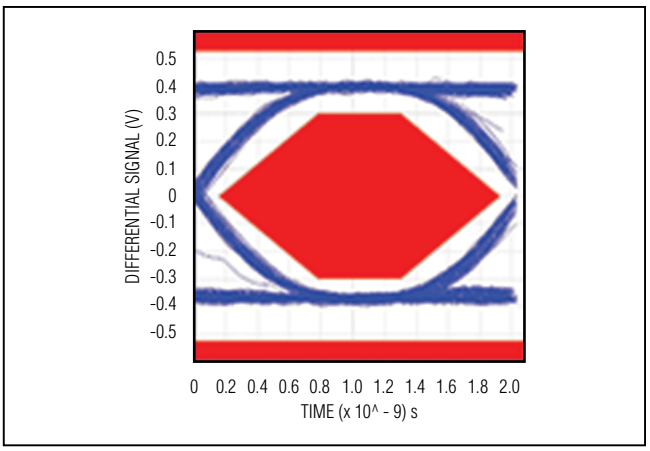


Figure 14. Tuned Near Eye Diagram (with Data Switch)

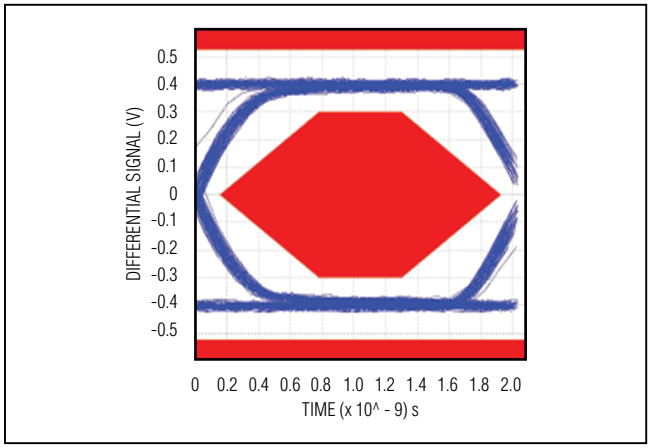


Figure 12. Near Eye Diagram (with No Switch)

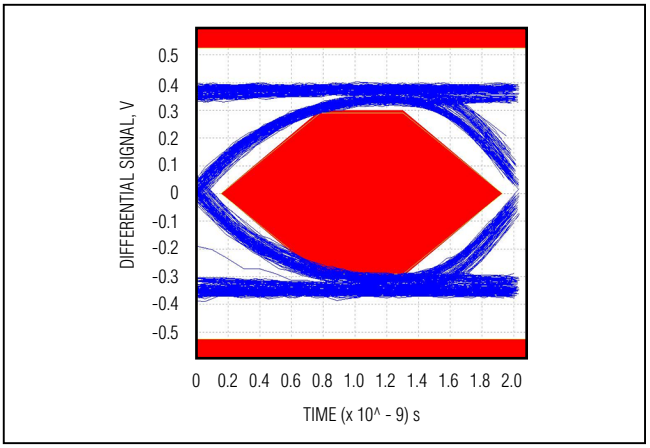


Figure 15. Untuned Far Eye Diagram, 3-Meter Cable

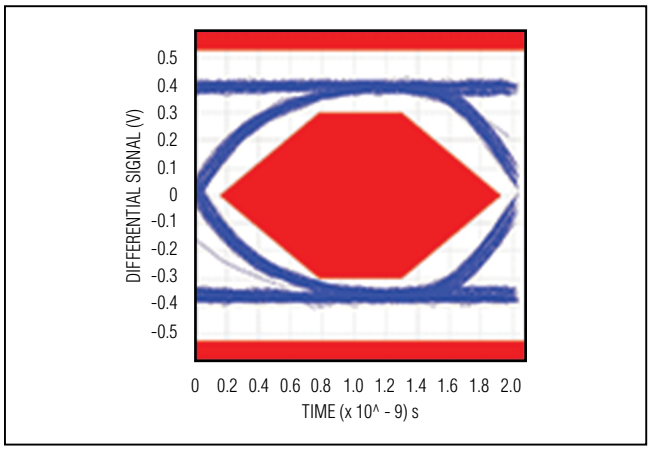


Figure 13. Untuned Near Eye Diagram (with Data Switch)

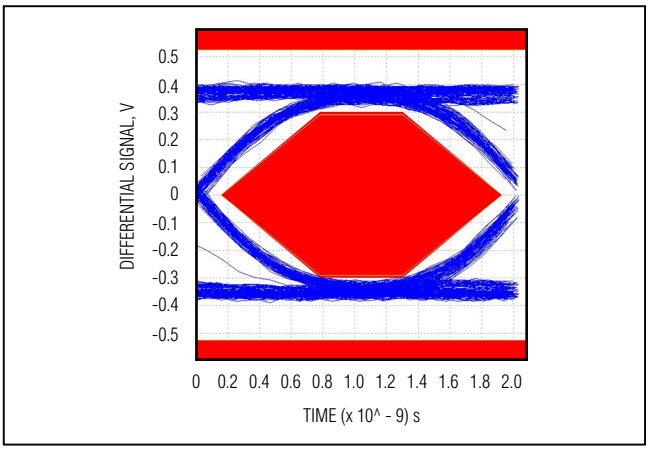


Figure 16. Tuned Far Eye Diagram, 3-Meter Cable

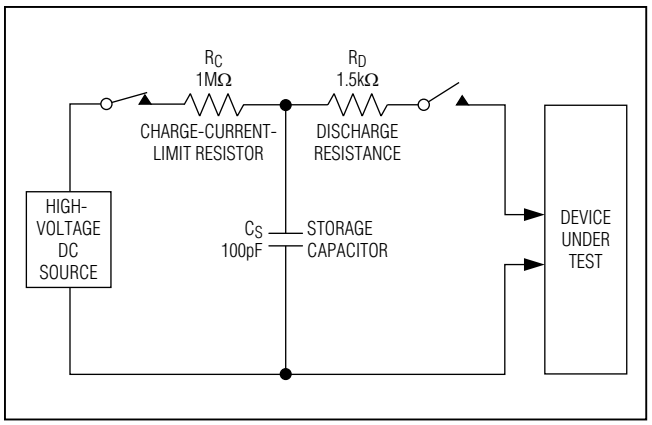


Figure 17. Human Body ESD Test Model

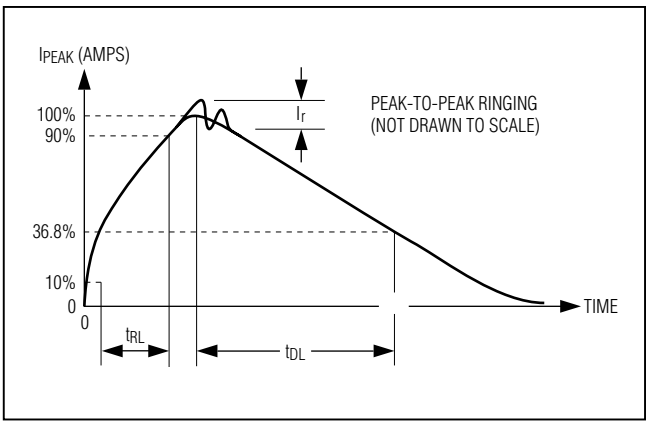


Figure 18. Human Body Current Waveform

USB Data Line Common-Mode Choke Placement

Most automotive applications use a USB-optimized common-mode choke to mitigate EMI signal from both leaving and entering the module. Optimal placement for this EMI choke is directly at the module USB connector. This common-mode choke does not replace the need for the tuning inductors previously mentioned.

ESD Protection

The MAX16984 should be placed as close as possible to the module USB connector for optimal ESD performance. No external ESD-protection diodes are required when using the MAX16984. Maxim devices incorporate ESD-protection structures to protect against electrostatic discharges encountered during handling and assembly. The MAX16984 provides additional protection against static electricity. Maxim's state-of-the-art structures protect against ESD of ±25kV on HVD+ and HVD-. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX16984 continues to work without latchup, while other solutions can latch up and require the power to be cycled. The MAX16984 is characterized for protection to the following limits:

1) ±25kV ISO 10605 Air Gap
2) ±8kV ISO 10605 Contact
3) ±15kV IEC 61000-4-2 Air Gap
4) ±8kV IEC 61000-4-2 Contact
5) ±15kV 330Ω, 330pF Air Gap
6) ±8kV 330Ω, 330pF Contact

Note: All application-level ESD testing is performed using a MAX16984 evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body Model

Figure 17 shows the Human Body Model, and Figure 18 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

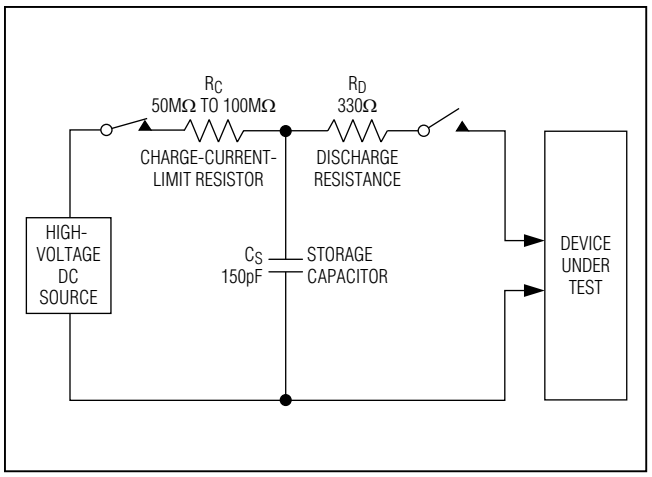


Figure 19. IEC 61000-4-2 ESD Test

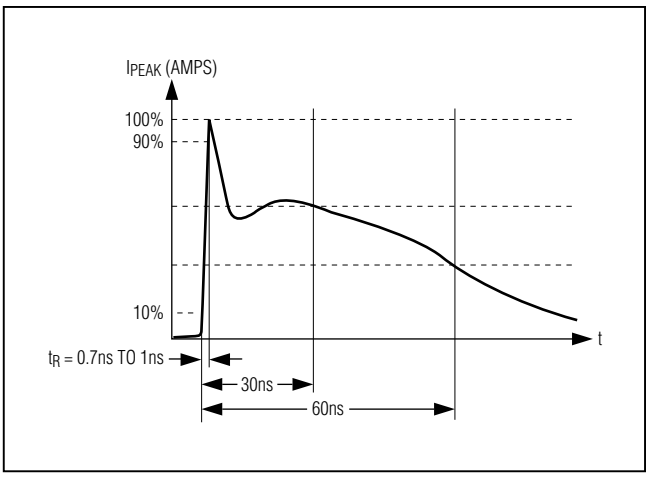
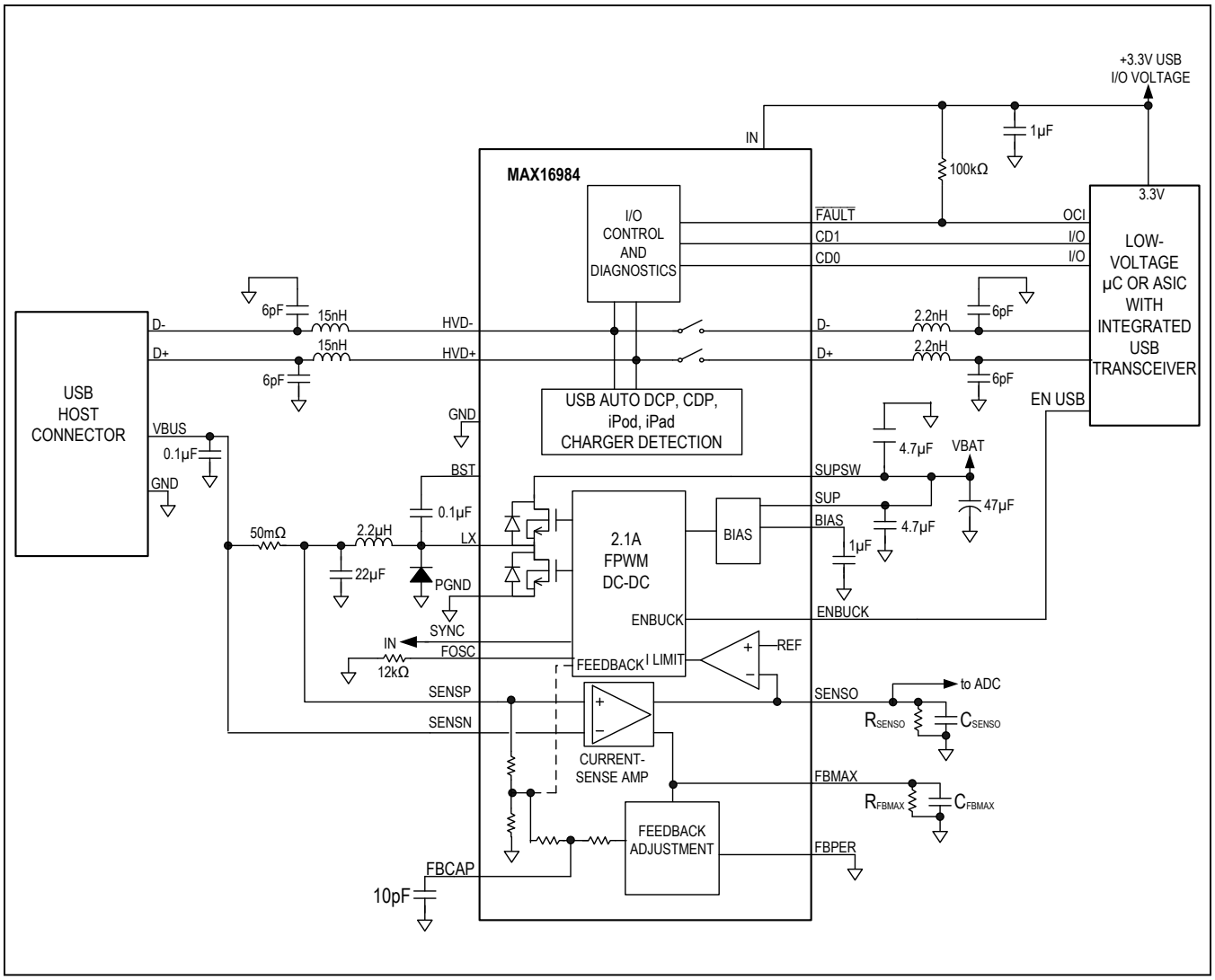


Figure 20. IEC 61000-4-2 ESD Generator Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX16984 helps users design equipment that meet Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 19), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 20 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	SPREAD SPECTRUM	PIN-PACKAGE
MAX16984RAGI/VY+	-40°C to +125°C	Disabled	28 QFND-EP* (SW)
MAX16984SAGI/VY+	-40°C to +125°C	Enabled	28 QFND-EP* (SW)
MAX16984RATI/V+	-40°C to +125°C	Disabled	28 TQFN-EP*
MAX16984SATI/V+	-40°C to +125°C	Enabled	28 TQFN-EP*
MAX16984RACIL/VY+	-40°C to +125°C	Disabled	28 CPQFN-EP* (SW)
MAX16984SACIL/VY+	-40°C to +125°C	Enabled	28 CPQFN-EP* (SW)
MAX16984RACIL/V+	-40°C to +125°C	Disabled	28 CPQFN-EP*
MAX16984SACIL/V+	-40°C to +125°C	Enabled	28 CPQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive-qualified part.
*EP = Exposed pad.
(SW) = Side wettable.
Tape-and-reel versions available—contact factory for availability.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 QFND-EP (Side-Wettable)	G2855Y+2	21-0563	90-0375
28 TQFN-EP	T2855+6	21-0140	90-0026
28 CPQFN-EP	CP2844+1	21-100469	90-100204
28 CPQFN-EP (Side-Wettable)	CP2844Y+1	21-100471	90-100202

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	7/13	Corrected values/figures, updated *Electrical Characteristics* table specs, and clarified spread-spectrum information	3–6, 11, 12, 17, 19, 20, 22, 27, 28, 31,
2	12/14	Updated *Switching Frequency (FOSC, SYNC)* section and *Typical Operating Circuit*	18, 31
3	4/15	Updated *Benefits and Features* section, added new Note 1 to *Absolute Maximum Ratings* and renumbered remaining notes through end of *Electrical Characteristics,* updated pins 15 and 16 in *Pin Description* table, updated *Tuning of USB Data Lines* section and *Typical Operating Circuit*	1–6, 16, 27, 31
4	5/16	Removed future product references	32
5	9/16	Updated *Switching Frequency (FOSC, SYNC)* section	8
6	5/18	Added new footnote for tape-and-reel versions under *Ordering Information* table	32
7	2/21	Updated *Benefits and Features, Package Thermal Characteristics, Pin Configuration, Pin Description, Ordering Information, and Package Information*	1, 2, 15, 16, 17
8	3/21	*Updated Pin Configuration*	15

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